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Interleaved ZVS Resonant Converter with a Parallel-Series Connection

Bor-Ren Lin† and Sin-Jhih Shen*

†*Dept. of Electrical Eng., National Yunlin University of Science and Technology, Yunlin, Taiwan

Abstract

This paper presents an interleaved resonant converter with a parallel-series transformer connection in order to achieve ripple current reduction at the output capacitor, zero voltage turn-on for the active switches, zero current turn-off for the rectifier diodes, less voltage stress on the rectifier diodes, and less current stress on the transformer primary windings. The primary windings of the two transformers are connected in parallel in order to share the input current and to reduce the root-mean-square (*rms*) current on the primary windings. The secondary windings of the two transformers are connected in series in order to ensure that the transformer primary currents are balanced. A full-wave diode rectifier is used at the output side to clamp the voltage stress of the rectifier diode at the output voltage. Two circuit modules are operated with the interleaved PWM scheme so that the input and output ripple currents are reduced. Based on the resonant behavior, all of the active switches are turned on under zero voltage switching (ZVS), and the rectifier diodes are turned off under zero current switching (ZCS) if the operating switching frequency is less than the series resonant frequency. Finally, experiments with a 1*k*W prototype are described to verify the effectiveness of the proposed converter.

Key words: Interleaved PWM, LLC converter, VCO, ZCS, ZVS

I. INTRODUCTION

To mitigate the environmental pollution and climate changes resulting from fossil fuel based power generation, soft switching power converters have been proposed recently to meet the demand for high efficiency from organizations such as the Environment Protection Agency (EPA) and the Climate Saver Computing Initiative (CSCI). There are two different kinds of control schemes related to the switching frequency in soft switching converters. One is based on a constant switching frequency with a variable duty cycle, while the other is based on a constant duty cycle and a variable switching frequency. Power converters with constant switching frequency and zero voltage switching (ZVS) techniques, such as active clamped ZVS converters [1]-[5], asymmetric half-bridge converters [6]-[7] and phase-shift pulse-width modulation (PWM) converters [8]-[9], have been proposed for many years to reduce the switching losses of MOSFETs and to increase circuit efficiency. However, the ZVS effect of these techniques is limited to specific load conditions. Thus it is difficult to design optimal converters with wide load ranges. Power converters with a variable switching frequency and the ZVS technique such as resonant converters [10]-[15] have been proposed to achieve ZVS turn-on or zero current switching (ZCS) turn-off for active switches. In a conventional series resonant converter, the output voltage cannot be properly regulated under the no-load condition due to its limited voltage gain. In order to overcome the drawbacks of conventional series resonant converters, LLC series resonant converters [16]-[19] have been presented that have the advantages of a high conversion efficiency, a high power density and a high voltage gain. If the switching frequency is less than the series resonant frequency, the rectifier diodes at the secondary side can be turned off under ZCS to overcome the reverse recovery losses.

This paper presents an interleaved series resonant converter to achieve ZVS turn-on for all of the active switches, ZCS turn-off for the rectifier diodes, ripple current reduction at the output capacitor and load current sharing. Two converter modules connected in parallel are used in the proposed circuit to share the load current and to reduce the current stress of the active switches. The interleaved PWM scheme is adopted to control the two circuit modules so that

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†Corresponding Author: linbr@yuntech.edu.tw
Tel: +886-5-5517456, Fax: +886-5-5312065, Nat'l Yunlin Univ. of Sci. and Tech.
*Dept. of Electrical Eng., National Yunlin University of Science and Technology, Taiwan

the ripple current at the output capacitors partially cancelled each other out. For each circuit module, a series resonant converter with two transformers and a full-wave diode rectifier is adopted to realize soft switching for all of the semiconductors. The input impedance of the resonant tank is related to the operating switching frequency. Thus the output voltage can be regulated by the variable switching frequency for different input voltages and load conditions. Since the input impedance of the resonant tank is operated at an inductive load, the active switches can be turned on under ZVS and the rectifier diodes can be turned off under ZCS if the switching frequency is less than the series resonant frequency. Thus the switching losses of the power switches and the reverse recovery losses of the rectifier diodes can be reduced. Two transformers are used in each circuit module to reduce the size of the magnetic core and to lessen the current stress on the primary windings. The secondary windings of the two transformers are connected in series in order to balance the transformer primary currents and to share the input current. For high output voltage applications, a full-wave diode rectifier is used in the secondary side to clamp the voltage stress of the rectifier diodes at the output voltage level. Compared to the conventional DC/DC converters used in low input voltage and high output voltage applications such as push-pull converters and symmetric half-bridge converters, the proposed converter has better circuit efficiency with a smaller size magnetic core and soft switching. Finally, experiments conducted on a 1*k*W prototype to verify the effectiveness of the proposed converter are described.

II. CIRCUIT CONFIGURATION

The basic block of a renewable energy power conversion system is given in Fig. 1(a). The front stage is a DC/DC converter and the second stage is a DC/AC inverter. Generally the input of the front stage comes from a PV based or fuel cell based renewable energy source with a low voltage input. The output of the DC/DC converter is a high DC voltage. Then a single-phase or a three-phase inverter is used to generate AC sinusoidal voltage. The circuit configuration of the proposed DC/DC converter is given in Fig. 1(b). Since the duty cycle for each of the active switches is equal to 0.5, the variable frequency modulation is adopted to regulate the output voltage. There are two circuit modules connected in parallel to share the input and output currents. The two circuit modules are operated with the interleaved scheme so that the input and output currents are partially cancelled. Therefore, the input and output ripple currents are reduced. Since the adopted circuit is used for high input current applications, the two transformers are connected in parallel in each of the circuit modules to share the input current. The secondary windings of the two transformers are connected in series in

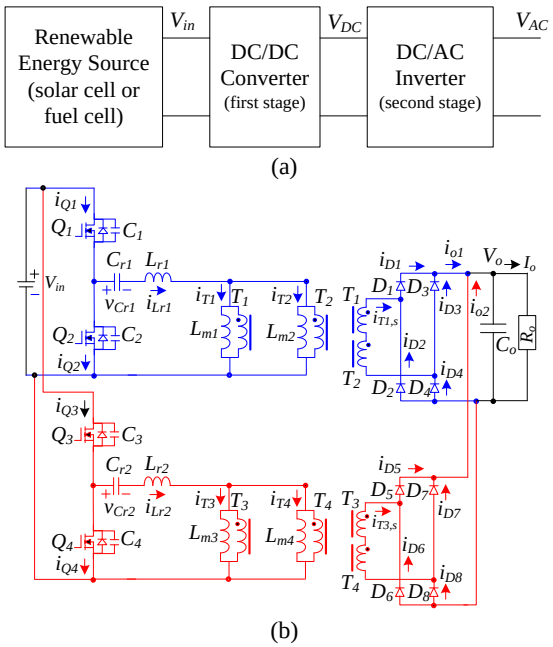


Fig. 1. Circuit configuration (a) renewable energy conversion system (b) the proposed DC/DC converter.

order to balance the two primary currents. V_{in} and V_o are the input and output terminal voltages. The input voltage V_{in} maybe a fuel cell voltage or a PV voltage from a solar panel. The first circuit module includes Q_1, Q_2, C_{r1}, L_{r1}, T_1, T_2, D_1~D_4 and C_o. The primary windings of T_1 and T_2 are connected in parallel to share the input inductor current i_{Lr1}. The secondary windings of T_1 and T_2 are connected in series to balance the primary currents, $i_{T1} \approx i_{T2} \approx i_{Lr1}/2$. The resonant tank in the first circuit module includes C_{r1}, L_{r1}, L_{m1} and L_{m2}. D_1~D_4 are the rectifier diodes. C_1 and C_2 are the output capacitances of Q_1 and Q_2, respectively. C_o is the output capacitance. Full-wave diode rectifiers are adopted in the secondary side in order to reduce the voltage stress on the rectifier diodes for high output voltage applications. The components of the second circuit module are Q_3, Q_4, C_{r2}, L_{r2}, T_3, T_4, D_5~D_8 and C_o. The primary and secondary windings of T_3 and T_4 are connected in parallel and series respectively to share the input inductor current i_{Lr2} and to balance the two primary currents $i_{T3} \approx i_{T4}$. The resonant tank in the second circuit module includes C_{r2}, L_{r2}, L_{m3} and L_{m4}. Based on the series resonant phenomenon, the active switches Q_1~Q_4 are turned on under ZVS if the resonant tank is operated as an inductive load. Therefore, the switching losses on the active switches are reduced to increase the circuit efficiency. On the other hand, the rectifier diodes can be turned off under ZCS if the switching frequency of the proposed converter is less than the series resonant frequency under a full load and a maximum input voltage. Thus the reverse recovery losses on fast recovery diodes are reduced. The proposed converter can be used for low input voltage and high output voltage

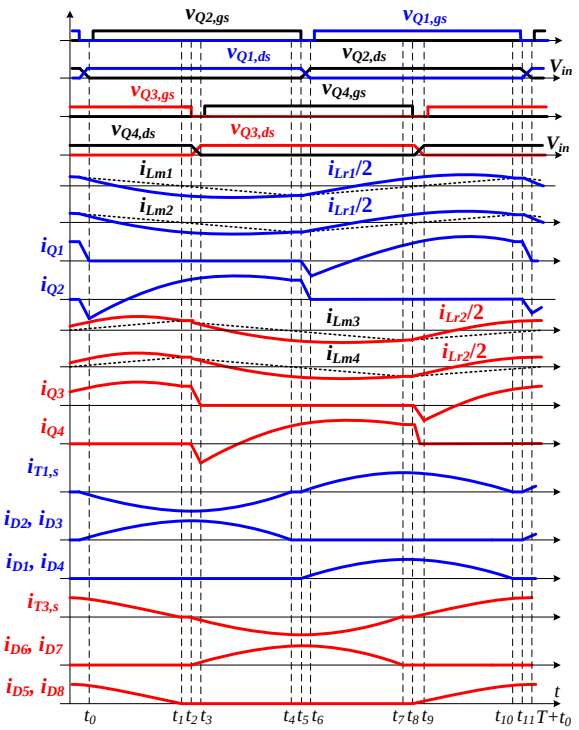


Fig. 2. Key waveforms of the proposed converter.

applications such as the battery-based DC/DC converters, the high power discharger systems and the DC/DC converters used in renewable energy systems.

III. Operation Principle and System Analysis

Each switch in the proposed converter is turned on with a 50% duty ratio. Therefore the output voltage regulation is controlled by a frequency modulation technique. The components of the two circuit modules are identical. The four transformers have the same turns ratio ($n=n_p/n_s$) and the same magnetizing inductance L_m. All of the active switches are ideal and have the same output capacitance ($C_1=C_2=C_3=C_4=C_{eq}$). Fig. 2 shows the key waveforms during a switching cycle. There are twelve operating modes in the proposed converter for each switching period. The equivalent circuits for each of the operating modes are shown in Fig. 3. Before time t_0, Q_3, D_2, D_3, D_5 and D_8 conduct. C_1 is charged and C_2 is discharged.

Mode 1 [$t_0 \le t < t_1$]: At time t_0, C_2 is discharged to zero voltage. Since $i_{Q2}<0$, the anti-parallel diode of Q_2 conducts. Switch Q_2 can be turned on at this moment to achieve ZVS. Since $i_{T1}<i_{Lm1}$, $i_{T2}<i_{Lm2}$, $i_{T3}>i_{Lm3}$ and $i_{T4}>i_{Lm4}$, diodes D_2, D_3, D_5 and D_8 conduct in this mode so that $v_{Lm1}=v_{Lm2}=-nV_o/2$ and $v_{Lm3}=v_{Lm4}=nV_o/2$. The magnetizing currents i_{Lm1} and i_{Lm2} decrease linearly with a slope of $-nV_o/(2L_m)$ and the magnetizing currents i_{Lm3} and i_{Lm4} increase linearly with a slope of $nV_o/(2L_m)$. C_{r1} and L_{r1} are resonant with the applied voltage $nV_o/2$ in circuit module 1, while C_{r2} and L_{r2} are resonant with the applied voltage V_{in}-$nV_o/2$ in circuit module 2. i_{Lr1} and v_{Cr1} decrease, and i_{Lr2} and v_{Cr2} increase in this mode. The resonant inductor currents i_{Lr1} and i_{Lr2} and the capacitor voltages v_{Cr1} and v_{Cr2} in this mode are expressed as:

$$i_{Lr1}(t)=\frac{nV_o/2-v_{Cr1}(t_0)}{Z_r}\sin\omega_r(t-t_0)+i_{Lr1}(t_0)\cos\omega_r(t-t_0) \quad (1)$$

$$i_{Lr2}(t)=\frac{V_{in}-nV_o/2-v_{Cr2}(t_0)}{Z_r}\sin\omega_r(t-t_0)+i_{Lr2}(t_0)\cos\omega_r(t-t_0) \quad (2)$$

$$v_{Cr1}(t)=nV_o/2-[nV_o/2-v_{Cr1}(t_0)]\cos\omega_r(t-t_0)+i_{Lr1}(t_0)Z_r\sin\omega_r(t-t_0) \quad (3)$$

$$v_{Cr2}(t)=V_{in}-nV_o/2-[V_{in}-nV_o/2-v_{Cr2}(t_0)]\times\cos\omega_r(t-t_0)+i_{Lr2}(t_0)Z_r\sin\omega_r(t-t_0) \quad (4)$$

where $Z_r=\sqrt{L_r/C_r}$ and $\omega_r=1/\sqrt{L_rC_r}$. Power is transferred from the input terminal voltage V_{in} to the output load through Q_3, C_{r2}, L_{r2}, T_3, T_4, D_5 and D_8. This mode ends at time t_1 when $i_{Lm3}=i_{T3}$ and $i_{Lm4}=i_{T4}$. Then diodes D_5 and D_8 are off.

Mode 2 [$t_1 \le t < t_2$]: This mode starts at t_1 when $i_{Lm3}=i_{T3}$ and $i_{Lm4}=i_{T4}$. Then diodes D_5 and D_8 are off in circuit module 2. Since Q_3 still conducts in this mode, C_{r2}, L_{r2}, L_{m3} and L_{m4} are resonant in circuit module 2. On the other hand, C_{r4}, L_{r4} and L_{m4} are also resonant with the input voltage $V_{in}/2$. i_{Lr2} and v_{Cr2} are obtained as:

$$i_{Lr2}(t)=\frac{V_{in}-v_{Cr2}(t_1)}{Z_p}\sin\omega_p(t-t_1)+i_{Lr2}(t_1)\cos\omega_p(t-t_1) \quad (5)$$

$$v_{Cr2}(t)=V_{in}-[V_{in}-v_{Cr2}(t_1)]\cos\omega_p(t-t_1)+i_{Lr2}(t_1)Z_p\sin\omega_p(t-t_1) \quad (6)$$

where $Z_p=\sqrt{\frac{L_r+L_m/2}{C_r}}$ and $\omega_r=1/\sqrt{(L_r+L_m/2)C_r}$.

The operation of circuit module 1 in this mode is the same as the operation in mode 1.

Mode 3 [$t_2 \le t < t_3$]: At time t_2, Q_3 is turned off and diodes D_6 and D_7 conduct. Thus $v_{Lm3}=v_{Lm4}=-nV_o/2$ and i_{Lm3} and i_{Lm4} decrease in this mode. Since $i_{Lr2}(t_2)>0$, C_3 is charged and C_4 is discharged. If the energy stored in L_{r2} at time t_2 is greater than the energy stored in C_3 and C_4, then C_4 can be discharged to zero voltage at time t_3. The capacitor voltages v_{C3} and v_{C4} are expressed as:

$$v_{C3}(t)\approx i_{Lr2}(t_2)(t-t_2)/(2C_{eq}) \quad (7)$$

$$v_{C4}(t)\approx V_{in}-i_{Lr2}(t_2)(t-t_2)/(2C_{eq}) \quad (8)$$

The operation behavior of circuit module 1 is the same as the circuit operation in mode 2.

Mode 4 [$t_3 \le t < t_4$]: At time t_3, C_4 is discharged to zero voltage so that the anti-parallel diode of Q_4 conducts. Before i_{Q4} becomes positive, Q_4 is turned on under ZVS. Since D_2, D_3,

D_6 and D_7 conduct in this mode, the magnetizing voltages $v_{Lm1}=v_{Lm2}=v_{Lm3}=v_{Lm4}= -nV_o/2$. Thus i_{Lm1}~i_{Lm4} decrease in this mode. C_{r1} and L_{r1} are resonant in circuit module 1, while C_{r2} and L_{r2} are resonant in circuit module 2.

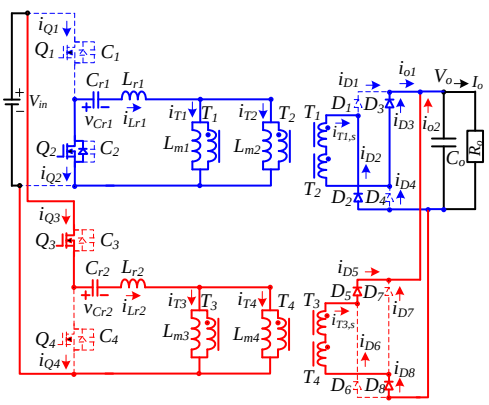
Mode 5 [$t_4 \le t < t_5$]: At time t_4, $i_{Lm1}=i_{T1}$ and $i_{Lm2}=i_{T2}$ in circuit module 1 such that diodes D_1~D_4 are reverse biased. Since Q_2 still conducts, C_{r1}, L_{r1}, L_{m1} and L_{m2} are resonant in this mode. The operation behavior of circuit module 2 is the same as the circuit operation in mode 4.

Mode 6 [$t_5 \le t < t_6$]: At time t_5, Q_2 turns off and diodes D_1 and D_4 conduct so that $v_{Lm1}=v_{Lm2}=nV_o/2$. Therefore, i_{Lm1} and i_{Lm2} increase in this mode. Since $i_{Lr1}(t_5)<0$, C_1 is discharged and C_2 is charged. If the energy stored in L_{r1} at time t_5 is greater than the energy stored in C_1 and C_2, then C_1 can be discharged to zero voltage at time t_6. The operation behavior of circuit module 2 in this mode is the same as the operation in mode 5.

Mode 7 [$t_6 \le t < t_7$]: At time t_6, C_1 is discharged to zero voltage. Since $i_{Q1}<0$, the anti-parallel diode of Q_1 conducts. Therefore, Q_1 can be turned on at this moment to achieve ZVS. Since D_1, D_4, D_6 and D_7 conduct in this mode, $v_{Lm1}=v_{Lm2}=nV_o/2$ and $v_{Lm3}=v_{Lm4}=-nV_o/2$ so that i_{Lm1} and i_{Lm2} increase, while i_{Lm3} and i_{Lm4} decrease. L_{r1} and C_{r1} are resonant with the applied voltage $V_{in}-nV_o/2$ in circuit module 1, while L_{r2} and C_{r2} are resonant with the applied voltage $nV_o/2$ in circuit module 2.

Mode 8 [$t_7 \le t < t_8$]: At time t_7, $i_{Lm3}=i_{T3}$ and $i_{Lm4}=i_{T4}$ so that diodes D_5~D_8 are off. Since Q_4 still conducts, C_{r2}, L_{r2}, L_{m3} and L_{m4} are resonant in module 2. The circuit operation of circuit module 1 is the same as the circuit operation in mode 7.

Mode 9 [$t_8 \le t < t_9$]: At time t_8, Q_4 is turned off and diodes D_5 and D_8 conduct. Therefore, $v_{Lm3}=v_{Lm4}=nV_o/2$ and the magnetizing currents i_{Lm3} and i_{Lm4} increase in this mode. Since $i_{Lr2}(t_8)<0$, C_4 is charged and C_3 is discharged. If the energy stored in L_{r2} at time t_8 is greater than the energy stored in C_3 and C_4, then C_3 can be discharged to zero voltage at time t_9. The operation behavior of circuit module 1 in this mode is the same as the circuit operation in mode 8.



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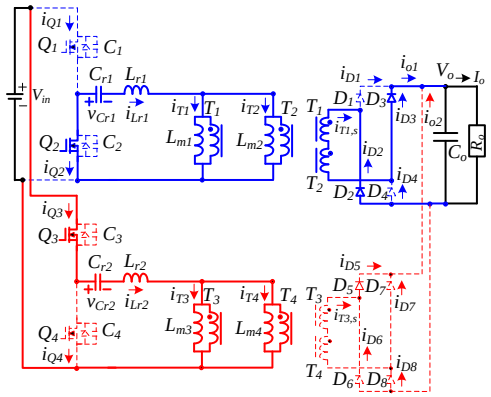

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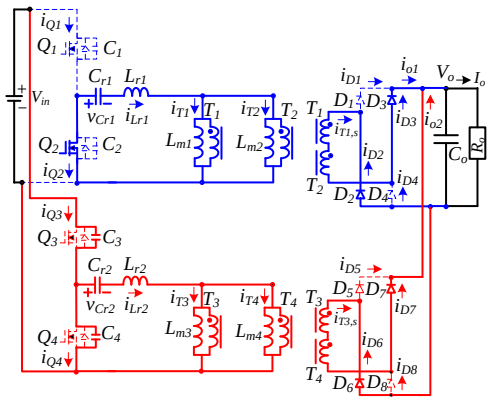

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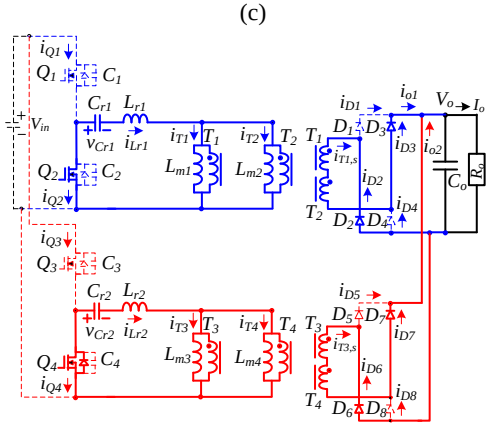

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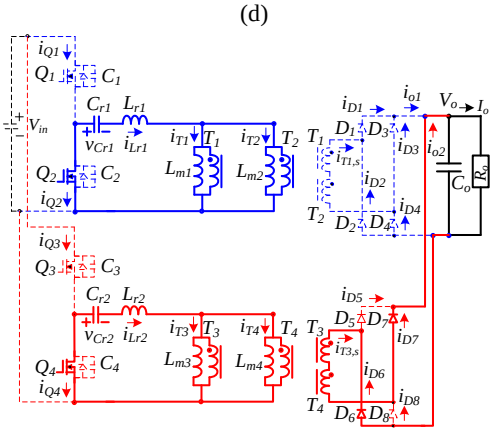

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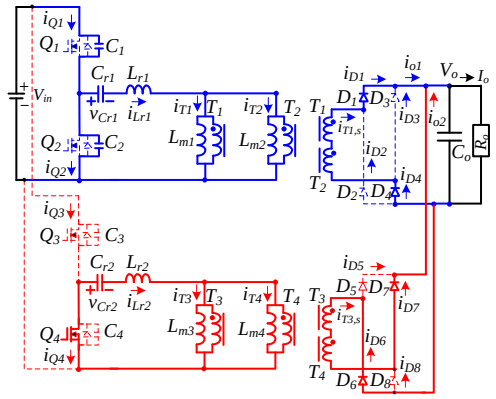

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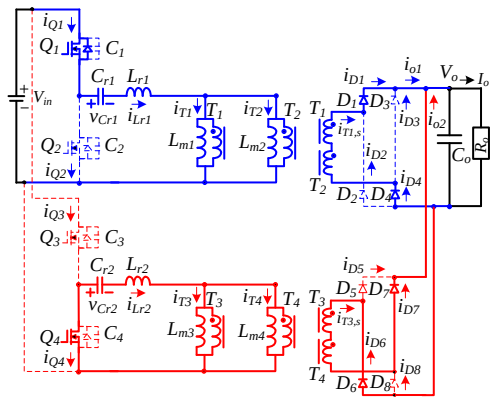

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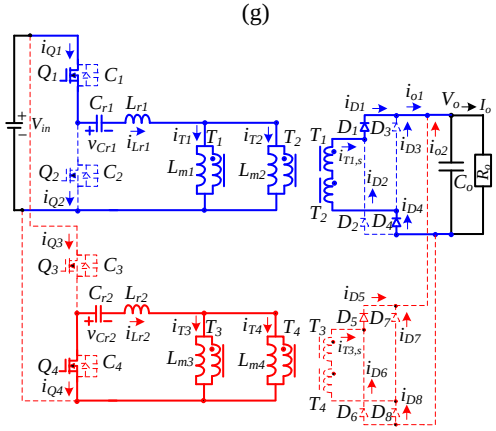

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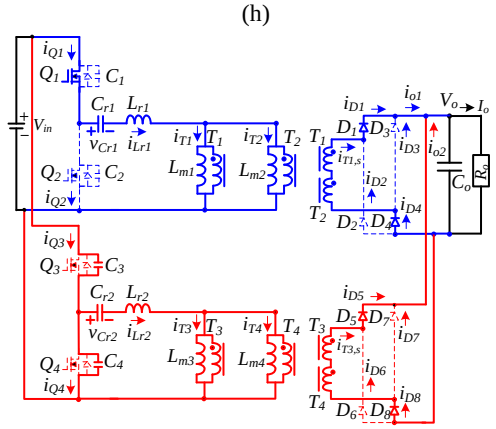

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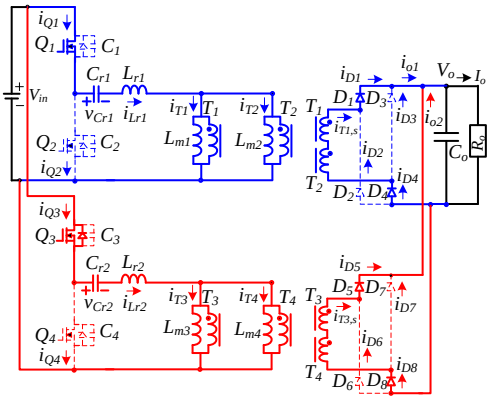

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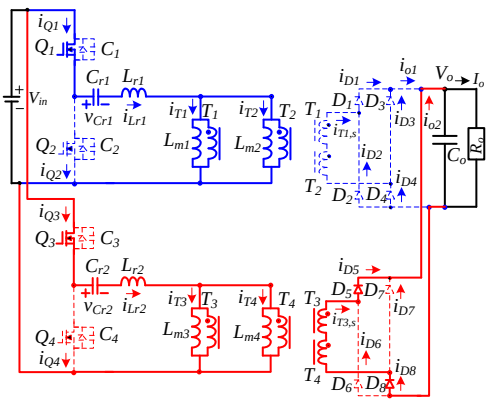

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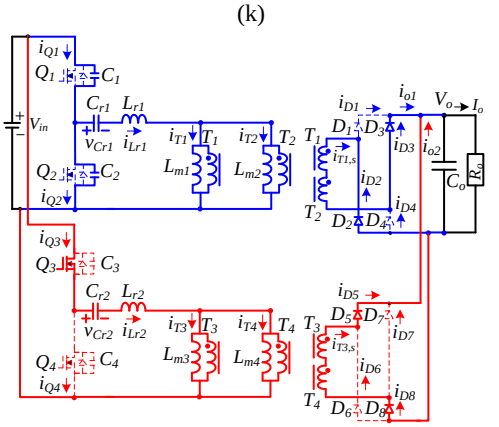


(l)

Fig. 3 Operation modes of the proposed converter during one switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8 (i) mode 9 (j) mode 10 (k) mode 11 (l) mode 12.

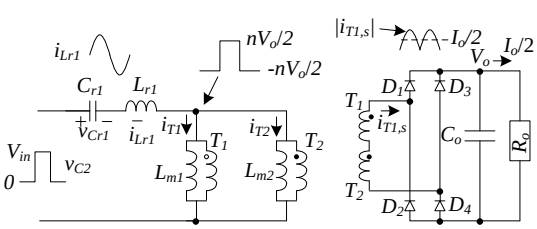


Fig. 4. Equivalent circuit of circuit module 1.

Mode 10 [$t_9 \le t < t_{10}$]: At time t_9, capacitor C_3 is discharged to zero voltage. Since $i_{Lr2}(t_9)<0$, the anti-parallel diode of Q_3 conducts. Thus Q_3 can be turned on at this moment to achieve ZVS. Diodes D_1, D_4, D_5 and D_8 conduct in this mode so that $v_{Lm1}=v_{Lm2}=v_{Lm3}=v_{Lm4}=nV_o/2$. The magnetizing currents i_{Lm1}~i_{Lm4} increase in this mode. Input power is delivered to the output load through Q_1, C_{r1}, L_{r1}, T_1, T_2, D_1 and D_4 in circuit module 1 and through Q_3, C_{r2}, L_{r2}, T_3, T_4, D_5 and D_8 in circuit module 2. Therefore, i_{Lr1}, i_{Lr2}, v_{Cr1} and v_{Cr2} increase.

Mode 11 [$t_{10} \le t < t_{11}$]: At time t_{10}, $i_{Lm1}=i_{T1}$ and $i_{Lm2}=i_{T2}$ so that diodes D_1~D_4 are all off in circuit module 1. Since Q_1 still conducts, C_{r1}, L_{r1}, L_{m1} and L_{m2} are resonant with the applied voltage V_{in}. The operation behavior of circuit module 2 in this mode is the same as the circuit operation in mode 10.

Mode 12 [$t_{11} \le t < T+t_0$]: At time t_{11}, Q_1 is turned off and diodes D_2 and D_3 conduct. Thus $v_{Lm1}=v_{Lm2}=-nV_o/2$. The magnetizing currents i_{Lm1} and i_{Lm2} decrease in this mode. Since $i_{Lr1}(t_{11})>0$, C_1 is charged and C_2 is discharged. If the energy stored in L_{r1} at time t_{11} is greater than the energy stored in C_1 and C_2, then C_2 can be discharged to zero voltage at time $T+t_0$. Then the anti-parallel diode of Q_2 conducts. This is the last operating mode of the proposed converter during one switching period.

The power flow through the resonant tank is related to the switching frequency. All of the harmonics of the switching frequency are neglected in the following analysis. Fig. 4 shows an equivalent circuit of circuit module 1. The duty ratios of switches Q_1 and Q_2 are equal to 0.5. The input voltage of the resonant tank is a square waveform between 0 and V_{in}. The DC value and the fundamental root-mean-square (rms) value of the input voltage v_{C2} are $V_{in}/2$ and $\sqrt{2}V_{in}/\pi$, respectively. The output side of circuit module 1 is driven by a quasi-sinusoidal current. When inductor current $i_{T1}>i_{Lm1}$, D_1 and D_4 conduct and $v_{Lm1}= v_{Lm2}=nV_o/2$. If $i_{T1}<i_{Lm1}$, then D_2 and D_3 conduct and $v_{Lm1}= v_{Lm2}=-nV_o/2$. Thus the fundamental rms value of the magnetizing voltage is expressed as $v_{Lm1,rms}=\sqrt{2}nV_o/\pi$. Since the output current of circuit module 1 is equal to $I_o/2$, the rms value of the secondary winding current is equal to $i_{T1,s,rms}=\pi I_o/(4\sqrt{2})$. Thus the load resistance R_o reflected to the transformer primary side is given as:

$$R_{ac1}=R_{ac2}=\frac{v_{Lm1,rms}}{i_{T1,s,rms}/n}=\frac{8n^2}{\pi^2}R_o \tag{9}$$

The AC resonant tank (L_{r1} and C_{r1}), shown in Fig. 5, is excited by an effectively sinusoidal input voltage $v_{C2,f}$ and it drives the effective resistive loads R_{ac1} and R_{ac2} in circuit module 1. The AC voltage gain of circuit module 1, based on Fig. 5, is expressed in (10).

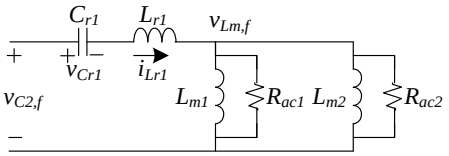


Fig. 5. AC resonant tank of circuit module 1 with fundamental switching frequency.

TABLE I

KEY CIRCUIT PARAMETERS OF THE PROTOTYPE CIRCUIT

Input voltage V_{in}	42 V~52 V
Output voltage V_o / Current I_o	400V/2.5 A
Series resonant frequency f_r	100 kHz
Switches Q_1~Q_4	IRFP064
Diodes D_1~D_8	30ETH06
Turns ratio of T_1~T_4	n_p:n_s=6:42
Resonant inductances L_{r1}, L_{r2}	0.633μH
Magnetizing inductances L_{m1}~L_{m4}	7.6μH
Resonant capacitances C_{r1}, C_{r2}	4μF
Output capacitor C_o	1320μF/450V

$$|G_{ac}(f)|=1/\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2+Q^2(\frac{f_s}{f_r}-\frac{f_r}{f_s})^2} \tag{10}$$

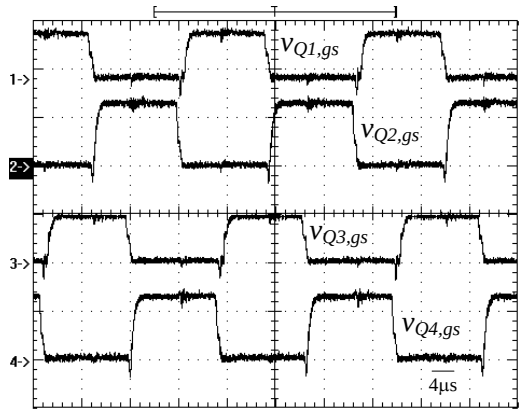
where $f_r=1/(2\pi\sqrt{L_{r1}C_{r1}})$, $Q=\sqrt{L_{r1}/C_{r1}}/(R_{ac1}/2)$, $k=2L_{r1}/L_{m1}$ and f_s is the switching frequency. The AC voltage gain is related to the switching frequency in (10). Therefore, the output voltage V_o can be regulated by the variation of the switching frequency f_s. Under the no load condition, R_{ac1} is infinite and the quality factor Q equals zero. Then the AC voltage gain under the no load condition is expressed as: $|G_{ac}(f)|_{Q=0}=1/[1+k(1-\frac{f_r^2}{f_s^2})]$.

If the design minimum DC voltage gain at the maximum input voltage and the maximum switching frequency is greater than the AC voltage gain under the no load condition, then the output voltage V_o can be controlled.

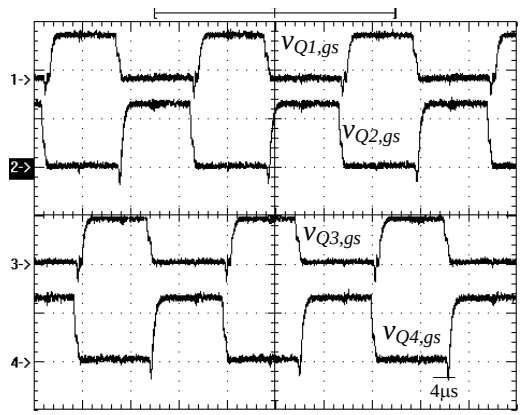
$$G_{dc,\min}=\frac{n(V_o+2V_f)}{V_{in,\max}}>1/[1+k(1-\frac{f_r^2}{f_{s,\max}^2})] =|G_{ac}(f)|_{Q=0,f_{s,\max}} \tag{11}$$

where V_f is the voltage drop across diodes D_1~D_4 and $f_{s,max}$ is the maximum switching frequency generated by the voltage controlled oscillator.

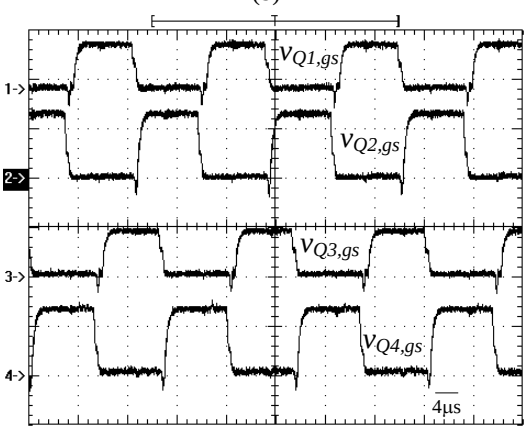
IV. EXPERIMENTAL RESULTS



(a)

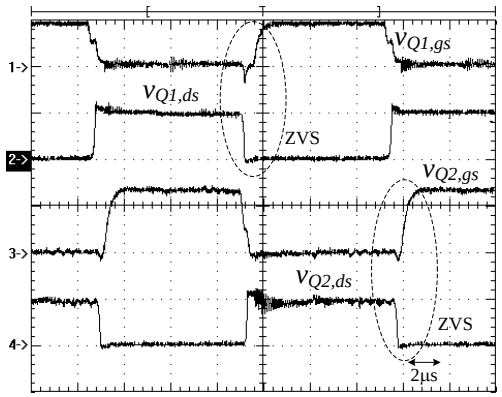


(b)

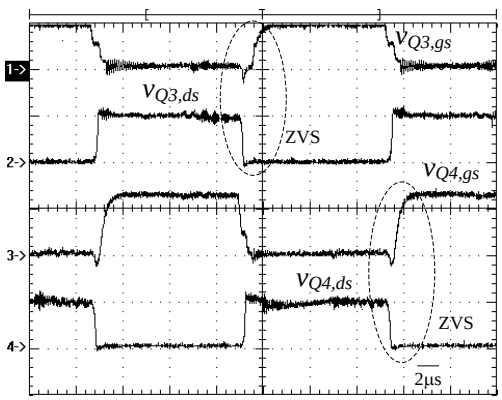


(c)

Fig. 6. results of gate voltages of Q_1~Q_4 at full load and input voltage (a) V_{in}=42V (b) V_{in}=48V (c) V_{in}=52V [$v_{Q1,gs}$~$v_{Q4,gs}$:10V/div].



(a)



(b)

Fig. 7. Measured gate voltage and drain voltage at V_{in}=48V and full load condition (a) Q_1 and Q_2 (b) Q_3 and Q_4 [$v_{Q1,gs}$~$v_{Q4,gs}$:10V/div; $v_{Q1,ds}$~$v_{Q4,ds}$:50V/div].

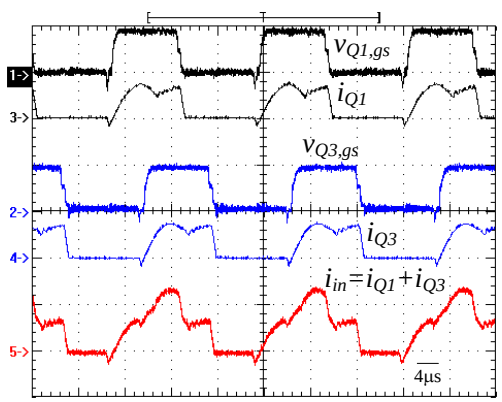


Fig. 8. Measured results of gate voltages, $v_{Q1,gs}$ and $v_{Q3,gs}$, switch currents, i_{Q1} and i_{Q3}, and the DC input current i_{in} at V_{in}=48V and full load condition [$v_{Q1,gs}$, $v_{Q3,gs}$:10V/div; i_{Q1}, i_{Q3}, i_{in}:50A/div].

Experimental results based on a laboratory prototype have been provided to demonstrate the performance of the proposed converter. The circuit parameters of the prototype circuit are shown in Table I. The variable switching frequency is adopted to generate the gate signals. The flip-flop circuits are used to generate the interleaved PWM signals. First, an LLC control IC based on a L6599 is used to generate two PWM signals. Then, two D-type flip-flop ICs are used to generate four PWM signals. Fig. 6 gives the experimental results for the gate voltages of Q_1~Q_4 at different input voltages and the full load condition. It can be observed that the gate voltage $v_{Q3,gs}$ lags the gate voltage $v_{Q1,gs}$ by one fourth of a switching period, and that the low input

voltage has less switching frequency. The measured gate voltage and the drain voltage of Q_1~Q_4 at an input voltage of V_{in}=48V and the full load condition are given in Fig. 7. Before Q_1~Q_4 are turned on, the drain voltages have been decreased to zero voltage. Therefore switches Q_1~Q_4 are turned on under ZVS from 20% to 100% load conditions. Fig. 8 gives the measured waveforms of the gate voltages, $v_{Q1,gs}$ and $v_{Q3,gs}$, the switch currents, i_{Q1} and i_{Q3}, and the DC input current i_{in} at V_{in}=48V and the full load condition. Since the currents i_{Q1} and i_{Q3} are phase-shifted by one-fourth of a switching period, the input current i_{in} has less current ripple. Fig. 9 shows the measured resonant inductor currents, i_{Lr1} and i_{Lr2}, and the resonant capacitor voltages, v_{Cr1} and v_{Cr2} at the full load condition. Fig. 10 gives the measured waveforms of i_{Lr1}, i_{T1} and i_{T2} for converter module 1 and i_{Lr2}, i_{T3} and i_{T4} for converter module 2 at the full load condition. The measured transformer primary currents are balanced so that i_{T1}=i_{T2}≈i_{Lr1}/2 and i_{T3}=i_{T4}≈i_{Lr2}/2. Fig. 11 shows the measured waveforms of the gate voltages, $v_{Q1,gs}$ and $v_{Q3,gs}$, and the diode currents i_{D1}, i_{D3}, i_{D5} and i_{D7} at V_{in}=48V and the full load condition. Before switches Q_1~Q_4 are turned off, the rectifier diode currents are decreased to zero. Thus diodes D_1~D_8 are all turned off under ZCS. Therefore, the reverse recovery losses of the rectifier diodes are reduced. Fig. 12 gives the measured results of the output currents i_{D1}+i_{D3} and i_{D5}+i_{D7} of the two circuit modules, the resultant output current i_{D1}+i_{D3}+i_{D5}+i_{D7} and the load voltage at the full load condition. The current i_{D1}+i_{D3}+i_{D5}+i_{D7} has less ripple current when compared to the ripple currents of i_{D1}+i_{D3} and i_{D5}+i_{D7}. The measured switching frequencies with different input voltages and different load conditions are shown in Fig. 13. The high input voltage requires a low DC voltage gain. Therefore, the operating switching frequency increases if the input terminal voltage V_{in} increases. A lower switching frequency is necessary if the load power is increased at the constant input terminal voltage. The measured efficiencies of the proposed converter under different load conditions are given in Fig. 14.

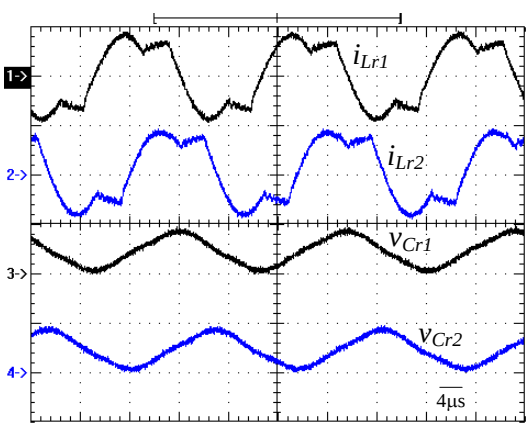


Fig. 9. Measured resonant inductor currents, i_{Lr1} and i_{Lr2}, and resonant capacitor voltages, v_{Cr1} and v_{Cr2} at full load condition [i_{Lr1}, i_{Lr2}:50V/div; i_{Lr1}, i_{Lr2}:50A/div].

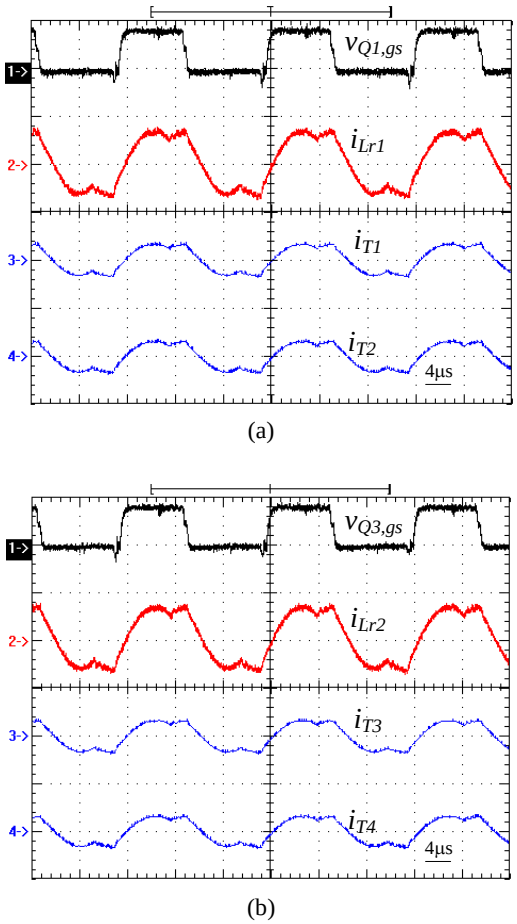


Fig. 10. Measured waveforms at nominal input voltage and full load (a) $v_{Q1,gs}$, i_{Lr1}, i_{T1} and i_{T2} for converter module 1 (b) $v_{Q3,gs}$, i_{Lr2}, i_{T3} and i_{T4} for converter module 2 [$v_{Q1,gs}$, $v_{Q3,gs}$:10V/div; i_{Lr1}, i_{Lr2}, i_{T1}, i_{T2}, i_{T3}, i_{T4}:50A/div].

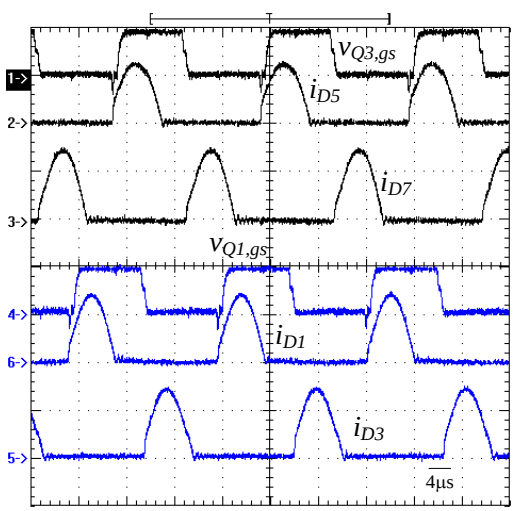


Fig. 11. Measured waveforms of the gate voltages, $v_{Q1,gs}$ and $v_{Q3,gs}$, and diode currents i_{D1}, i_{D3}, i_{D5} and i_{D7} at V_{in}=48V and full load condition [$v_{Q1,gs}$, $v_{Q3,gs}$:10V/div; i_{D1}, i_{D3}, i_{D5}, i_{D7}:2A/div].

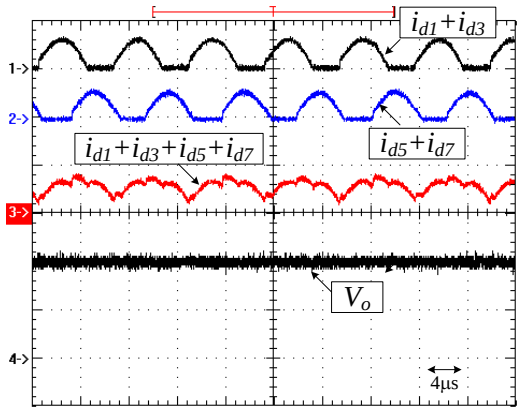


Fig. 12. Measured results of output currents $i_{D1}+i_{D3}$ and $i_{D5}+i_{D7}$ of two circuit modules, the resultant output current $i_{D1}+i_{D3}+i_{D5}+i_{D7}$ and output voltage V_o at full load condition [$i_{D1}+i_{D3}$, $i_{D5}+i_{D7}$, $i_{D1}+i_{D3}+i_{D5}+i_{D7}$:5A/div; V_o:200V/div].

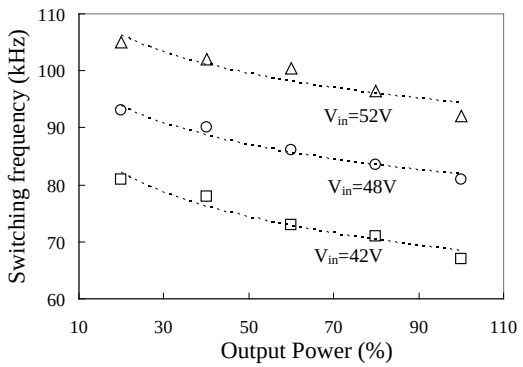


Fig. 13. Measured switching frequencies with different input voltages and load conditions.

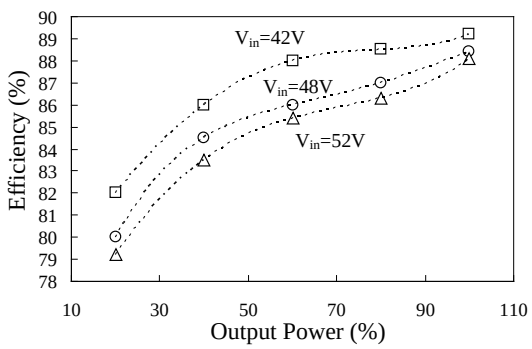


Fig. 14. Measured efficiencies of the proposed converter with different input voltages and load conditions.

V. CONCLUSION

This paper presents an interleaved series resonant converter to achieve ZVS turn-on for active switches and ZCS turn-off for rectifier diodes. Thus the switching losses and the reverse recovery losses of the power semiconductors are reduced and the ripple current at the output capacitor is also reduced. In each circuit module, two transformers are used to reduce the power rating of each magnetic core. The primary windings of the two transformers are connected in parallel and the secondary windings are connected in series in order to reduce and balance the current rating on each transformer. Thus the small size of the magnetic cores and reduced winding turns are adopted in each transformer. A full-wave diode rectifier is used in the high voltage side to clamp the voltage stress of the diodes at the output terminal voltage instead of at two times the output voltage as in a conventional center-tapped rectifier. The proposed converter can be used for low input voltage and high output voltage applications such as battery stack power conversion systems and renewable energy conversion systems. Finally experimental results are provided to verify the performance of the proposed converter.

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REFERENCES

[1] P. Das, B. Laan, S. A. Mousavi, and G. Moschopoulos, "A Nonisolated Bidirectional ZVS-PWM active clamped DC–DC converter," *IEEE Trans. Power Electron.*, Vol. 24, No. 2, pp. 553-558, 2009.

[2] I.-D. Kim, J.-Y. Kim, E.-C. Nho, and H.-G. Kim, "Analysis and design of a soft-switched PWM sepic DC-DC converter," *Journal of Power Electron.*, Vol. 10, No. 5, pp. 461-467, Sep. 2010.

[3] B.-R. Lin, H.-K. Chiang, and C.-Y. Cheng, "Interleaved DC-DC converters with partial ripple current cancellation," *Journal of Power Electronics*, Vol. 12, No. 2, pp. 249-257, Mar. 2012.

[4] B. R. Lin and J. Y. Dong, "Analysis and implementation of an active clamping zero-voltage turn-on switching /zero-current turn-off switching converter," *IET Proc. - Power Electron.*, Vol. 3, No. 3, pp. 429-437, 2010.

[5] J.-H. Kim, Y.-C. Jung, S.-W. Lee, T.-W. Lee, and C.-Y. Won, "Power loss analysis of interleaved soft switching boost converter for single-phase PV-PCS," *Journal of Power Electron.*, Vol. 10, No. 4, pp. 335-341, Jul. 2010.

[6] B.-R. Lin and C.-H. Tseng, "Analysis of parallel-connected asymmetrical soft-switching converter," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 3, pp. 1642-1653, Jun. 2008.

[7] J. C. P. Liu, N. K. Poon, B. M. H. Pong, and C. K. Tse, "Low output ripple dc-dc converter based on an overlapping dual asymmetric half-bridge topology," *IEEE Trans. Power Electron.*, Vol. 22, No. 5, pp. 1956-1963, Sep. 2007.

[8] G. B. Koo, G. W. Moon, and M. J. Youn, "New zero-voltage-switching phase-shift full-bridge converter with low conduction losses," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 1, pp. 228-235, Feb. 2005.

[9] H.-J. Chiu, Y.-K. Lo, T.-P. Lee, C.-C. Chuang, and S.-C. Mou, "A single-stage phase-shifted full-bridge AC/DC converter with variable frequency control," *International Journal of Circuit Theory and Applications*, Vol. 38, No. 8, pp. 867-879, 2010.

[10] S.-S. Hong, S.-K. Ji, Y.-J. Jung and C.-W. Roh, "analysis and design of a high voltage flyback converter with resonant

elements," *Journal of Power Electron.*, Vol. 10, No. 2, pp. 107-114, Mar. 2010.
[11] A. K. S. Bhat, "Analysis and design of a modified series resonant converter," *IEEE Trans. Power Electron.*, Vol. 8, No. 5, pp. 423-430, Oct. 1993.
[12] M. K. Kazimierczuk and N. Thirunarayan, "Class D voltage-switching inverter with tapped resonant inductor," *IEE Proc. - Electric Power Applications*, Vol. 140, No. 3, pp. 177-185, 1993.
[13] D. Czarkowski and M. K. Kazimierczuk, "Phase-controlled CLL resonant converter," in *Proc. IEEE Applied Power Electronics Conference*, pp. 432-438, 1993.
[14] M. K. Kazimierczuk, "Synthesis of phase-modulated dc/ac inverters and dc/dc converters," *IEE Proc. - Electric Power Applications*, Vol. 139, No. 4, pp. 387-394, 1992.
[15] M. K. Kazimierczuk and D. Czarkowski, *Resonant Power Converters*, Chap. 9 and 18, John Wiley & Sons, 2011.
[16] Y. Gu, Z. Lu, L. Hang, Z. Qian, and G. Huang, "Three-level LLC series resonant DC/DC converter," *IEEE Trans. Power Electron.*, Vol. 20, No. pp. 781-789,Jul. 2005;
[17] K. Jin, and X. Ruan, "Hybrid full-bridge three-level LLC resonant converter - A novel dc-dc converter suitable for fuel-cell power system," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 5, pp. 1492-1503, Oct. 2006.
[18] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 5, pp. 1321-1329, May 2009.
[19] K. H. Yi and G. W. Moon, "Novel two-phase interleaved LLC series-resonant converter using a phase of the resonant capacitor," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 5, pp. 1815-1819, May 2009.

Bor-Ren Lin received his B.S. in Electronic Engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988, and his M.S. and Ph.D. in Electrical Engineering from the University of Missouri, USA, in 1990 and 1993, respectively. From 1991 to 1993, he was a Research Assistant with the Power Electronic Research Center, University of Missouri. Since 1993, he has been with the Department of Electrical Engineering, National Yunlin University of Science and Technology, Douliou, Taiwan, where he is currently a Professor. He has authored more than 200 published technical journal papers in the area of power electronics. His current research interests include power-factor correction, multilevel converters, active power filters, and soft-switching converters. Dr. Lin is an Associate Editor of the IEEE Transactions on Industrial Electronics, The Institution of Engineering and Technology Proceedings—Power Electronics and the Journal of Power Electronics. He was the recipient of Research Excellence Awards in 2004, 2005, 2007 and 2011 from the College of Engineering, National Yunlin University of Science and Technology. He received best paper awards from the IEEE Conference on Industrial Electronics and Applications 2007 and 2011, from the Taiwan Power Electronics 2007 Conference, and from the IEEE Power Electronics and Drive Systems 2009 Conference.

Sin-Jhih Shen received his M.S. in Electrical Engineering from the National Yunlin University of Science and Technology, Yunlin, Taiwan, in 2011. His current research interests include the design and analysis of power factor correction techniques, switching mode power supplies and soft switching converters.