JPE 12-4-4

http://dx.doi.org/10.6113/JPE.2012.12.4.548

Novel Single-State PWM Technique for Common-Mode Voltage Elimination in Multilevel Inverters

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Abstract

In this paper, a novel offset-based single-state pulse width modulation (PWM) method for achieving zero common-mode voltage (CMV) and reducing switching losses in multilevel inverters is presented. The specific active switching state of the zero common-mode (ZCM) voltage that approximates the reference voltage can be deduced from the switching state sequence of the reduced CMV phase disposition PWM (CMV PD PWM) method. From the reference leg voltages for the zero common-mode voltage, an N-to-2-level transformation defines a virtual two-level inverter and the corresponding nominal leg voltage references. The commutation process of the reduced CMV PD PWM method in a multilevel inverter and its outputs can be simply followed in a nominal switching time diagram for the virtual inverter. The characteristics of the reduced CMV PD PWM and the single-state PWM for zero common-mode voltage are analyzed in detail in this paper. The theoretical analysis of the proposed PWM method is verified by experimental results.

Key words: Eliminating common mode voltage, Multilevel inverter, Single-state PWM technique,

I. INTRODUCTION

The two most common multilevel inverter topologies are diode-clamped or neutral-point-clamped (NPC) inverters and cascaded inverters, as shown in Figs. 1 and 2. There are basically three PWM schemes for controlling multilevel inverters: carrier-based PWM, space vector PWM, and selective harmonics elimination (SHE) PWM [1][2]. Space vector modulation (SVPWM) has become one of the most popular PWM techniques for power converters. The simple PWM algorithm, its suitability for digital implementation, and the high performance of SVPWM for two-level inverters have drawn a significant amount of attention from many researchers. However, the advantages of multilevel inverters have been little explored to date. If the number of levels in a multilevel inverter is high, determining the switching states and calculating the dwelling times can be much more tedious than for a two-level inverter. While determining the location of the reference vector and the related pivot vectors in SVPWM methods is difficult, PWM implementation can be easily achieved using the carrier-based PWM (CPWM) method. When using this method, the inverter leg voltage is computed as the sum of the active voltage (the fundamental voltage) and the common-mode voltage. The availability of common-mode control in the leg voltage provides a high degree of flexibility when using the carrier-based PWM technique.

The common-mode voltages generated as a result of PWM switching are observed on the motor windings and are capacitive coupled to the motor shaft, leading to bearing currents [3]. The effect of the common-mode voltage on the bearing current of an AC motor is a reduction in the life expectancy of the motor [4]. In a multilevel inverter, there are a number of switching states for achieving ZCM voltage (Fig. 3).

Manuscript received Jul. 19, 2011; revised Mar. 22, 2012
Recommended for publication by Associate Editor Dong-Choon Lee.
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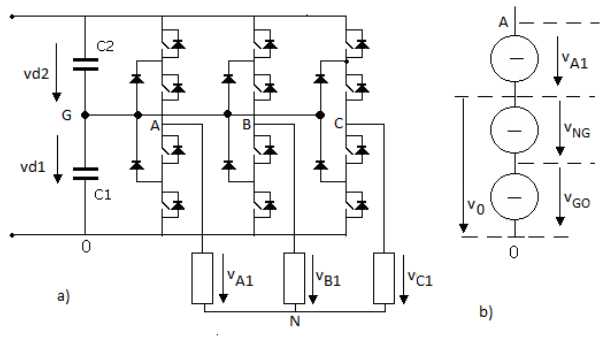

Fig. 1. (a) The three-level NPC inverter and (b) Equivalent circuit of the A-phase leg voltage.

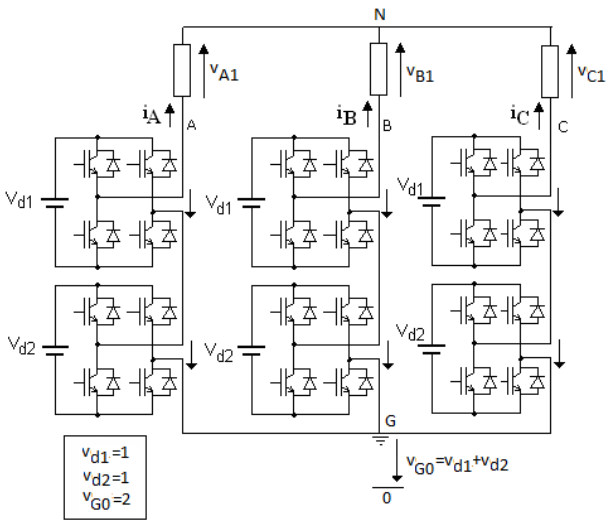

Fig. 2. Five-level cascaded inverter; "0" is a virtual potential.

For partial elimination of the CMV in PWM methods, the output voltage can be obtained by using the discontinuous PWM technique with a reduced-average common-mode voltage [5]-[9]. Researchers have also tried to achieve complete common-mode elimination in PWM methods [6], [10], [11]. These approaches require double commutations, which leads to increased switching loss. In the carrier-based approach [10], [11], using two modulating signals per phase caused twelve commutations per triangular carrier wave. A similar switching loss situation was found in research by P.C. Loh et al. [6].

This paper proposes a single-state PWM method with a ZCM voltage that produces only one zero CMV switching state during a switching state sequence.

Assumption: All voltage levels are described in units**.**

For the 3-level inverter shown in Fig. 1, the switching state vector is $\vec{S} = [S_A, S_B, S_C]^T = [2,1,0]^T$, which corresponds to the inverter output voltage levels at the voltage potential "0" of $v_{A0} = 2, v_{B0} = 1, v_{C0} = 0$. Similarly, for the 5-level

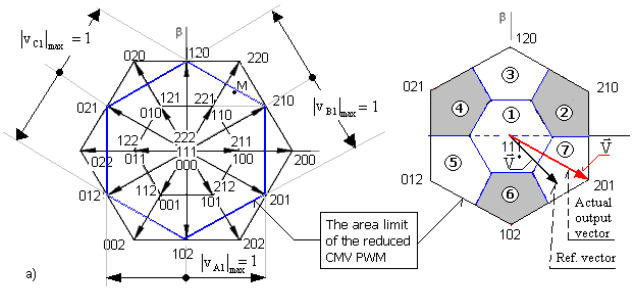

Fig. 3. Three-level inverter. (a) Vector diagram and limits under ZCM; b) vector diagram divided into seven sectors corresponding to the seven ZCM voltage vectors.

cascaded inverter in Fig. 2, the switching state vector $[4,2,1]^T$ corresponds to the inverter voltage levels at the potentials "0" and "G" of $v_{A0} = 4, v_{B0} = 2, v_{C0} = 1$ and $v_{AG} = 2, v_{BG} = 0, v_{CG} = -1$, respectively. In this paper, the inverter voltage levels are assumed to have no negative values, i.e., with levels at the potential "0," as shown in Figs.1 and 2.

II. Characteristics of The Proposed Single-State PWM Method for Eliminating Common Mode Voltage

A. Analysis of the Proposed Method

1) The offset for the zero average common mode voltage: Define the reference leg voltage v_X between the output X and the DC-neutral point "0," consisting of the fundamental voltages v_{X1} and the offset v_0 (see Fig.1) as follows:

$$\begin{cases} v_{A1} = v_m \cos\theta; \\ v_{B1} = v_m \cos(\theta - 2\pi/3) \\ v_{C1} = v_m \cos(\theta - 4\pi/3 \end{cases} \quad (1)$$

$$v_X = v_{X1} + v_0 \quad ,X=A,B,C \quad (2)$$

where v_m is the amplitude and θ is the phase angle.

The offset for the reduced CMV PWM method is defined for the zero average value of the common mode voltage as follows, with n being the number of levels:

$$v_{NG} = 0 \quad (3)$$

$$v_0 = (n-1)/2 \quad (4)$$

2) Two-step algorithm to attain the output switching state: The output switching state of the proposed method is not obtained

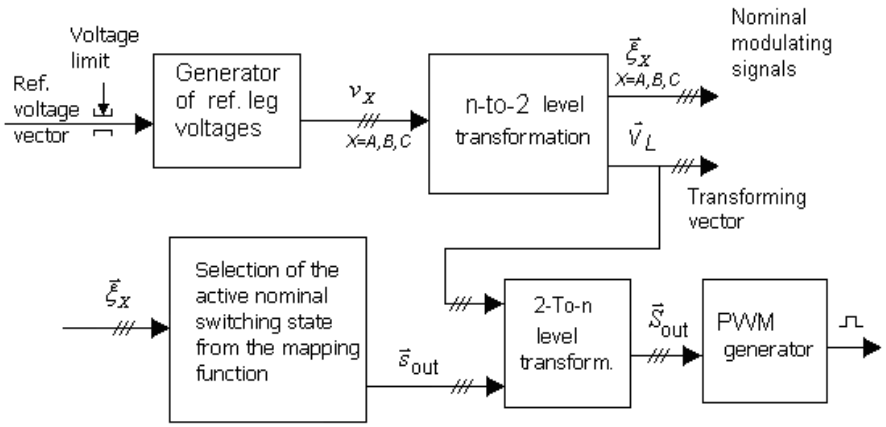

Fig. 4. The proposed single-state PWM scheme for eliminating common-mode voltage.

directly. It is deduced from the resulting switching state sequence of the conventional reduced CMV PD PWM method defined by (4). As a result, it selects the only switching state with zero CMV. From that consideration, the output voltages of the proposed method can be produced in a two-step PWM algorithm as follows.

Step 1: Four switching states $\vec{S}_1, \vec{S}_2, \vec{S}_3, \vec{S}_4$ are deduced in the reduced CMV PD PWM algorithm. A PD PWM algorithm helps to involve the nearest vectors to the reference vector.

Step 2: This step selects the switching state $\vec{S}_{out} = [S_A, S_B, S_C]^T$ corresponding to the zero CMV vector $\vec{V}$. It is satisfied by the following condition:

$$S_A + S_B + S_C = 3(n-1)/2 \tag{5}$$

3) The working area in the hexagonal diagram: It is necessary to determine the working area of a reference vector to satisfy (4) and cover all of the ZCM voltage vectors. For the reference vector, the offset (4) is valid if its limits are defined as:

$$v_{0\min} \le v_0 \le v_{0\max} \ , \tag{6}$$

or in detail:

$$-\mathrm{MIN} \le \frac{n-1}{2} \le (n-1) - \mathrm{MAX} \ , \tag{7}$$

where MAX and MIN are defined as the maximum and minimum functions of (1), as follows:

$$MAX = Max(v_{A1}, v_{B1}, v_{C1}) \tag{8}$$

$$\mathrm{MIN} = \mathrm{Min}(v_{A1}, v_{B1}, v_{C1}) \tag{9}$$

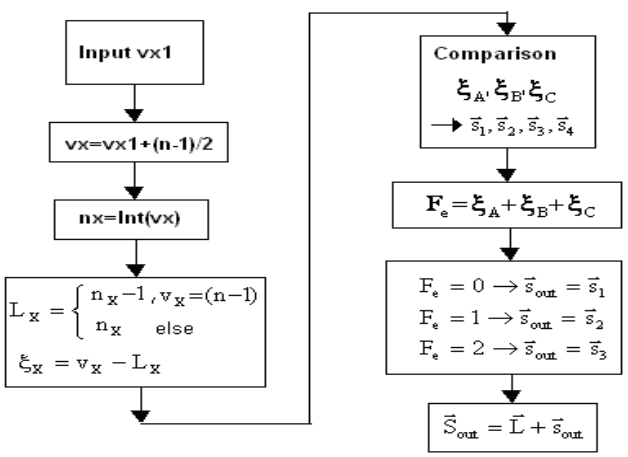

Fig. 5. PWM algorithm for the proposed ZCM voltage PWM, X=A, B, C.

⊕ The inequality on the right side (7) yields:

$$\mathrm{MAX} \le (n-1)/2 \tag{10}$$

⊕ The inequality on the left side (7) yields:

$$\mathrm{MIN} \ge -(n-1)/2 \, . \tag{11}$$

As a result, the instantaneous phase voltage value of the effective voltage vector for the average ZCM voltage must be set within the limits given by that phase voltage. For example, the A-phase voltage limits are $|v_{A1}| \le (n-1)/2$. Condition (4) and the derived limits (10) and (11) define a working area for the proposed PWM method. The vector diagram limits of the three-level inverter are drawn in Fig. 3. Note that each switching state sequence of the reduced CMV PWM in the working area always involves a vector of zero CMV.

B. Implementing PWM Scheme

Based on the above analysis, the proposed PWM method can be implemented. Its block scheme and corresponding algorithm are shown in Figs.4 and 5. A similar PWM scheme without eliminating the common mode voltage was developed in [13].

An N-to-2-level inverter transformation block appears in the scheme to ease the two-step algorithm described in section II.A. It defines the nominal modulating signals and the transforming vector. These nominal signals are compared, as shown in Table I, in order to determine the four switching states in a nominal switching state sequence, from which the output voltage vector will be selected.

1) Description of N-to-2-level inverter transformation and generation of nominal switching state sequence for the reduced CMV PWM algorithm: For the reference leg voltage, $\mathrm{v_X}$, a subsequent change between the two closest active levels, $\mathrm{L_X}$ and $\mathrm{H_X}$, will be generated at the corresponding inverter output. Their functions can be determined as follows:

$$L_X = \begin{cases} n_X & if \quad 0 \le v_X < (n-1) \\ n_X - 1 & if \quad v_X = (n-1) \end{cases} \tag{12}$$

$$H_X = L_X + 1 \tag{13}$$

$$\text{where } \mathrm{n_X = Int(v_X)}; X = A, B, C. \tag{14}$$

The N-to-two-level inverter transformation concentrates consideration to a smaller hexagonal vector diagram. As a result, it helps to ease the selection process. Instead of considering voltage levels compared to the potential "0," it considers voltage levels relative to the vector $\vec{\mathrm{L}} = [\mathrm{L_A}, \mathrm{L_B}, \mathrm{L_C}]^{\mathrm{T}}$. The vector $\vec{L}$ is a transforming vector and the first vector in a switching sequence. It is located at the center of the vector diagram of the corresponding virtual two-level inverter.

The reference voltages for each of the virtual inverters are defined as nominal references, and they are expressed as follows (see Fig.6):

$$\xi_{\mathrm{X}} = \mathrm{v_X} - \mathrm{L_X}; 0 \le \xi_{\mathrm{X}} \le 1. \tag{15}$$

The max, mid, and min functions are defined as the maximum, medium, and minimum values from the three variables, $\xi_{\mathrm{a}}, \xi_{\mathrm{b}}, \xi_{\mathrm{c}}$, as follows:

$$\max = Max(\xi_A, \xi_B, \xi_C) \tag{16}$$

$$mid = Mid(\xi_A, \xi_B, \xi_C); \tag{17}$$

$$\min = Min(\xi_A, \xi_B, \xi_C). \tag{18}$$

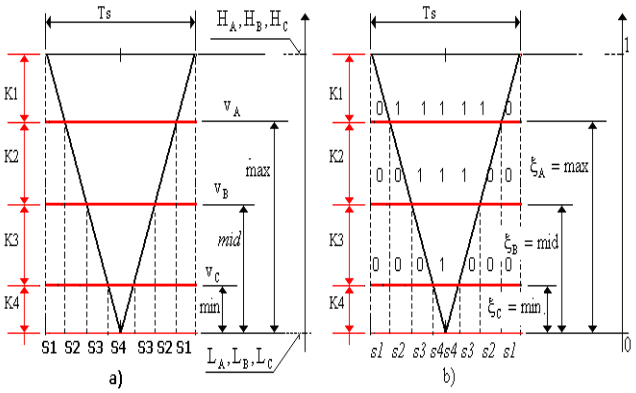

Fig. 6. Carrier PD PWM method for a multilevel inverter: (a) switching time diagram; (b) nominal switching time diagram and nominal switching state sequence under the conditions $\xi_A > \xi_B > \xi_C$.

TABLE I

NOMINAL SWITCHING STATE SEQUENCE IN THE PD PWM TECHNIQUE

The mapping function $[\xi_A, \xi_B, \xi_C]^T =$	Nominal switching state sequence $(\vec{\mathrm{s}}_1 \rightarrow \vec{\mathrm{s}}_2 \rightarrow \vec{\mathrm{s}}_3 \rightarrow \vec{\mathrm{s}}_4)$
$[\max, \mathrm{mid}, \min]^{\mathrm{T}}$	$[0,0,0]^{\mathrm{T}} \rightarrow [1,0,0]^{\mathrm{T}} \rightarrow [1,1,0]^{\mathrm{T}} \rightarrow [1,1,1]^{\mathrm{T}}$
$[\max, \min, \mathrm{mid}]^{\mathrm{T}}$	$[0,0,0]^{\mathrm{T}} \rightarrow [1,0,0]^{\mathrm{T}} \rightarrow [1,0,1]^{\mathrm{T}} \rightarrow [1,1,1]^{\mathrm{T}}$
$[\mathrm{mid}, \max, \min]^{\mathrm{T}}$	$[0,0,0]^{\mathrm{T}} \rightarrow [0,1,0]^{\mathrm{T}} \rightarrow [1,1,0]^{\mathrm{T}} \rightarrow [1,1,1]^{\mathrm{T}}$
$[\mathrm{mid}, \min, \max]^{\mathrm{T}}$	$[0,0,0]^{\mathrm{T}} \rightarrow [0,0,1]^{\mathrm{T}} \rightarrow [1,1,0]^{\mathrm{T}} \rightarrow [1,1,1]^{\mathrm{T}}$
$[\min, \max, \mathrm{mid}]^{\mathrm{T}}$	$[0,0,0]^{\mathrm{T}} \rightarrow [0,1,0]^{\mathrm{T}} \rightarrow [0,1,1]^{\mathrm{T}} \rightarrow [1,1,1]^{\mathrm{T}}$
$[\min, \mathrm{mid}, \max]^{\mathrm{T}}$	$[0,0,0]^{\mathrm{T}} \rightarrow [0,0,1]^{\mathrm{T}} \rightarrow [0,1,1]^{\mathrm{T}} \rightarrow [1,1,1]^{\mathrm{T}}$

The three nominal references (16)-(18) establish a reference vector for the corresponding virtual two-level inverter. Their comparison with the max, mid, and min functions produces a corresponding nominal switching state sequence $\vec{\mathrm{s}}_1, \vec{\mathrm{s}}_2, \vec{\mathrm{s}}_3, \vec{\mathrm{s}}_4$, as shown in Fig. 6b and Table 1. The benefit of the previous transformation that time duties of the nominal switching state $\vec{s}_K$ in Fig.6b is the same as that of the switching state $\vec{S}_K$ in Fig.6a, and the switching state sequence $\vec{S}_K$ can be regained from the nominal switching state $\vec{s}_K$ by adding the vector $\vec{L}$ to it.

2) Derivation of the output voltage vector: From (12)-(15), the function $\mathrm{F_l}$ using vector $\vec{L}$ is defined as:

$$F_l = L_A + L_B + L_C . \quad (19)$$

Similarly, the extra function F_e is defined as follows:

$$F_e = \xi_A + \xi_B + \xi_C \ , \quad (20)$$

where $\vec{\xi} = [\xi_A, \xi_B, \xi_C]^T$ is the nominal voltage vector.

The CMV function of a reference voltage vector is defined as the sum of the leg voltage components. From (1)-(4), the reference voltage $\vec{V}^*$ in the reduced CMV PWM method can be expressed as:

$$F_{CM}(\vec{V}^*) = v_A + v_B + v_C = F_l + F_e = 3(n-1)/2 \quad (21)$$

Since $0 \le \xi_X \le 1$, then $0 \le F_e \le 3$. From (20), (21), and Table 1, it can be seen that there are three possible cases that may occur in the reduced CMV PWM method. From these, one switching state from the sequence in Table 1 will be selected to produce the output switching state described in Table 2. Notice that the condition $F_l = 3(n-1)/2 - 3$ does not exist, so it is excluded (see Appendix 1).

The proposed scheme depicted in Figs. 4 and 5 is advantageous due to the following characteristics.

(*) Simplicity of implementation: The main operator is making the comparisons, thus there is no need for a coordinate transformation or a look-up table.

(**) General applicability: The proposed PWM algorithm is applicable to any number of levels.

3) Examples for 3-level inverters: Example 1: The PWM control of a three-level NPC inverter (n=3) can be analyzed as a control for one of eight virtual two-level inverters. For each of the virtual two-level inverters, the three phase voltages generated from the switching combinations upon a set of three active DC voltages form a small hexagonal vector diagram. This hexagonal diagram centers at the vector $\vec{L}$. There are three virtual inverters centered at the transforming vectors of $[1,0,0]^T$, $[0,0,1]^T$, and $[0,1,0]^T$ to satisfy the condition (26) of $F_l = 1$. Three other virtual inverters center at the transforming vectors of $[0,1,1]^T$, $[1,1,0]^T$, and $[1,0,1]^T$ to satisfy the condition (24) of $F_l = 2$. There is only one virtual inverter centered at $[1,1,1]^T$ to satisfy the condition (22) of $F_l = 3$, as shown in Fig. 3a. This particular case occurs if the reference vector $\vec{V}^*$ is equal to a ZCM voltage vector.

Example 2: The three fundamental voltages are $v_{A1} = 0.707$; $v_{B1} = 0.258$; and $v_{C1} = -0.965$. The offset for the ZCM and the corresponding leg voltages are derived as $v_0 = 1$; $v_A = 1.707$; $v_B = 1.258$; and $v_C = 0.035$.

These corresponding leg voltages also define the transforming vector $\vec{L} = [1,1,0]^T$. With the help of the transforming vector $\vec{L} = [1,1,0]^T$, the three nominal leg voltages of the virtual two-level inverter can be calculated as $\xi_A = 0.707; \xi_B = 0.258; \xi_C = 0.035$. Because $F_e = 1$ and $\xi_A > \xi_B > \xi_C$, by applying (24) and the first row in Table 1, the actual switching state produced by a single-state PWM modulator is $\vec{S}_{out} = [1,1,0]^T + [1,0,0]^T = [2,1,0]^T$.

TABLE II

GENERATING THE OUTPUT ZERO CMV VECTOR

Conditions of the reference voltage $\vec{V}^*$ for the reduced CMV PWM method	The active switching-state of the single state PWM method to eliminate CMV
$F_l = 3(n-1)/2$ (22)	$\vec{s}_{out} = \vec{s}_1$ (23)
$F_l = 3(n-1)/2 - 1$ (24)	$\vec{s}_{out} = \vec{s}_2$ (25)
$F_l = 3(n-1)/2 - 2$ (26)	$\vec{s}_{out} = \vec{s}_3$ (27)
Switching state output	$\vec{S}_{out} = \vec{L} + \vec{s}_{out}$ (28)

III. UNDER- AND OVERMODULATION

In order to set up the operating range of the output voltages and control characteristics, the active voltage for the whole operating range must be determined, including that for overmodulation. This can be done by using principal control between the two limit trajectories [14].

From the vector diagram, the operating range of the active voltages can be divided into three ranges as follows.

A. Undermodulation

The active vector $\vec{v}_1$ is located inside a circle inscribed in the medium hexagon. The radius of this limit circle can be easily determined as $v_S/2$, i.e., $m = 0.866$. The fundamental voltages are defined as (3) with:

$$v_m = v_S / 2 \quad (29)$$

B. Overmodulation mode 1

The vector $\vec{v}_1$ moves along the boundary of the medium hexagon. There are variations in the design of the outer voltage trajectory for overmodulation mode 1. One variation can be defined by algorithm (31). The corresponding amplitude of the fundamental voltages can be determined as:

$$v_{1m} = 0.911 \times v_s / \sqrt{3} \quad (\text{i.e., } m = 0.911). \tag{30}$$

The leg voltages for a modulation index of m=0.911 can be calculated as:

$$v_{A,0.911} = \begin{cases} (n-1) & \text{if } \begin{cases} 0 \le \theta < \pi/6 \\ 11\pi/6 \le \theta < 2\pi \end{cases} \\ -\dfrac{(n-1)(\theta-\pi/6)}{2\pi/3} + (n-1) & \text{if } \pi/6 \le \theta < 5\pi/6 \\ 0 & \text{if } 5\pi/6 \le \theta < 7\pi/6 \\ \dfrac{(n-1)(\theta-7\pi/6)}{2\pi/3} & \text{if } 7\pi/6 \le \theta < 11\pi/6 \end{cases} \tag{31a}$$

$$v_{B,0.911} = \begin{cases} (n-1) & \text{if } 3\pi/6 \le \theta < 5\pi/6 \\ -\dfrac{(n-1)(\theta-5\pi/6)}{2\pi/3} + (n-1) & \text{if } 5\pi/6 \le \theta < 9\pi/6 \\ \dfrac{(n-1)(\theta-11\pi/6)}{2\pi/3} & \text{if } 11\pi/6 \le \theta < 2\pi \\ \dfrac{(n-1)(\theta+\pi/6)}{2\pi/3} & \text{if } 0 \le \theta < 3\pi/6 \\ 0 & \text{if else} \end{cases} \tag{31b}$$

$$v_{B,0.911} = \begin{cases} (n-1) & \text{if } 7\pi/6 \le \theta < 9\pi/6 \\ -\dfrac{(n-1)(\theta+3\pi/6)}{2\pi/3} + (n-1) & \text{if } 0 \le \theta < \pi/6 \\ -\dfrac{(n-1)(\theta-9\pi/6)}{2\pi/3} + (n-1) & \text{if } 9\pi/6 \le \theta < 2\pi \\ \dfrac{(n-1)(\theta-3\pi/6)}{2\pi/3} & \text{if } 3\pi/6 \le \theta < 7\pi/6 \\ 0 & \text{if else} \end{cases} \tag{31c}$$

C. Overmodulation mode 2

The outer trajectory consists of the six discrete vectors located at the pivots of the medium hexagon. The reference vector $\vec{v}_1$ holds constantly at each location for one-sixth of the fundamental period before jumping abruptly to the following vector. This operation produces a six-step voltage, which attains the fundamental amplitude

$$v_{1m} = \sqrt{3} v_s / \pi \quad (\text{i.e. } m = 0.955). \tag{32}$$

Consider only the 1st fundamental period. The leg voltages v_{X1}, where $X = A, B, C$ for m=0.955, can be deduced as follows:

$$v_{A,0.955} = \begin{cases} (n-1) & \text{if } 0 \le \theta < \pi/3 \wedge 5\pi/3 \le \theta < 2\pi \\ 0.5(n-1) & \text{if } \pi/3 \le \theta < 2\pi/3 \wedge 4\pi/3 \le \theta < 5\pi/3 \\ 0 & \text{if } 2\pi/3 \le \theta < 4\pi/3. \end{cases} \tag{33a}$$

$$v_{B,0.955} = \begin{cases} (n-1) & \text{if } \pi/3 \le \theta < \pi/2 \\ 0.5(n-1) & \text{if } 0 \le \theta < \pi/3 \wedge \pi/2 \le \theta < 4\pi/3 \\ 0 & \text{if } 4\pi/3 \le \theta < 2\pi. \end{cases} \tag{33b}$$

$$v_{C,0.955} = \begin{cases} (n-1) & \text{if } \pi/2 \le \theta < 5\pi/3 \\ 0.5(n-1) & \text{if } 2\pi/3 \le \theta < \pi/2 \wedge 5\pi/3 \le \theta < 2\pi \\ 0 & \text{if } 0 \le \theta < 2\pi/3. \end{cases} \tag{33c}$$

To attain ZCM, the reference leg voltages v_X that correspond to the modulation index *m* in overmodulation can be expressed as:

$$\begin{aligned} v_X &= v_0 + (1-\eta) v_{X1,mA} + \eta v_{X1,mB} \\ &= (1-\eta) v_{X,mA} + \eta v_{X,mB} \end{aligned}, \tag{34}$$

where $v_{X1,mA}$ and $v_{X1,mB}$ are the leg voltages corresponding to the two limit-modulation indexes of m_A and m_B, where $m_A < m < m_B$ and

$$\eta = (m - m_A)/(m_B - m_A). \tag{35}$$

Diagrams of the leg voltages of the five-level inverter for three limit-modulation indexes are shown in Fig. 7. To have a complete set of limit trajectories, the reference voltages for the zero modulation index, which are equal to the offset function, will be added, and are described as follows:

$$v_{X,m=0} = (n-1)/2 \tag{36}$$

Deduction of the reference leg voltage for the whole operating range of the output voltage at m=0.955 can be followed in Fig. 8. These reference voltages are then used to generate the trigger pulse for the switching devices.

IV. Harmonics And Control Characteristics of Single-State PWM Method to Eliminate Common Mode Voltage

A. The control characteristics and THD factor

The PWM performance of the single-state PWM method with a reduced common-mode voltage was presented and discussed in [12]. The characteristics of 7-, 9-, 11- and 31-level inverters have been computed and are shown in Fig. 9. The fundamental frequency used in all of the analysis for this paper is selected as 50 Hz.

The nonlinearity that exists in 7-, 9-, and 11-level inverters is nearly removed in the 31-level inverter, providing approximate linearity for the entire range of modulation indexes from 0.07 to 0.955, including the overmodulation range. The harmonic content also has the advantages of a

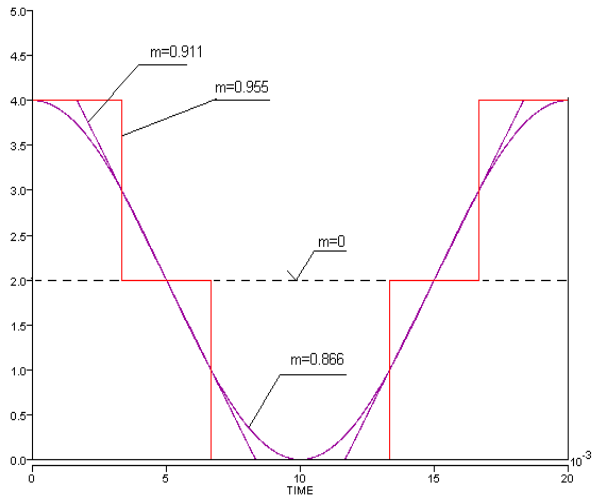

Fig. 7. Five-level inverter; PWM with ZCM, and reference leg voltages for modulation indexes of 0, 0.866, 0.911, and 0.955.

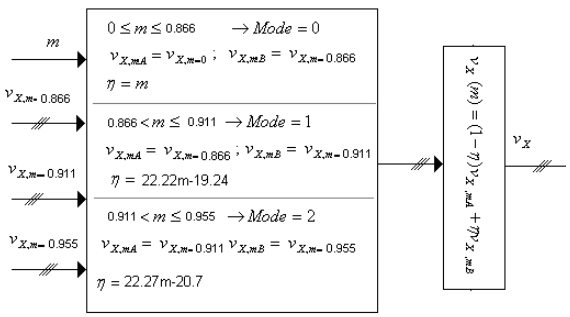

Fig. 8. Generator of the leg voltages.

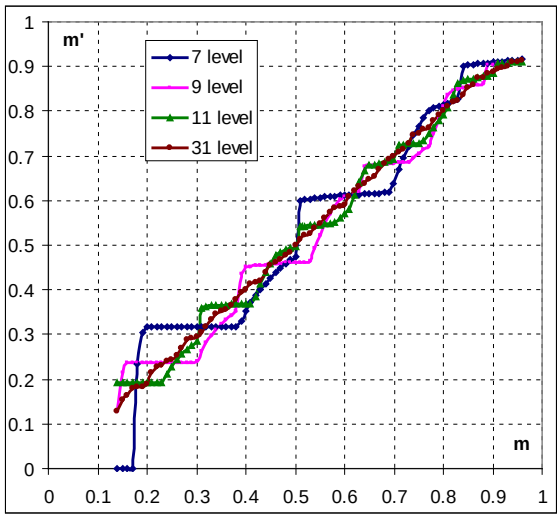

Fig. 9. Control characteristic of a 7, 9, 11 and 31-level inverter.

higher number of levels, as shown in Fig.10. For the 31-level inverter, for m > 0.3, the amplitudes of most of the lower-order harmonics are significantly reduced to below 3% of the fundamental. For m > 0.18, the amplitudes of the 5th and 7th harmonics are below 5%, and the total harmonic distortion factor (THD) is less than 8%. In order to reduce the THD factor below this limit, the modulation index in an 11-level inverter should be confined to the narrow range of m > 0.84, as deduced from the diagram in Fig. 10.

B. The switching losses

The reduction of the switching loss in the proposed method can be explained by the reference voltage, located in area 7 of Fig. 3b. In the vicinity of sub-area 7, there are the four closest voltage vectors of zero CMV: $[2,1,0]^T$, $[1,1,1]^T$, $[1,0,2]^T$ and $[2,0,1]^T$. It can be proven easily that an arbitrary vector located in sub-area 7 is nearer to the vector $[2,0,1]^T$ than it is to the other three vectors. Thus, the vector $[2,0,1]^T$ is selected as the actual output vector for any reference vector in area 7. In other words, there are no commutations while the reference voltage moves in that sub-area.

The double switching pattern of a conventional PWM technique to fully eliminate CMV [6] required twelve switching for each sampling period. In contrast, in the proposed method, a double commutation may occur only if the reference vector moves across the sub-area border. The larger the sub-area, the lower the amount of switching in the fundamental period. This causes a higher THD factor and nonlinearity of the beneficial reduction in switching loss. These characteristics depend on the number of levels of the inverter circuit and the modulation index.

For n=31, a step pulse waveform of the output voltage of the proposed PWM method introduces a low amount of switching losses. A high output voltage can approximate a sinusoidal waveform. Under these circumstances, the single-state PWM could be more advantageous than the multi-commutation PWM method [6], as explained in the following.

In Table III, the THD factor and the amount of switching per fundamental period were computed in order to compare the sinusoidal PWM method (N1, THD1) with the proposed method (N2,THD2) for a 31-level inverter. The reference modulation index is considered as a parameter. The switching frequency f_{SW} of the sinusoidal PWM technique was selected so that the amount of switching in each fundamental period will be approximately that of the proposed method. For example, at a modulation index m=0.8, the single-state PWM has the same amount of switching losses, but it has a lower THD factor (3.16% versus 3.86%) when compared to the sinusoidal PWM method with a carrier frequency of 1200 Hz. Since the sinusoidal PWM technique is principally better in terms of both the THD factor and the switching losses when compared to the eliminating-CMV PWM technique, a better THD performance is expected from the proposed method [6] than from the considered inverter.

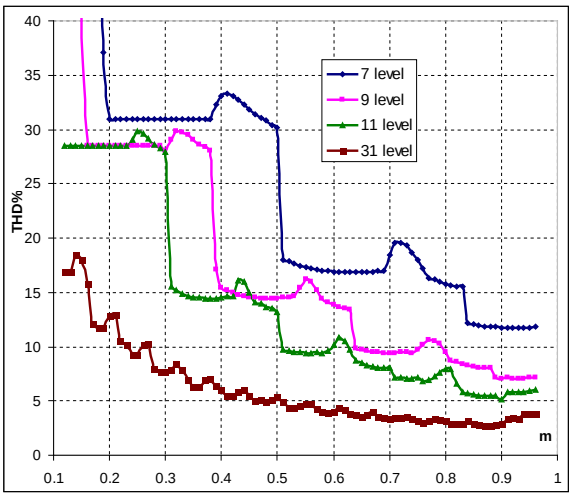

Fig. 10. THD diagram of a 7, 9, 11 and 31-level inverter computed for harmonics up to 51st order.

TABLE III

COMPARISON BETWEEN THE SINUSOIDAL PWM AND SINGLE-STATE ZCM PWM METHODS

m	0.1	0.2	0.3	0.4	0.5
f_{SW} [Hz]	400 (300)	400	400	400 (500)	1000 (900)
N1 [-]	20(16)	16	22	26(30)	48(46)
THD1 [%]	35.41 (37.34)	15.94	9.57	7.03 (7.79)	6.37 (6.09)
N2	16	16	20	28	46
THD2 [%]	30	12.9	7.71	5.97	5.38
m	0.6	0.7	0.8		
f_{SW} [Hz]	900	1100	1200		
N1 [-]	48	56	64		
THD1 [%]	4.56	4.25	3.86		
N2	48	56	64		
THD2 [%]	4.01	3.37	3.16		

For low-level (up to n=5) multilevel inverters, high THD factors and nonlinear control characteristics can prevent the proposed method from being useful in practical applications. However, the single-state CMV-eliminating PWM method for 7- and 9-level inverters has a THD factor that is less than 10% for a modulation index higher than 0.64, as shown in Fig. 10. One approach that can be usefully considered is a hybrid modulation which combines the single-state PWM method to reduce switching loss in the higher modulation index range with another method to improve the THD factor in the lower modulation index range. In electric motor control, the proposed PWM method can be considered for application in a Direct Torque Control drive system, where a single output voltage vector is produced with an error from the reference. However, these problems are beyond the scope of the current study.

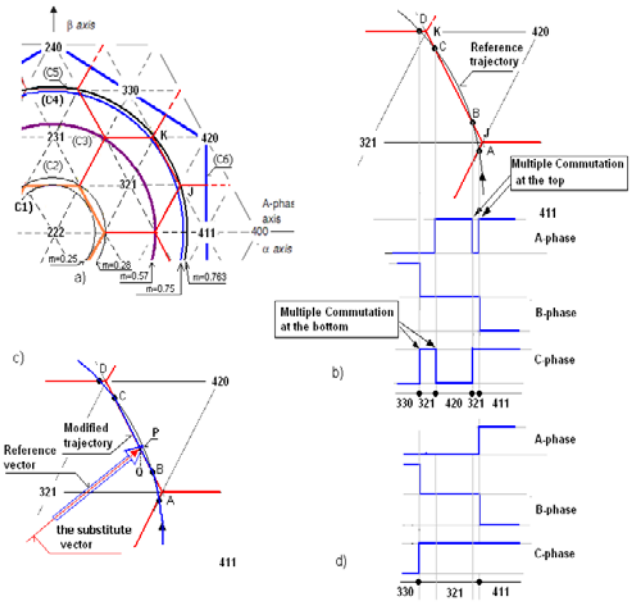

Fig. 11. Five-level inverter. (a) Voltage vector diagram with the ZCM voltage vectors; (b) Existing multiple commutations; (c) curve BC is replaced by the straight line BC in the modified technique; (d) without the multiple commutations .

V. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, two circuits were built: a five-level cascaded inverter and a 31-level hybrid cascaded inverter. In the cascaded five-level inverter, shown in Fig. 2(b), each phase consisted of two H-bridge single-phase inverters and was supplied by a 75 VDC source. In the hybrid cascaded 31-level inverter, four single-phase H-bridge inverters were connected in series for each phase. Their related DC voltages were set to 10V, 20V, 40V, or 80V.

The hardware was built using IGBTs FG60N100BNTD H20, and the dead-time was set by the hardware to be 3 μ S. The driver was designed with a photo-couple PC123. The parameters of the RL load were R=10 Ω and L=30 mH. The measuring equipment used was a Tektronix TDS2014b. The PWM algorithm was implemented with the use of the control kit, eZdsp TMS320F2812, with CCS studio V3.1 software. The experiments were implemented with an output frequency of 50 Hz.

A. Case of a 5-level inverter

There were five particular reference modulation indexes of 0.25, 0.288, 0.577, 0.75, and 0.763. Their circular trajectories correspond to the curves C1 through C5 in Fig. 11a. All of the voltages that have modulation indexes within close limits have similar waveforms. To demonstrate this, the output voltage m=0.7 is presented in Fig. 12. Multiple commutations are shown at the top and bottom of the voltage waveform.

This situation occurred only at some angle intervals and for a narrow modulation index range (i.e., between 0.75 and 0.763, as shown in Fig. 11a for a five-level inverter). This observation can be clarified with use of the phase voltage diagram for m=0.76, shown in Fig. 13. The reference vector moves across the sectors at A, B, C, and D.

The intersections at these points produce multiple commutations in the A phase and the C phase, as shown in Fig. 11b. The increase in the amount of switching stresses in sector JK caused by inserting the switching state $[420]^T$ between the two switching states $[321]^T$ can be avoided by using a "dropping pulse" technique. If the reference vector moves on curve BC, this trajectory will be replaced with the corresponding straight line BC (Fig. 11c). For example, the reference vector $\vec{P}$ will be replaced by the reference vector $\vec{Q}$. As a result, the switching state $[420]^T$ that appears in the time diagram in Fig. 11c is ejected, and the multiple switching is removed, as shown in Fig. 11d. For a high number of levels, this modification is acceptable. For example, in Fig. 11c, the errors between the reference $\vec{P}$ for the vectors $[420]^T$ (the original implementing vector) and $[321]^T$ (the substitute implementing vector) are nearly the same.

B. Case of 31-level inverter

Diagrams of the three-phase currents were generated, and the phase leg and common-mode voltages were measured. The diagrams for the undermodulation mode with m=0.7 are shown in Figs. 14-15, those for overmodulation mode 1 with m=0.911 are shown in Figs. 16-17, and the diagrams for overmodulation mode 2 with m=0.93 are shown in Figs. 18-19. The close sinusoidal voltage waveform of the 31-level inverter (Fig. 15), when compared with that of the 5-level inverter (Fig. 12), shows the benefit of the proposed method for multilevel inverters with a high number of levels.

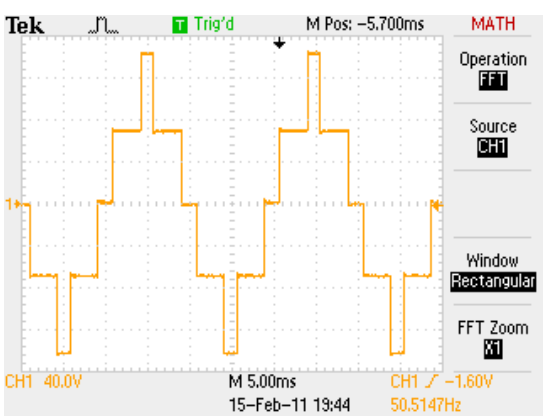

Fig. 12. Five-level inverter: Diagram of the A-phase voltage v_{AN} [40V/Div] , [5ms/Div] for m=0.7.

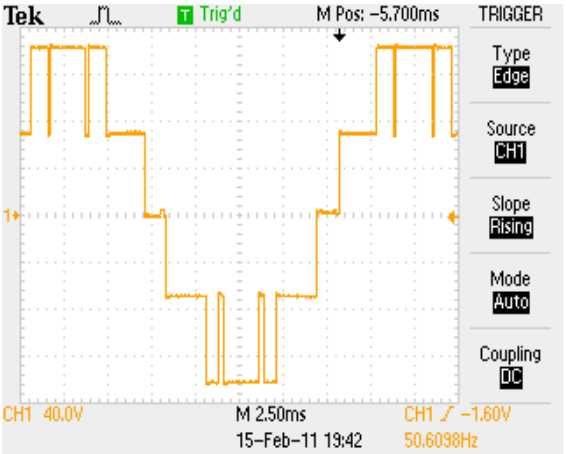

Fig. 13. Experimental results for the five-level inverter: Diagram of the A-phase voltage v_{AN} [40V/Div], [2.5ms/Div] for m=0.76.

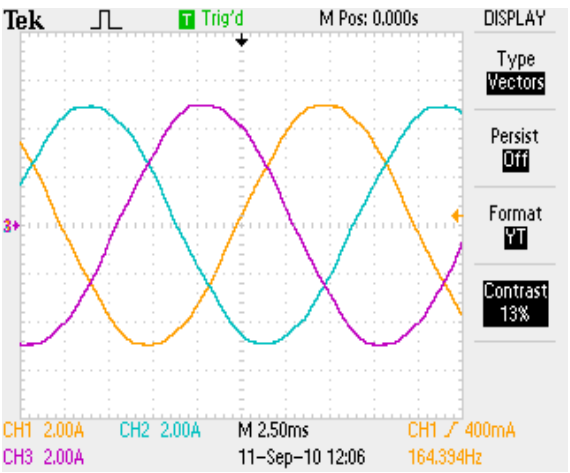

Fig. 14. Experimental results for the 31-level inverter in undermodulation mode (m=0.7): Diagrams of the three-phase load currents i_A, i_B, i_C [2A/Div], [2.5ms/Div].

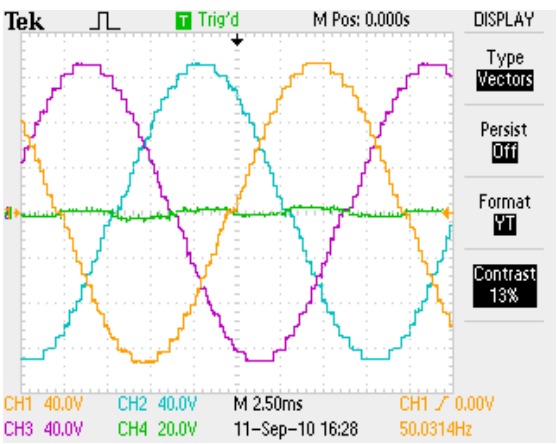

Fig. 15. Experimental results for the 31-level inverter in undermodulation mode (m=0.7): Diagram of 3f load voltages v_{AN}, v_{BN}, v_{CN} [40V/Div], [5ms/Div] and the common-mode voltage v_{NG} [20V/Div].

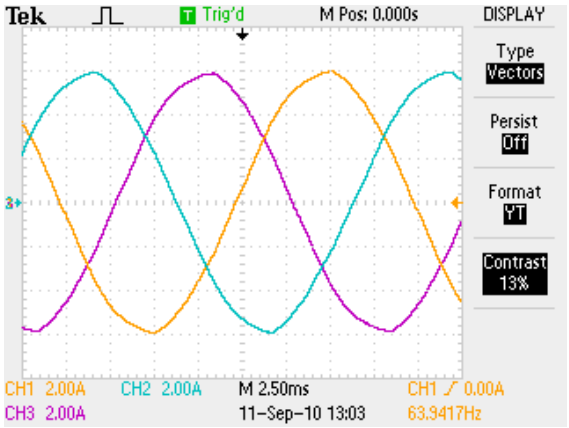

Fig. 16. Experimental results for the 31-level inverter in overmodulation mode 1 (m=0.911): Diagrams of the three-phase load currents i_A, i_B, i_C [2A/Div], [2.5ms/Div].

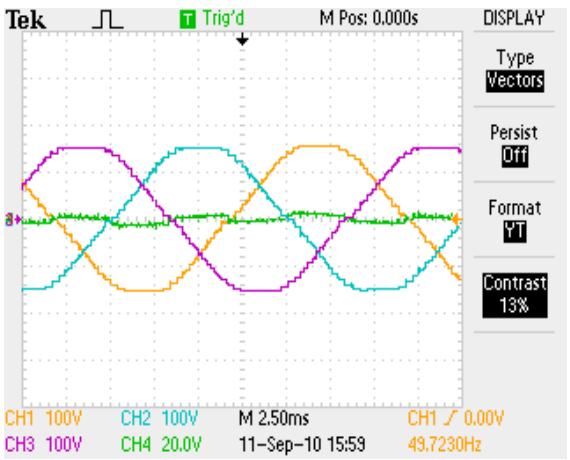

Fig. 17. Experimental results for the 31-level inverter in overmodulation mode 1 (m=0.911): Diagram of 3f load voltages v_{AN}, v_{BN}, v_{CN} [100V/Div], [2.5ms/Div], and the common-mode voltage v_{NG} [20V/Div] , [5ms/Div].

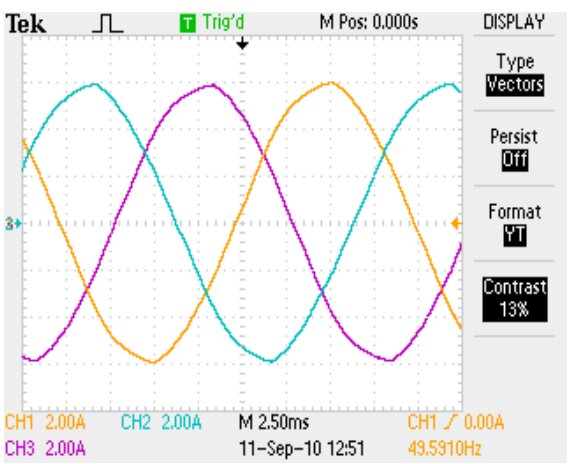

Fig. 18. Experimental results for the 31-level in overmodulation mode 2 (m=0.93): Diagrams of the three-phase load currents i_A, i_B, i_C [2A/Div], [2.5ms/Div].

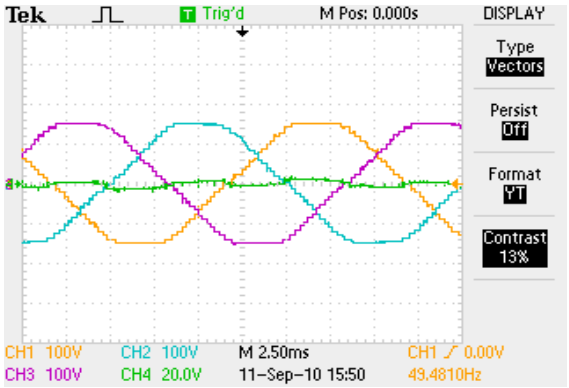

Fig. 19. Experimental results for the 31-level inverter in overmodulation mode 2 (m=0.93): Diagram of 3f load voltages v_{AN}, v_{BN}, v_{CN} [100V/Div], [2.5ms/Div], and the common-mode voltage v_{NG} [20V/Div].

VI. CONCLUSIONS

A novel offset-based single-state PWM technique for eliminating common-mode voltage has been presented in this paper. The offset variable can be set to define a virtual two-level inverter with corresponding nominal references in order to obtain a voltage vector with a zero common-mode voltage. The proposed PWM method utilizes the correlation between carrier-based PWM and space vector PWM to select the ZCM voltage vector nearest to the reference.

The proposed method produces an approximate vector and is suitable for applications in high-level inverters. This was demonstrated by the control characteristics and THD diagrams. The theoretical analysis was verified by experimental results for 5- and 31-level cascaded inverters.

APPENDIX

Assume $F_e = 3$. This assumption requires that $L_A = L_B = L_C = (n-2)$, and $F_l = 3(n-1)/2$. The vector $[n-2, n-2, n-2]^T$ located at the coordinate center has an amplitude of zero. However, by applying (12)-(14) to the zero vector, $F_l = 3(n-1)/2$ and $F_e = 0$. This result is inconsistent with the initial assumption. Therefore, $F_e = 3$ is not possible.

ACKNOWLEDGMENT

This research is funded by Vietnam National Foundation for Science and Technology Development (NAFOSTED) under grant number 103.06-2011.04 and supported (in part) by the Network based Automation Research Center (NARC) at University of Ulsan.

REFERENCES

[1] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, Vol. 7, No. 3, pp. 497-505, Jul. 1992.

[2] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 4, pp. 724-738, Aug. 2002.

[3] Fei Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage PWM voltage-source-inverter drive applications," *IEEE Trans. Ind. Appl.*, Vol. 36, No. 5, pp. 1336-1341, Sep./Oct. 2000.

[4] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Trans. Ind. Appl.*, Vol. 32, No. 5, pp. 1105-1114, Sep./Oct. 1996.

[5] H. Kim, H. Lee, and S. Sul, "A new PWM strategy for common mode voltage reduction in neutral-point-clamped inverter-fed AC motor drives," *IEEE Trans. Ind. Appl.*, Vol. 37, No. 6, pp. 1840-1845, Nov./Dec. 2001.

[6] P. C. Loh, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *IEEE Trans. Ind. Appl.*, Vol. 39, No. 5, pp. 1386-1395, Sep./Oct. 2003.

[7] M. M. Renge and H. M. Suryawanshi, "Three-dimensional space vector modulation to reduce common-mode voltage for multilevel inverter," *IEEE Trans. Ind. Electron.* Vol. 57, No. 7, pp. 2324-2331, Jul. 2010.

[8] A. K. Gupta,and A. M. Khambadkone, "Space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, Vol. 22, No. 5, pp.1672-2681, Sep. 2007.

[9] A. Videt, P. Le Moigne, N. Idir, P. Baudesson, and X. Cimetière, "A new carrier-based pwm providing common-mode-current reduction and dc-bus balancing for three-level inverters," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6, pp. 3001-3011, Dec. 2007.

[10] H. Zhang, A. von Jouanne, and A. Wallace, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *in Proc. 33rd IAS Annual Meeting*, pp. 752-758, 1998.

[11] H. Zhang, A. V. Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, Vol. 36, No. 6, pp. 1645-1653, Nov./Dec. 2000.

[12] J. Rodríguez, J. Pontt, P. Correa, P. Cortés, and C. Silva, "A new modulation method to reduce common-mode voltages in multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 4, pp. 834-839, Aug. 2004.

[13] N. V. Nho, Q. T. Hai and H. H. Lee, "Carrier based single-state PWM technique for minimizing vector errors in multilevel inverters," *Journal of Power Electronics*, Vol.10, No. 4, pp. 357-364,Jul. 2010.

[14] N. V. Nho and M. J. Youn, "Comprehensive study on Space Vector PWM and carrier based PWM correlation in multilevel invertors," *IEE Proceedings-Electric Power Applications*, Vol. 153, No. 1, pp. 149-158, Jan. 2006.

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