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A Novel DC Bus Voltage Balancing of Cascaded H-Bridge Converters in D-SSSC Application

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Abstract

This paper introduces a new scheme to balance the DC bus voltages of a cascaded H-bridge converter which is used as a Distribution Static Synchronous Series Compensator (D-SSSC) in electrical distribution network. The aim of D-SSSC is to control the power flow between two feeders from different substations. As a result of different cell losses and capacitors tolerance the cells DC bus voltage can deviate from their reference values. In the proposed scheme, by individually modifying the reference PWM signal for each cell, an effective balancing procedure is derived. The new balancing procedure needs only the line current sign and is independent of the main control strategy, which controls the total DC bus voltages of cascaded H-bridge. The effect of modulation index variation on the capacitor voltage is analytically derived for the proposed strategy. The proposed method takes advantages of phase shift carrier based modulation and can be applied for a cascaded H-bridge with any number of cells. Also the system is immune to loss of one cell and the presented procedure can keep balancing between the remaining cells. Simulation studies and experimental results validate the effectiveness of the proposed method in the balancing of DC bus voltages.

Key words: Cascaded H-bridge, DC bus voltage balancing, D-SSSC, Multilevel converter

I. INTRODUCTION

In the conventional electrical distribution network, the feeders are arranged in the radial format to supply the customers. Nowadays, small power plants and Distributed Generations (DGs) are growing fast to avoid installing new bulk power plants. These DGs are directly connected to the medium voltage network. The configuration of conventional electrical distribution systems may limit the production rate of DGs and needs to change to the looped or even meshed grid topology, which utilizes a power electronic device to manage the power flow. A Distribution Static Synchronous Series Compensator (D-SSSC) is a series converter which is used to loop the radial configuration and is able to control the power flow between the connected feeders [1], [2]. By means of multilevel converter topologies, the D-SSSC can be connected directly to the medium voltage level, omitting the bulky and costly transformer [3].

In recent years, the use of multilevel topologies is growing as a result of increasing the need to process power at the medium voltage levels. The most famous multilevel converters are diode clamp, flying capacitor and cascaded H-bridge converters [4]. Among them, the cascaded H-bridge converter is the best solution for certain type of application as a matter of its modularity, simple control and less elements. But its drawback is the necessity of isolated DC buses and keeping them balanced regardless of discrepancy in the components, losses or different loads connected to H-bridge cells. Fortunately in D-SSSC application the isolation transformer for supplying the DC buses can be avoided, and only the buses should be balanced.

Many methods to balance the DC bus voltages of cascaded H-bridge cells are proposed in the literatures, especially for the FACTS devices. In [5]-[9] the DC bus balancing of cascaded H-bridge as a STATCOM is discussed. In [6] an observer is designed to keep the voltage balancing between the cells, whereas the control strategy seems to be hard to implement. By controlling the active and reactive power of each cell separately, the voltage balancing is achieved in [7], where the procedure

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complexity increases because of calculating the active and reactive power of each cell. In [8] a swapping technique is used to establish DC balancing, where hierarchy of each H-bridge is swapped sequentially with the period of the fundamental frequency. This method is able to only compensate the unbalancing effect of its main control strategy. In [9] a feedback control strategy for balancing individual DC capacitor voltages, based on detailed small-signal model is presented, and the effect of the method is shown for three different mode of STATCOM operation. Expanding this method to different switching frequency and H-bridges with different number of cells is quite challenging. The references [10] and [11] propose a balancing method for other applications of cascaded H-bridge, where in [10] both the low frequency (stepped modulation) and high frequency [pulse-width modulation (PWM)] switching methods are utilized to provide DC balancing for a cascaded H-bridge rectifier. In [11] two modulation strategies are introduced to keep balancing between cells for an asymmetric cascaded H-bridge which the power drawn from all of the DC sources are balanced except for the DC source used in the first H-bridge by using a rotating switching function.

In this paper a novel method to balance the DC bus voltages in a cascaded H-bridge inverter is introduced. This method is based on applying slightly different modulation index for each cell, while keeping the output voltage almost unchanged. The method needs only the line current sign and is independent of the main control strategy. This method can be used for the cascaded H-bridge with any number of cells. According to the current sign and injected voltage reference, each cycle is divided in 4 quarters. The impact of modulation variation in the DC bus voltage of the H-bridge cell in D-SSSC application is determined and applied to it for balancing the DC bus voltages. As a result of controlling the total DC bus voltage independently from individual cells, the method can still keep balancing if one cell is bypassed or shorted. Simple implementation with low computational efforts, using conventional modulation strategy, expandability for cascaded H-bridge with different cell numbers and working in faulted condition are the major advantages of the proposed method.

II. D-SSSC TOPOLOGY

Fig. 1 shows the 7 level cascaded H-bridge which is used as D-SSSC and is in series with a line. The D-SSSC acts as a capacitive or inductive impedance to control power flow between two feeders from different substations. As demonstrated in Fig. 2 the injected voltage, V_S, is composed of V_{S_q} and V_{S_d} which are respectively the components in quadrature and in phase with the line current. The in phase

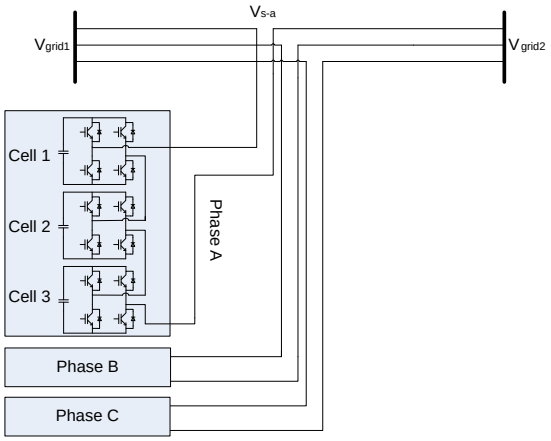


Fig. 1. Seven level cascaded H-bridge as a D-SSSC.

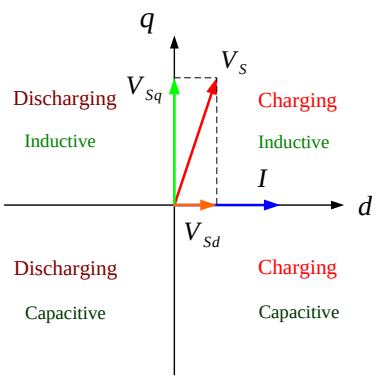


Fig. 2. Injected voltage and line current phasor diagram.

component can be used to maintain DC bus voltage and the quadrature component is used to resemble a capacitive or inductive impedance to control the power flow.

The block diagram of the power flow control strategy for each phase is shown in Fig. 3. The reference value of active power (reactive power or line current) is compared with its actual value generating the active power (reactive power or current) error. The modulation index of the quadrature injected voltage, u_{q_max}, is generated using a PI controller.

The output of PI controller is used to identify the D-SSSC operation mode. The line current increases when the injected voltage decreases the line impedance by inserting a lower inductive impedance or higher capacitive impedance, and vice versa.

A PLL is used to identify the line current phase. When the PI controller output is negative the injected voltage has $+90^o$ phase shift with respect to the line current (inductive mode), while it will be -90^o if the PI controller output becomes positive (capacitive mode).

Another control loop is used to maintain the DC bus voltage at its reference value. The reference voltage is compared to the actual value (the sum of capacitor voltages) and, using a PI controller, the in phase component of injected voltage (u_{d_max}) is developed. A limiter is used to keep the in phase voltage

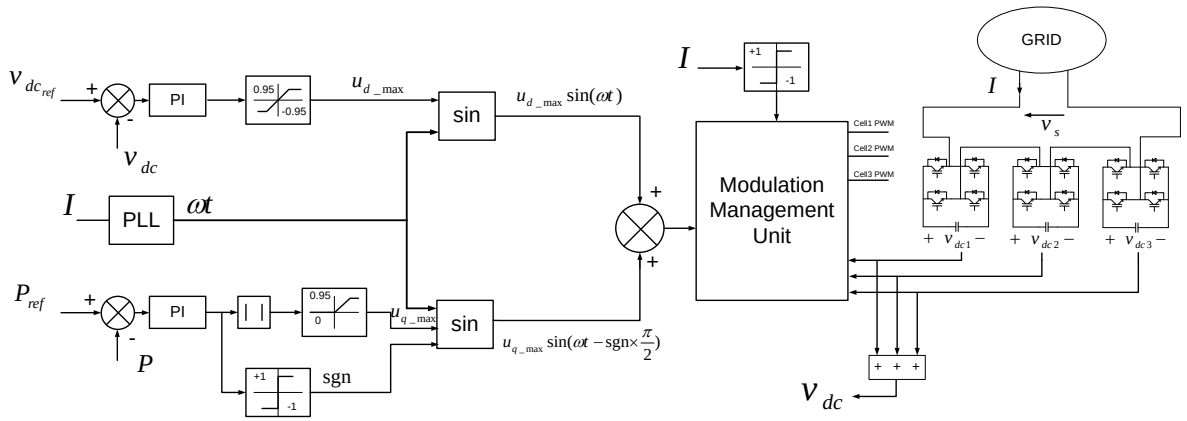


Fig. 3. Block diagram of D-SSSC control strategy

amplitude within its proper range. The reference value for the PWM generator is developed by adding two output signals together.

As demonstrated the total value of DC bus voltages is controlled by the main control strategy. The Modulation Management Unit (MMU) which is proposed in this paper provides cell switches command and DC bus balancing which is presented in the next section.

III. MODULATION MANAGEMENT UNIT

A. Modulation Strategy

Modulation of any carrier based PWM strategy is quite challenging. The popular modulation strategies are Phase Shift Carrier PWM, Phase Disposition Carrier PWM and Phase Opposition Disposition Carrier PWM. Phase Shift Carrier PWM is more common because of its lower harmonic contents. The sinusoidal reference waveforms for the two legs of each cell are phase shifted by 180^o while each cell carrier is phase shifted by $180^o/N$, where N is the number of H-bridges. This modulation strategy leads to cancellation of all carrier and associated sideband harmonics up to the $2N^{th}$ carrier group [12], [13]. To balance the DC bus voltages of a cascaded H-bridge, each cell reference voltage is derived separately in the proposed scheme.

B. H-Bridge Capacitor Sizing

The DC bus capacitor should be selected according to the required DC bus voltage ripple. Fig .4 shows a cell of a cascaded H-bridge converter where the output voltage can be +E, 0, -E regarding the switches states.

As demonstrated in Table I the capacitor can be charged when the output voltage is +E and the current is positive or the output voltage is –E and the current is negative. Also the capacitor discharges when the output voltage is +E and the current is negative or the output voltage is –E and the current is positive. When the output is zero, the capacitor is not able to charge or discharge by the system current.

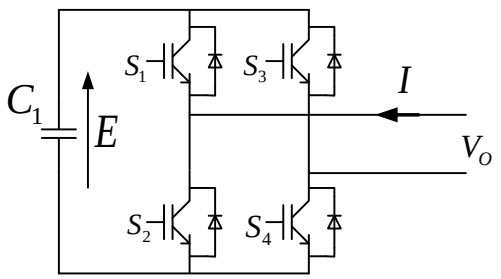


Fig. 4. An H-bridge cell of a cascaded H-bridge multilevel converter.

TABLE I

H-BRIDGE SWITCHING STATE

S_1	S_2	S_3	S_4	Output Voltage	Line Current Sign	Capacitor State
1	0	0	1	+E	+	Charging
					-	Discharging
0	1	0	1	0	+	Constant
					-	Constant
0	1	1	0	-E	+	Discharging
					-	Charging
1	0	1	0	0	+	Constant
					-	Constant

So these features of an H-bridge can be used to change its DC bus voltage by modifying the modulation index which is introduced as follow:

Fig. 5(a) shows the line current and first harmonic of the injected voltage of an H-bridge cell where there is $+90^o$ degree phase shift between them. The DC bus voltage during this injection is shown in Fig. 5(b) where it consists of a dc part, V_{dc} and a 2ω peak-to-peak ripple, V_R. The voltage ripple can be calculated using the energy equivalence assumption. The DC bus capacitor C_T has a total energy, $E_C(t)$, composing a DC component E_{dc} and ac component $E_{ac}(t)$.

The ac energy of capacitor can be determined via net ac power flowing into and out of the capacitor as mentioned in

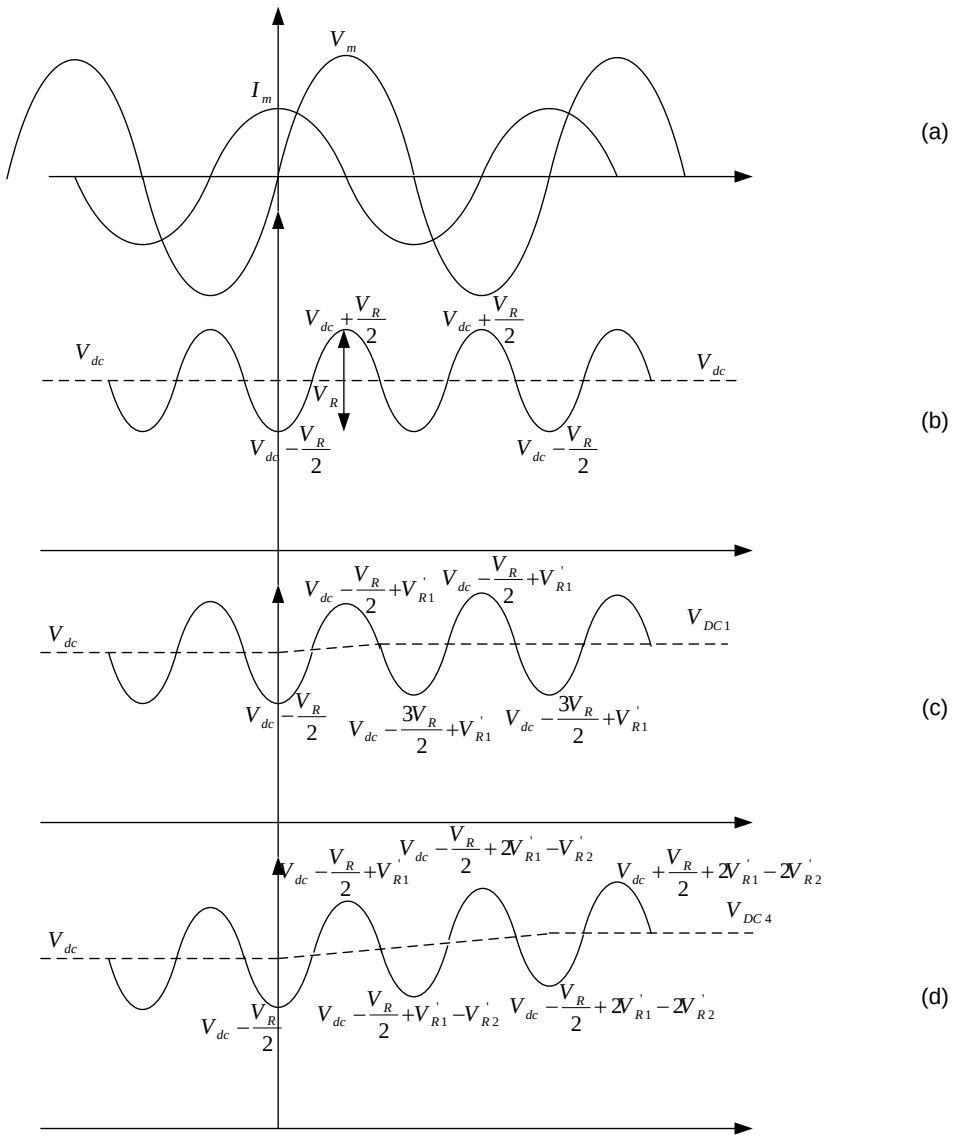


Fig. 5. (a) injected voltage and line current, (b) DC bus voltage without using balancing procedure, (c) DC bus voltage with balancing in one quarter of line period, (d) DC bus voltage with balancing in all the quarters of line period.

(1).

$$E_{ac}(t)=\int\left(p_i(t)-p_o(t)\right)dt \tag{1}$$

As there is no external source to charge the capacitor the $p_i(t)$ is equal to zero. The injected voltage of converter is always in quadrature to the line current. So the output power can be derived as (2) and the capacitor ac energy is equal to (3):

$$P_o(t)=V_m\sin(\omega t)I_m\sin(\omega t\pm\frac{\pi}{2}) \tag{2}$$

$$E_{ac}(t)=\frac{V_mI_m}{4\omega}\sin(2\omega t\pm\frac{\pi}{2}) \tag{3}$$

The peak-to-peak ripple in the capacitor voltage, V_R is related to the ΔE_C which is indicated in (4):

$$\Delta E_C=\frac{1}{2}C_T\left[(V_{dc}+\frac{V_R}{2})^2-(V_{dc}-\frac{V_R}{2})^2\right]=\frac{V_mI_m}{2\omega} \tag{4}$$

So the peak-to-peak ripple in the capacitor is derived as (5):

$$V_R=\frac{V_mI_m}{2\omega CV_{dc}} \tag{5}$$

By replacing the peak voltage according to the modulation index, $V_m=MV_{dc}$, the peak-to-peak ripple becomes as (6):

$$V_R=\frac{MI_m}{2\omega C} \tag{6}$$

Where the capacitor can be sized from (6) to have proper peak-to-peak voltage ripple.

C. Balancing Procedure

As demonstrated in Fig. 5(c) if the modulation index is changed to (M+ΔM) only for a quarter of cycle, where the current and voltage are positive, the peak-to-peak voltage ripple for that quarter will be changed to V'_{R1}, where:

$$V'_{R1} = \frac{(M+\Delta M)I_m}{2\omega C} \tag{7}$$

The time expression of new capacitor voltage is given in (8):

$$V_C(t) = V_{dc} - V_R + V'_{R1} + \frac{V_R}{2}\cos(2\omega t) \tag{8}$$

The DC bus voltage of the capacitor is derived as (9):

$$V_{DC1} = \frac{1}{T}\int_0^T V_C(t)dt = V_{dc} - V_R + V'_{R1} \tag{9}$$

Substituting the V_R and V'_{R1} in (9) from (6) and (7), the new DC bus voltage is obtained as (10).

$$V_{DC1} = V_{dc} + \frac{\Delta M I_m}{2\omega C} \tag{10}$$

So by applying a change of ΔM in the modulation index only for a quarter of cycle a new DC bus voltage is obtained. Considering (10), a positive ΔM will increase the DC bus voltage and negative one decrease the DC bus voltage. Note that if the same variation in modulation index has been applied to all quarters of a cycle the DC part of capacitor voltage would stay constant and only its ripple would change.

Fig. 5(d) shows the same modulation changing procedure for all four quarter of cycle where for the first and third quarter (where the capacitor is charging) the modulation index is changed to (M+ΔM) while for the second and fourth quarter (where the capacitor is discharging) is changed to (M-ΔM). The peak-to-peak voltage ripples will be derived as $V'_{R1} = \frac{(M+\Delta M)I_m}{2\omega C}$ and $V'_{R2} = \frac{(M-\Delta M)I_m}{2\omega C}$.

The time expression of capacitor voltage becomes as (11).

$$V_C(t) = V_{dc} + 2V'_{R1} - 2V'_{R2} + \frac{V_R}{2}\cos(2\omega t) \tag{11}$$

The DC bus voltage of the capacitor in this case is denoted as V_{DC4} and is derived as (12).

$$V_{DC4} = \frac{1}{T}\int_0^T V_C(t)dt = V_{dc} + 2V'_{R1} - 2V'_{R2} = V_{dc} + \frac{2\Delta M . I_m}{\omega C} \tag{12}$$

As it is clear the effect of modulation changing becomes 4 times of the changing in one quarter. The same procedure can be done for applying this technique in 2 or 3 quarters which will result to the DC bus voltages of (13) and (14), respectively.

$$V_{DC2} = V_{dc} + \frac{\Delta M I_m}{\omega C} \tag{13}$$

$$V_{DC3} = V_{dc} + \frac{3\Delta M I_m}{2\omega C} \tag{14}$$

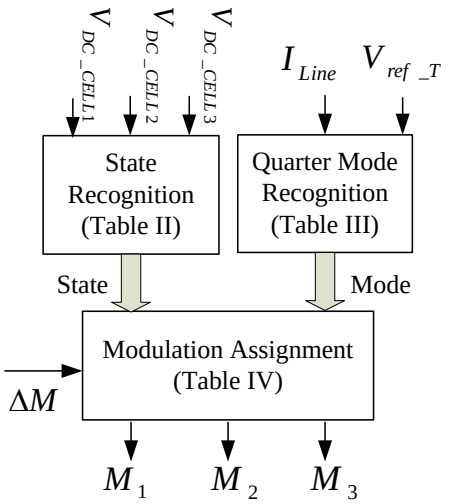


Fig. 6. Balancing method block diagram.

TABLE II

STATES OF CELLS DC BUS VOLTAGE

States	Conditions
ST1	$V_{Cell1} \le V_{Cell2} \le V_{Cell3}$
ST2	$V_{Cell1} \le V_{Cell3} \le V_{Cell2}$
ST3	$V_{Cell2} \le V_{Cell1} \le V_{Cell3}$
ST4	$V_{Cell2} \le V_{Cell3} \le V_{Cell1}$
ST5	$V_{Cell3} \le V_{Cell1} \le V_{Cell2}$
ST6	$V_{Cell3} \le V_{Cell2} \le V_{Cell1}$

This procedure of changing the DC bus voltage by modifying the modulation index can be applied for balancing the DC bus voltages of a cascaded H-bridge. The total DC bus (the sum of all cells DC bus) is controlled by the main control unit, where applying the proper u_{d_max} guarantees that the DC bus voltage be equal to its reference. So by independently changing the modulation index of each cell according to the proposed method, the balancing can be achieved. The modulation changing procedure depends on the cells DC bus voltages difference. Where the cell with higher DC bus voltage is assigned with a modulation index to decrease it, and vice versa. Note that the ΔM is chosen as small value and can be added or subtracted from the modulation index M to fulfill the balancing requirements. In the implementation, it can be selected as the smallest step of modulation index changing. The proposed balancing method block diagram is shown in Fig. 6.

First, the cells are arranged according to their DC bus voltages. For example for 7-level cascaded H-bridge which is consisted of 3 cells, the numbers of states are 6 as demonstrated in Table II.

Then using the line current and injected voltage reference sign, the quarters of cycle are identified and demonstrated in Table III.

TABLE III

CONVERTER OPERATION MODE

Voltage sign	Current sign	Mode
Positive	Positive	M1=Charging
Positive	Negative	M2=Discharging
Negative	Positive	M3=Discharging
Negative	Negative	M4=Charging

TABLE IV

MODULATION ASSIGNMENT

Cell #	Cell #1 Command		Cell #2 Command		Cell #3 Command	
Mode	M1 or M3	M2 or M4	M1 or M3	M2 or M4	M1 or M3	M2 or M4
ST1	+ΔM	-ΔM	0	0	-ΔM	+ΔM
ST2	+ΔM	-ΔM	-ΔM	+ΔM	0	0
ST3	0	0	+ΔM	-ΔM	-ΔM	+ΔM
ST4	-ΔM	+ΔM	+ΔM	-ΔM	0	0
ST5	0	0	-ΔM	+ΔM	+ΔM	-ΔM
ST6	-ΔM	+ΔM	0	0	+ΔM	-ΔM

TABLE V

MODULATION INDEX CHANGING FOR THE CASCADED H-BRIDGE WITH DIFFERENT CELL NUMBERS

number of cells	number of levels	modulation changing
2	5	+ΔM , -ΔM
3	7	+ΔM , 0 , -ΔM
4	9	+2ΔM , +ΔM , -ΔM , -2ΔM
5	11	+2ΔM , +ΔM , 0 , -ΔM , -2ΔM

Then by choosing a small value for ΔM the appropriate modulation index is chosen for each cell. For example if the state is ST1 and the voltage mode is charging positive, a +ΔM is chosen for the first cell modulation index and a -ΔM is chosen for the third cell while the second cell modulation index is kept unchanged. Table IV shows the modulation variation for each cell in different modes and states where the increment, decrement and unchanged modulation index are denoted by +ΔM, -ΔM and 0, respectively.

Actually the balancing procedure can be applied for each switching intervals and also for one, two, three or four quarters. Where for example changing the modulation index by ΔM in all the quarters, produces the same DC bus voltage variation as applying the modulation index alteration by 4ΔM for one quarter.

D. Establishing The Method For Cascaded H-Bridge With Different Cell Number

For balancing the DC bus voltages of a cascaded H-bridge with the other cell numbers, the same procedure can be established. Table V shows the modulation index variation for the cascaded H-bridge with 2 to 5 cells.

For example for a nine level cascaded H-bridge which is in its first state ($V_{Cell1} \le V_{Cell2} \le V_{Cell3} \le V_{Cell4}$) and the converter mode is M1, the modulation changes can be +2ΔM, +ΔM, -ΔM, -2ΔM for cell1 to cell4, respectively.

Also the combination between the modulation index variation and applying the procedure for some quarters of cycle can be used for balancing procedure. For the above example the other possibility is to apply +ΔM in four quarters for cell1 and two quarters for cell2, and -ΔM in two quarter for cell3 and four quarters for cell4.

It should be noted that the balancing procedure in four quarters with smaller modulation changing is more desirable to the bigger modulation index variation in part of quarters.

IV. SIMULATION RESULTS

A part of Tehran electrical distribution network is chosen for simulation studies where a seven level cascaded H-bridge acts as D-SSSC to connect two separate feeders from different substations together. Each phase of converter consists of three cells with isolated DC bus. The total DC bus voltage is controlled as 1000V by the main controller to fulfill the requirement of system. So each cell capacitor voltage should be controlled at 333V to have balanced DC bus voltages. In the simulation studies for making the cells intentionally unbalanced, a parallel resistor is added to the second cell DC bus as demonstrated in Fig. 7.

The effect of applying the DC bus balancing procedure is shown in Fig. 8, where the difference between the DC bus voltages reaches to 60V before applying the balancing procedure at t=3s. Figs. 8(a) to (d) are for applying the balancing method with ΔM=0.01 in one quarter to all quarters, respectively. As it is clear by increasing the applied quarters in each cycle, the balancing method becomes more effective. Where for applying balancing procedure in one quarter it takes 3 seconds to have a balanced DC bus voltages while for two, three and four quarters it takes 1, 0.5 and 0.3 second, respectively. It should be noted the applied resistor introduces a severe unbalancing in the DC bus voltages, where the proposed method shows its ability to handle this unbalancing.

The effect of balancing procedure on the D-SSSC output voltage with and without balancing procedure are shown in Figs. 9(a) and (b), respectively, which results to less distorted output voltage.

Also as mentioned before, the proposed balancing method can still handle the balancing between cells even if one or more cells are bypassed due to any fault. Fig. 10(a) shows the total and each cells DC bus voltages, when at t=2s the cell3 becomes a short circuit.

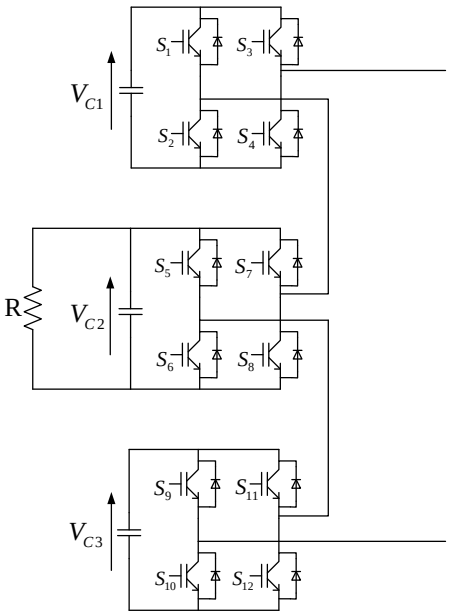
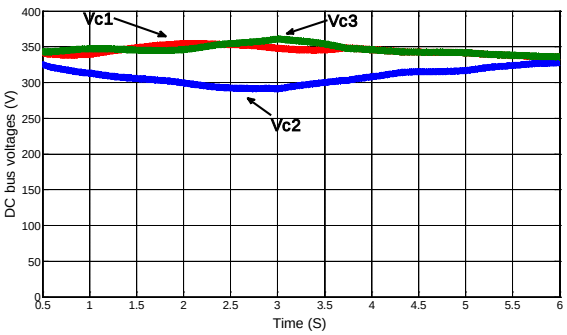
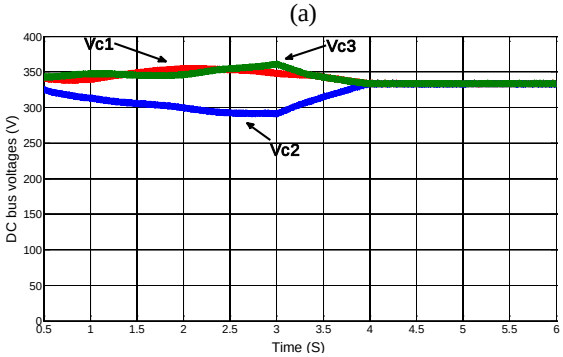


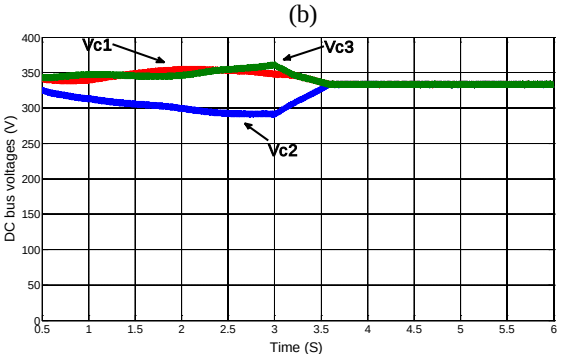
Fig. 7. Unbalanced seven level cascaded H-bridge by placing a resistor on second cell DC bus.



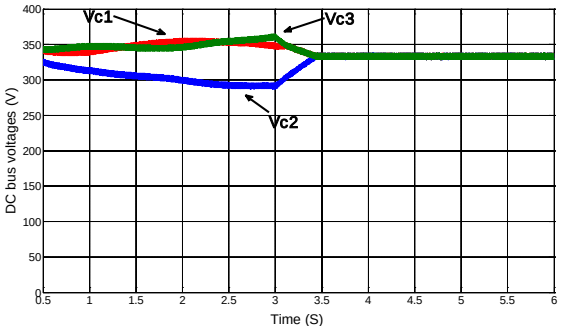
(a)



(b)

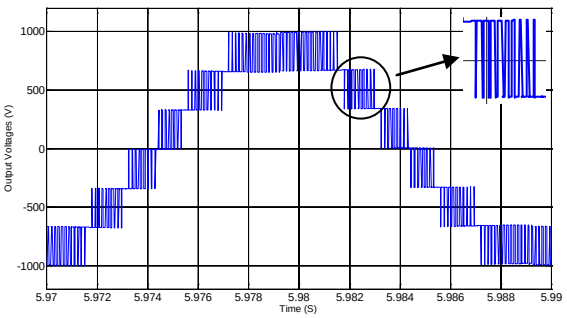


(c)

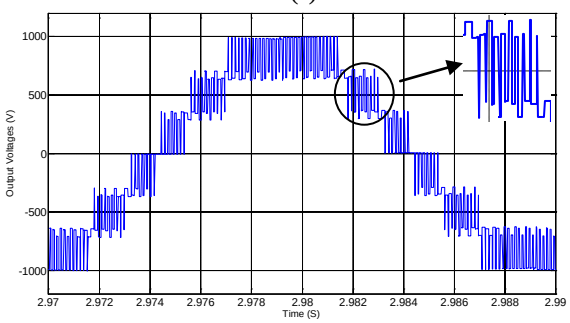


(d)

Fig. 8. DC bus voltages of cells: (a) balancing procedure in one quarter, (b) two quarters, (c) three quarters, (d) all the quarters.



(a)



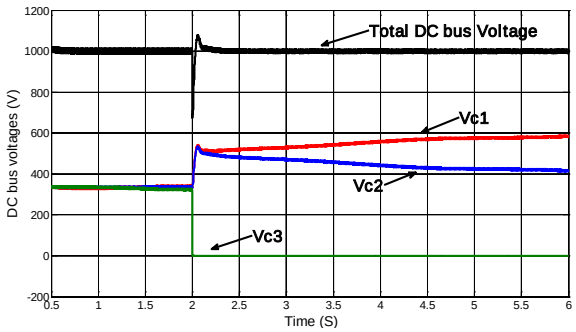
(b)

Fig. 9. Output voltage: (a) with balancing method (b) without balancing method.

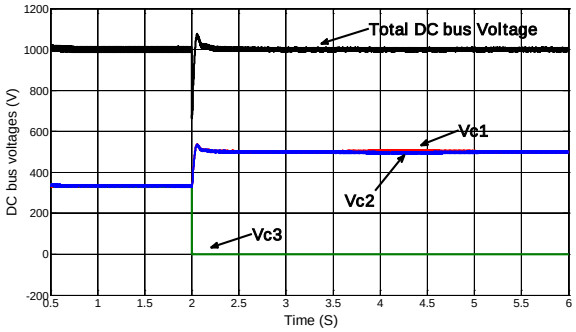
As it is clear the main controller can handle the total DC bus voltage at its reference value but the DC bus voltage of cell1 and cell2 diverge from each other. Fig. 11(b) shows the same voltages when the proposed balancing method is applied to the system which the DC bus voltages of cell1 and cell2 changes from 333V to 500Vand remain balanced even the cell3 reaches to zero.

V. IMPLEMENTATION

The simple scaled down model of the system is implemented by using a single phase cascaded H-bridge converter which consists of 3 H-bridge cells to produce seven level output voltage. The parameters of the experimental setup are given in Table VI, and Fig. 11 shows its major parts. The voltages and



(a)



(b)

Fig. 10. DC bus voltage during fault: (a) without balancing method, (b) with balancing method.

TABLE VI

IMPLEMENTED SYSTEM PARAMETERS

Source voltage (rms)	100 V
Output Frequency	50 Hz
Converter Power (single phase)	1 KVA
Switching frequency	1 KHz
Line inductance	110 mH
Line resistance	33 Ω

currents in the experimental setup are 1/10 and 1/100 of the case study quantities, respectively. So in the experimental setup, the impedances will be 10 times of the real network. In the case study the line inductance and resistance, including the transformers leakage inductances and series resistances, are 11mH and 3.3Ω, respectively. Which lead to 110mH inductance and 33Ω inductance in Table VI. A TMS320F2812 DSP controller is used as the main processor to control the procedure and generate the PWM signals for each cell. A resistor is paralleled to one of the cells to increase the unbalancing between cells in the implemented setup.

A. Applying Balancing Procedure for Different Quarters of a Cycle

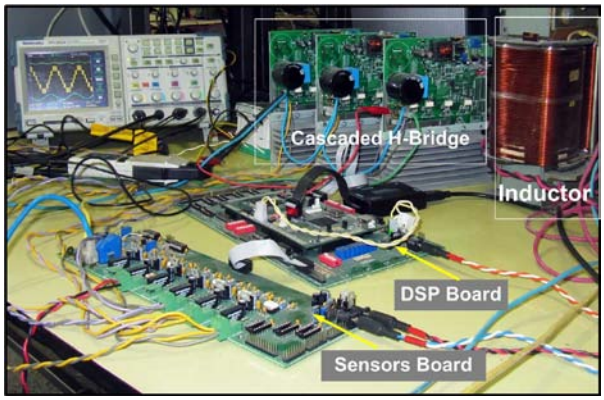


Fig. 11. Experimental setup.

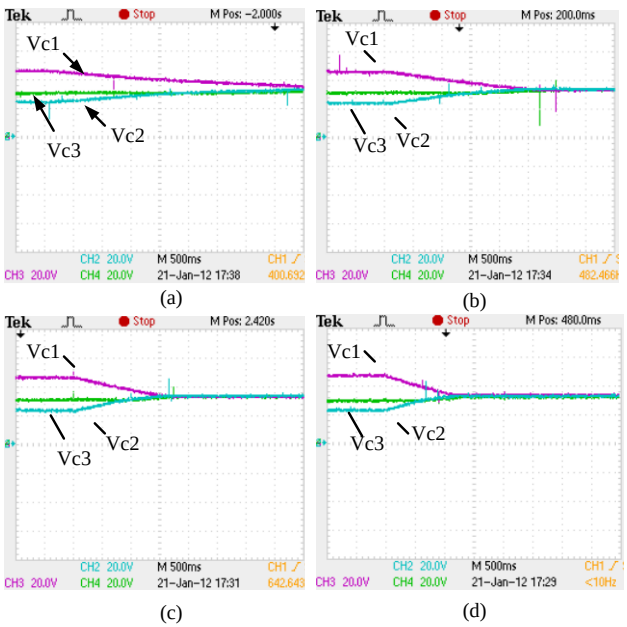


Fig. 12. DC bus voltages of Cells for: (a) one quarter, (b) two quarter, (c) three quarter, (d) four quarter.

Fig. 12(a) to (d), show the cells DC bus voltages when the balancing procedure is applied to unbalanced system for one, two, three and four quarters of cycle, respectively. ΔM is chosen as a smallest step of modulation index, which is 1/256.

By applying the balancing procedure the DC bus voltages are balanced to 33V. Where before applying the balancing procedure the DC bus voltage has a difference up to ±25% of their nominal value. As discussed before, increasing the applied quarter of balancing procedure leads to more effective balancing.

Fig. 12(a) is for applying the balancing procedure for one quarter which it takes 4.5s to balance the DC bus voltages while this time interval decrease to 1s, when the proposed method is applied for all the quarters as demonstrated in Fig. 12(d). Also for two and three quarters, this time interval is 2s and 1.5s, respectively.

B. Balancing Procedure For Different Line Current

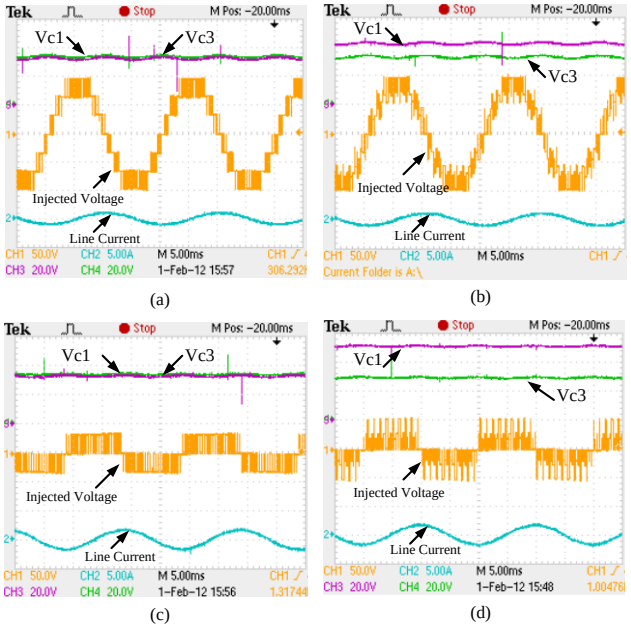


Fig. 13. Output voltage, two cells DC bus voltage and line current in inductive impedance injection mode: (a) I_{Line_rms}=0.7A with balancing procedure, (b) I_{Line_rms}=0.7A without balancing procedure, (c) I_{Line_rms}=1.2A with balancing procedure, (d) I_{Line_rms}=1.2A without balancing procedure.

According to (10), (12) to (14), the DC bus voltage depends on the line current. In order to show the effectiveness of the procedure to balance the DC bus voltages for different line current the following experimental tests are arranged.

Figs. 13 and 14 show the output voltage and cells DC bus voltages without and with balancing procedure when the SSSC acts as inductive and capacitive impedance, respectively. The balancing procedure is able to keep balancing between the cells DC bus voltage for different power flow. The current changes from 0.7A to 1.8A by injecting highest inductive impedance in Figs. 13(a) and 13(b) to highest capacitive impedance in Figs. 14(c) and 14(d).

The bigger 100Hz ripple in the DC bus voltage for higher power injection are noticeable in Figs. 13(a),(b) and 14(c),(d).

C. Balancing Procedure During Short Circuit Of One Cell

Fig. 15 shows the ability of proposed method to balance the DC bus voltages during a short circuit of one cell. To avoid damaging the H-bridges, two lower switches in each leg are turned on, to simulate a short circuit in the cell. The cell with paralleled resistor to its DC bus capacitor is selected to be shorted. In Fig. 15(a) the balancing procedure is available. After short circuiting of one cell, the other DC bus voltages keep their balancing and reaching to 50V from 33V. Fig. 15(b) shows the same procedure while the balancing procedure is stopped when one cell is shorted. The remained cells are not able to keep balancing between each other and the whole DC bus voltage should be tolerated by cell1.

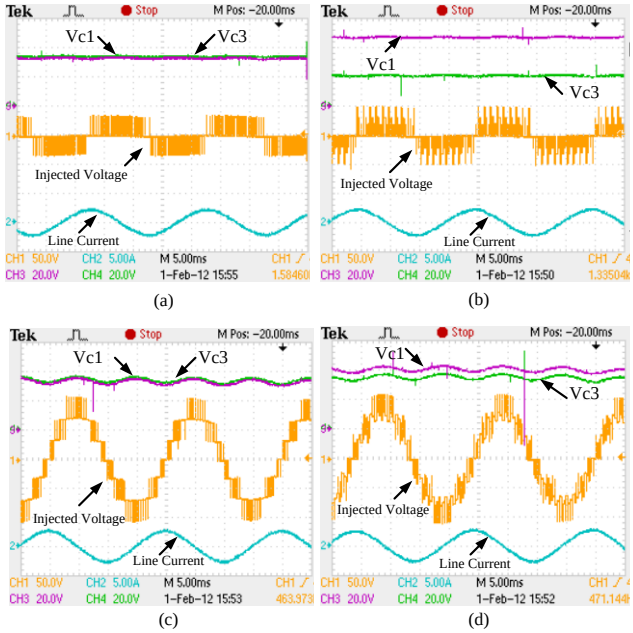


Fig. 14. Output voltage and cells DC bus voltage in capacitive impedance injection mode: (a) I_{Line_rms}=1.5A with balancing procedure, (b) I_{Line_rms}=1.5A without balancing procedure, (c) I_{Line_rms}=1.8A with balancing procedure, (d) I_{Line_rms}=1.8A without balancing procedure.

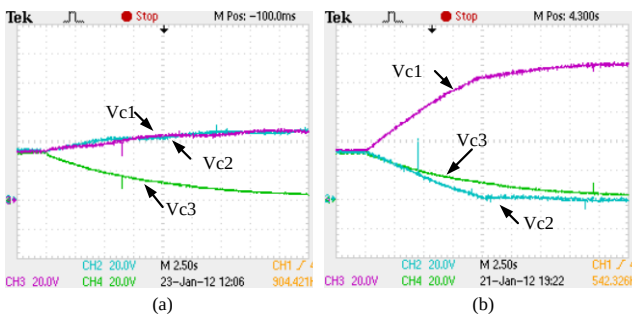


Fig. 15. DC bus voltages during short circuiting of cell1: (a) with balancing procedure (b) without balancing procedure.

VI. CONCLUSIONS

In this paper a method for balancing the DC bus voltages of a cascaded H-bridge in D-SSSC application has been presented. The method is based on the slightly modifying the modulation index of each H-bridge independently to keep balancing between them. The proposed method has no restriction on cascaded cell number and can handle the balancing in faulty mode when one or more cells become short circuit. The analytical calculation is done to show the effect of modifying the modulation index in each quarter of line voltage on DC bus voltage for an H-bridge and then it is extended to provide balancing for a cascaded H-bridge converter. The feasibility of balancing method was shown by different simulation studies and experimental results on an implemented seven level cascaded H-bridge.

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