Start-Up Current Control Method for Three-Phase PWM Rectifiers with a Low Initial DC-Link Voltage

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Abstract

When a PWM rectifier has a low DC-link voltage during startup, the output voltage vector cannot be high enough to regulate the input current. This lack of a PWM rectifier output voltage vector can cause an unregulated inrush current when the rectifier operation starts. This paper presents a PWM rectifier start-up current control algorithm for when it starts operation with a lower DC-link voltage than unloaded condition case. To avoid the unregulated inrush current caused by a lack of DC-link voltage, the proposed control scheme regulates the one phase current with one switch chopping and it generates the current command considering the uncontrolled current magnitude information, which is calculated in advance. Simulation and experiment results support the validity of the proposed method.

Key words: AC-DC power rectifier, Industrial power systems, Power conversion, Pulse width modulated power rectifiers, Voltage control

I. INTRODUCTION

The use of three-phase PWM rectifier systems is becoming increasingly popular in many applications, since they can operate at a unity power factor and allow for a bidirectional power flow. Further, PWM rectifiers are advantageous in that the input line current harmonic distortion is very small when compared with diode or thyristor rectifiers [1]-[8].

Since diode rectifiers transform power from the AC to DC without a voltage boosting mechanism, the DC-link voltage is the lower than the peak to peak voltage of the AC. On the other hand, the PWM rectifier boosts the DC-link voltage higher than the input AC voltage. This means that the DC-link voltage is higher than the peak-to-peak gird voltage. Hence the available rectifier output voltage vector, induced from the DC-link voltage, could be higher than the input AC voltage vector. The PWM rectifier has enough of a high output voltage vector margin to suppress the phase currents against the input line voltage vector when this is needed.

Meanwhile, if the PWM rectifier does not start off, it operates only with the free-wheeling diodes like a diode rectifier. Under the unloaded condition, the DC-link voltage is the same as that of the peak-to-peak grid voltage. In this unloaded condition, the available output voltage vector margin of the PWM rectifier is not very low. It has no problem in rectifier operation start since the DC-link voltage increases as soon as the rectifier operation begins. However, in some applications, the PWM rectifier starts to operate in the loaded condition. The DC-link load reduces the initial DC-link voltage so that it is lower than the peak to peak grid voltage. The reduced DC-link voltage generates the reduced rectifier output voltage vector magnitude which does not have enough of a control voltage margin against the input grid voltage. Hence it makes an uncontrolled start-up rectifier current, and the PWM rectifier cannot suppress it until the DC-link voltage rises to a certain level [1], [12]. To make matters worse, if the magnitude of the uncontrolled start-up rectifier current is larger than the system over current limit, the rectifier hardly starts up.

Furthermore, some rectifiers utilize shunt resistors or single current sensors for current measurement [9]-[11]. These shunt resistors or single current sensors are installed at the bottom of the DC-link or between the emitter of the lower power switches and the minus DC-link terminal. They have a current feedback value when the rectifier phase currents flow through them. Hence this forces the PWM rectifier to generate some specified voltage vectors during every PWM period for current
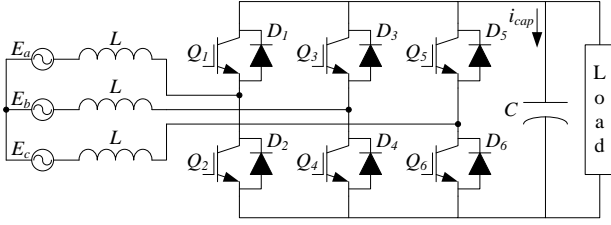
Fig. 1. Three-phase PWM rectifier configuration with load.

measurement. The specified voltage vectors also reduce the available rectifier output voltage vector. The reduced rectifier output voltage vector creates the same problem as a low initial DC-link voltage when the PWM rectifier starts operation. It might make an uncontrolled start-up rectifier current as well.

A previous study showed and analyzed the startup inrush current [12]. It described the usefulness of the input source voltage feed-forward compensation in the synchronous reference frame (SRF). However, it focused on the unloaded condition without a voltage vector limitation.

In this paper, a start-up current control method for PWM rectifiers with a low initial DC-link voltage or a reduced rectifier output voltage vector is proposed. The proposed scheme controls only one phase current with two input AC lines at a time like a diode rectifier. In addition, it generates the current commands after calculating the uncontrolled current magnitude to avoid an unexpected over current in the rectifier. The proposed scheme is advantageous in PWM rectifier start-up operation under the loaded condition or a shunt resistor current measurement rectifier.

II. MODELS OF PWM RECTIFIERS

Fig. 1 shows the PWM rectifier configuration with a load, where E_a, E_b, and E_c denote the input AC grid voltage, L and C denote input boosting inductance and the DC-link capacitor, $Q_1 \sim Q_6$ and $D_1 \sim D_6$ denote the semiconductor switches and the free-wheeling diodes, and i_{cap} denotes the capacitor current. E_a, E_b, and E_c can be described as follows:

$$E_a = A\cos\omega t, \tag{1}$$

$$E_b = A\cos\left(\omega t - \frac{2\pi}{3}\right), \tag{2}$$

$$E_c = A\cos\left(\omega t + \frac{2\pi}{3}\right), \tag{3}$$

where A and ω denote the phase peak voltage and the angular frequency of the input source voltage.

Choosing the dc link voltage and the line currents as a state, the PWM rectifier in the rectifier SRF can be described as:

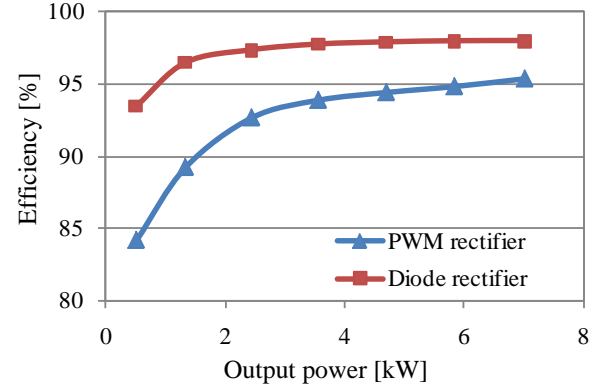$$C\dot{V}_{dc} = i_{cap} = \frac{3}{2}(v_d^e i_d^e + v_q^e i_q^e) - i_{load}, \tag{4}$$

Fig. 2. Output power versus efficiency of PWM rectifier and diode rectifier with 50A/1200V IGBT module, : input line voltage *380V_rms*, *L=2.27mH, C=1680μF*.

$$L\dot{i}_d^e = \omega L i_q^e + E_d^e - v_d^e, \tag{5}$$

$$L\dot{i}_q^e = -\omega L i_d^e + E_q^e - v_q^e \tag{6}$$

where $v_d{}^e$ and $v_q{}^e$ denote d-q axes PWM rectifier output voltage vector, $i_d{}^e$ and $i_q{}^e$ denote d-q axes rectifier currents, $E_d{}^e$ and $E_q{}^e$ denote d-q axes source voltages in the rectifier SRF, respectively. i_{cap} and i_{load} denote the capacitor current and the load current. The dc link capacitor voltage is denoted by V_{dc}. If the reference frame is aligned to the d-axis of the source voltage, then let $E_q{}^e = 0$.

Since the rectifier output voltage vector is induced from the DC-link voltage, it is limited as follows:

$$-\frac{2}{3}V_{dc} < v_d^e < -\frac{2}{3}V_{dc},$$
$$-\frac{2}{3}V_{dc} < v_d^e < -\frac{2}{3}V_{dc}, \tag{7}$$
$$\sqrt{v_d^{e2} + v_q^{e2}} < \left(\frac{2}{3}V_{dc} \sim \frac{1}{\sqrt{3}}V_{dc}\right).$$

If the DC-link voltage is high enough, the rectifier output voltage vector has a wide range of output voltage.

When the PWM rectifier stops its operation, all of the active switches $Q_1 \sim Q_6$ are turned off and the PWM rectifier operates with the free-wheeling diodes $D_1 \sim D_6$ as a diode rectifier. Since the diode rectifier converts power from AC to DC without a voltage boosting mechanism, the maximum DC-link voltage is the line to line peak voltage of the input source voltage.

III. START OPERATION PROBLEM WITH A LOW DC-LINK VOLTAGE

PWM rectifiers cause unwanted switching losses. In addition, a high DC-link voltage may cause an unwanted loss at the load, since the inverters for motor drives are connected to the DC link as a load in many applications. If the inverter is connected
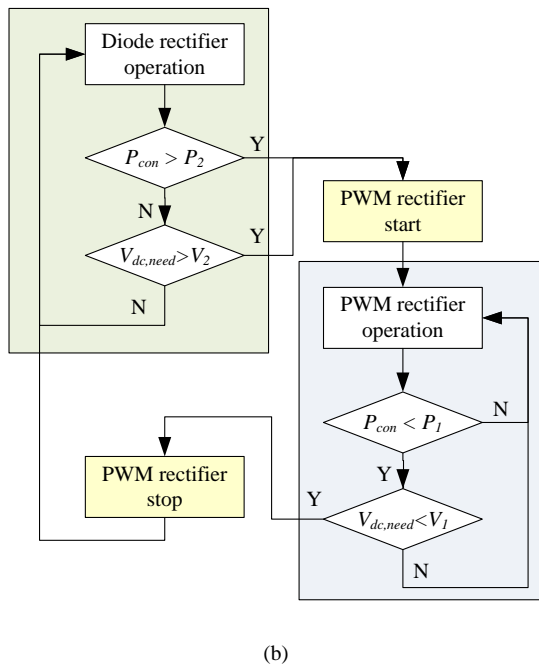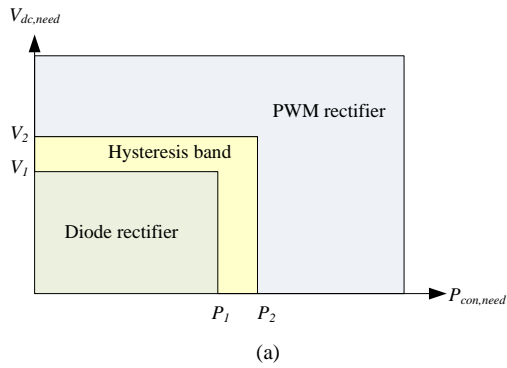
(a)

(b)

Fig. 3. (a) The PWM rectifier's control strategy for high efficiency, (b) control sequence.

TABLE I

SYSTEM SPECIFICATIONS

Items	Values
Input grid voltage	$380V_{rms}$
Input boosting inductance L	2.27mH
DC-link capacitance C	1680uF
Switchs Q_1~Q_6	IGBT, 50A/1200V (Mitusbishi)

to the DC-link as a load, the PWM rectifier not only generates its own switching loss but also increases the inverter's switching loss by a higher DC-link voltage than the diode rectifier's DC-link output voltage. Fig. 2 (a) shows efficiency test results with the PWM rectifier and the diode rectifier, depending on the rectifiers' output power. Table I shows the system specifications for the test. The diode rectifier has a higher efficiency than the PWM rectifier due to the switching
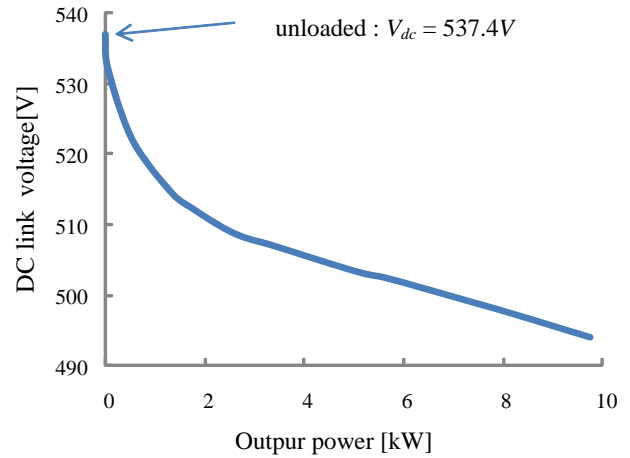

Fig. 4. Output power versus DC-link voltage of diode rectifier .

loss.

Avoiding switching loss, without the PWM rectifier operation, which is rectifying the input line voltage with only the free-wheeling diodes of switches like the diode rectifier, is more beneficial from the viewpoint of system efficiency. When the load needs a high DC-link voltage or consumes a lot of power, the PWM rectifier operates to meet the high DC link voltage demand or to limit the input current harmonics cased by the high power demand. Fig. 3 shows this PWM rectifier operation scheme. The hysteresis band is included for stable operation under the boundary condition. This scheme is only used for a one-directional power flow from the input AC to the load. For a reverse power flow, the control scheme proposed in [13] is an answer to reduce the switching loss. Since the PWM rectifier has the same topology as [13], except for the snubber capacitor, this switching scheme can be easily applied to handle the reverse power flow.

Fig 4 shows the simulation results of the diode rectifier's DC-link voltage along the output load power. As the output load power grows, the diode rectified DC-link voltage decreases. When the PWM rectifier begins operation, the DC-link voltage is lower than under the unloaded condition. By (7), the low DC-link voltage makes the lack of a control voltage margin to regulate and suppress the PWM rectifier current. Consequently, this makes the current controller unstable and increases the uncontrolled rectifier current. The unstable states continue until the DC-link voltage is high enough to regulate the input line current.

Fig. 5 shows the rectifier voltage vector space (hexagonal shape) defined by the initial DC link voltage and the input AC voltage vector (round shape). The output voltage margin in the figure shows the PWM rectifier voltage for suppressing the input AC currents. In Fig. 5 (a), the PWM rectifier operates with a boosted DC link voltage. A large DC-link voltage makes enough of a voltage margin, and the phase currents and d-axis current are regulated as shown in the bottom of the figure. Fig.
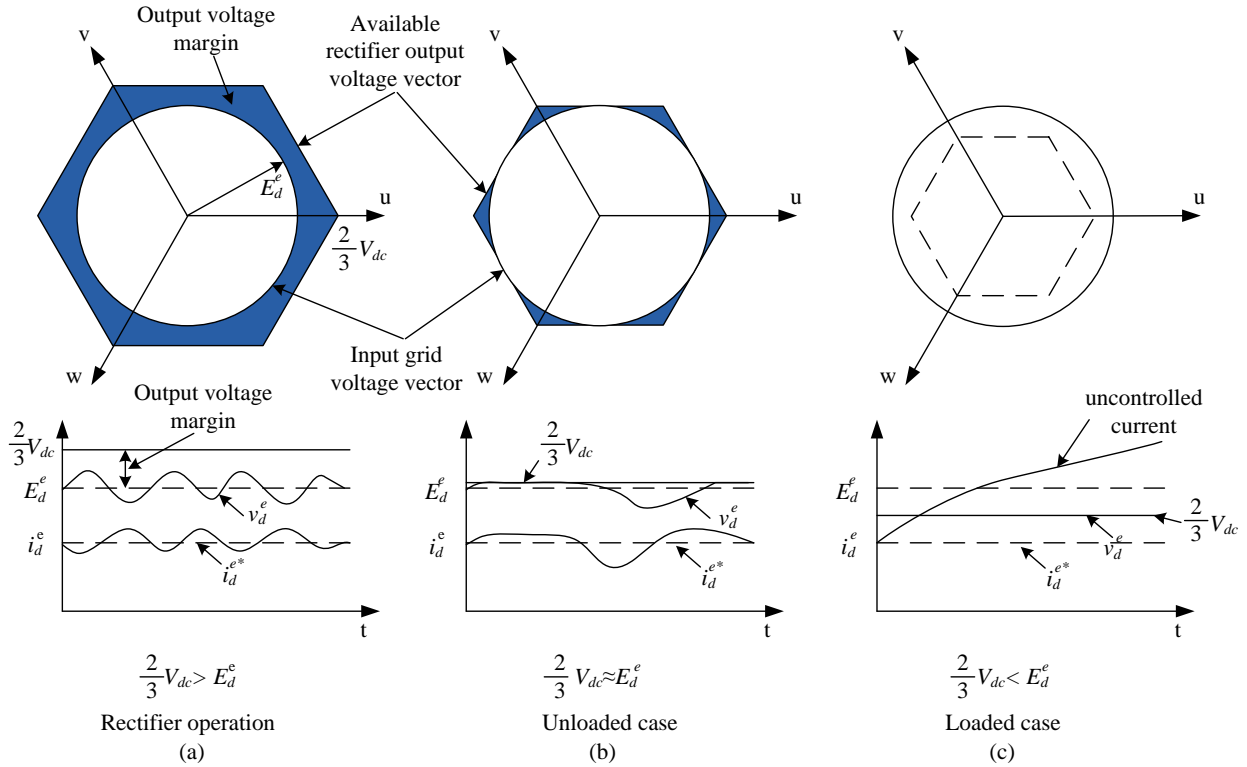
Fig. 5. Top : PWM rectifier's output voltage vector, bottom : plots of voltage and current when PWM rectifier operates with (a) boosted DC link voltage, (b) the DC link voltage having the same voltage with the peak to peak input AC voltage (PWM rectifier starts off with unloaded condition), (c) the DC link voltage having lower voltage than the peak to peak input AC voltage (PWM rectifier starts off with loaded condition).

5 (b) shows when the DC link voltage is the same as the peak to peak voltage of the input AC. Although the output voltage margin is low, the phase current and the d-axis current are not well regulated. However, no unregulated current exists. Fig. 5 (c) shows when the DC link voltage is lower than the input AC vector. In this case, since the rectifier output voltage vector's maximum is less than the input voltage vector, the rectifier current controller fails in the phase currents and the d-axis current regulation. Hence, the d-axis currents increase continuously as shown at the bottom of the figure.

If the PWM rectifier uses a single sensor or a shunt resistor for current measurement, it will occasionally generate additional voltage vectors, which are irrelevant to the current controller, to measure the input line current [9]-[11]. This additional voltage vector generation also restricts the rectifier voltage vector for current regulation at the PWM rectifier operation start even under the unloaded condition. Hence it has the same effect with a low DC link voltage and generates an uncontrolled PWM rectifier current.

A new start-up current control method that avoids the uncontrolled input phase currents caused by a low DC link

voltage or a low rectifier voltage vector is proposed in this paper. The proposed controller charges the DC-link capacitor up to a certain level for stable conventional rectifier operation by regulating only one phase current like a two-phase rectifier.
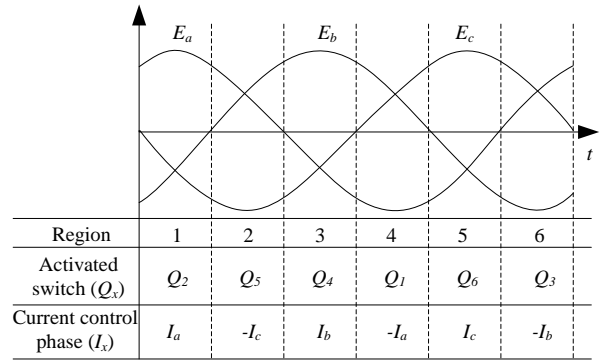

Region	1	2	3	4	5	6
Activated switch (Q_x)	Q_2	Q_5	Q_4	Q_1	Q_6	Q_3
Current control phase (I_x)	I_a	$-I_c$	I_b	$-I_a$	I_c	$-I_b$

Fig. 6. Current control regions and fixed switch based on the input line voltage

IV. PROPOSED START-UP CURRENT CONTROL SCHEME

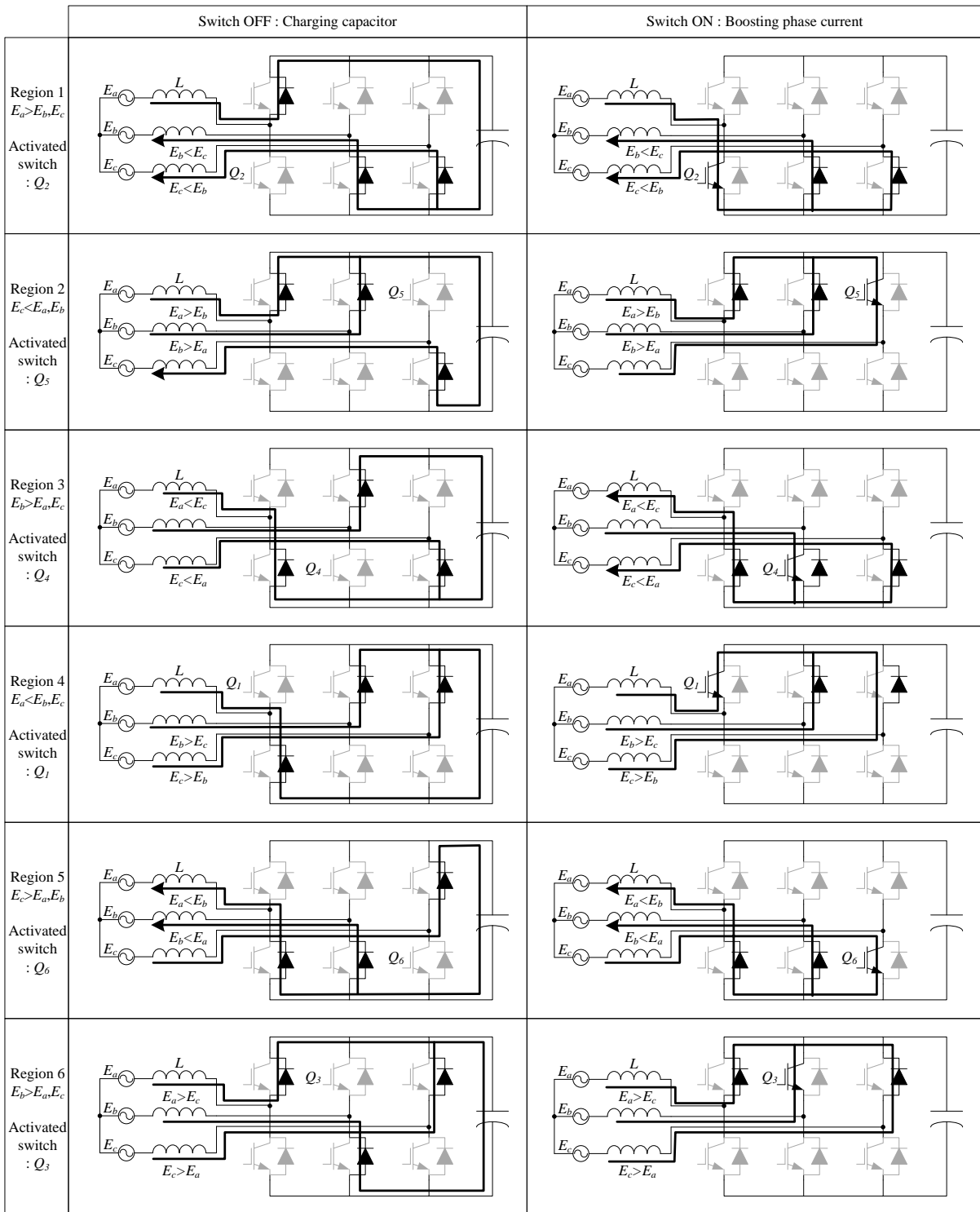| Switch OFF : Charging capacitor	Switch ON : Boosting phase current
Region 1 $E_a>E_b,E_c$ Activated switch : Q_2	
Region 2 $E_c<E_a,E_b$ Activated switch : Q_5	
Region 3 $E_b>E_a,E_c$ Activated switch : Q_4	
Region 4 $E_a<E_b,E_c$ Activated switch : Q_1	
Region 5 $E_c>E_a,E_b$ Activated switch : Q_6	
Region 6 $E_b>E_a,E_c$ Activated switch : Q_3	

Fig. 7. Switch on and off current flow at every region with proposed method.

If the load consumes the DC-link energy from the diode rectifier, the input AC current flows mostly through the two phases having the largest and the smallest voltage magnitude among the three phases. In the proposed current control scheme, only the two phases input lines are controlled, which is like the diode rectifier. The control regions are divided and only one switch is fixed as a control factor based on the grid voltage. Fig. 6 shows the proposed controller's divided region, the control target phase, and the fixed switch for the controller output. In region 1, the proposed controller regulates the a-phase current
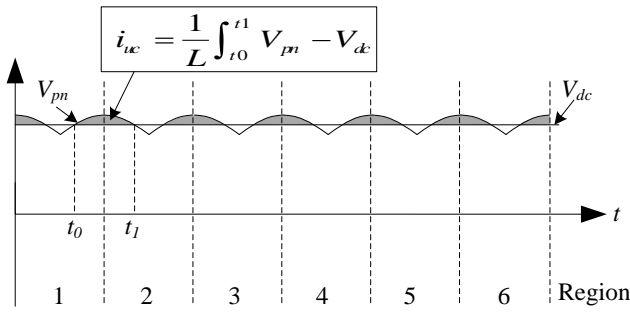
Fig. 8. Plots of V_{pn}, V_{dc}, and i_{uc}.

by turning on and off Q_2. The a-phase current passes from a to b in the first half cycle of region 1 and to c in the second half cycle of region 1. Fig. 7 shows the current flow in each region with the proposed control method. Considering the two phases, the PWM rectifier dynamics are given by:

$$2L\frac{di_x}{dt} = -V_x + V_{pn}, \tag{8}$$

$$\text{where } V_x = (1-d_x)V_{dc},$$

where V_x, i_x, and d_x denote the rectifier control output voltage by switching, the control target phase current, and the duty ratio, respectively. x is defined in Fig. 6. V_{pn} denotes the peak to peak of the input AC voltage. V_{pn} is obtained as follows:

$$V_{pn} = \sqrt{3}V_p \cos\left(\omega t - \frac{\pi}{6} - \frac{n\pi}{3}\right), \tag{9}$$

$$\text{where } \frac{n\pi}{3\omega} \leq t < \frac{(n+1)\pi}{3\omega}, n = 0,1,2...,$$

To control i_x, the P-controller is applied. Since the proposed current control scheme experiences control target phase changes at every one sixth of a period of the fundamental input voltage frequency, an I-controller cannot be useful due to the error integration.

$$V_x = -k_p(i_x^* - i_x) + V_{pn}(t), \tag{10}$$

where i_x^* denotes the phase current command. Since V_x is the controller output, its maximum value is V_{dc}. V_{pn} can be larger than V_{dc} for a fixed time period, as shown Fig. 5(c). Under this condition, i_x increases and the current controller does not have enough of a voltage margin to suppress it. From (8) and (9), this uncontrolled current i_{uc} is given by:

$$i_{uc} = \frac{1}{L}\int_{t0}^{t1} V_{pn} - V_{dc} dt, \tag{11}$$

$$= \frac{2\sqrt{3V_p^2 - V_{dc}^2}}{L\omega} - \frac{V_{dc}(t_1 - t_0)}{L},$$
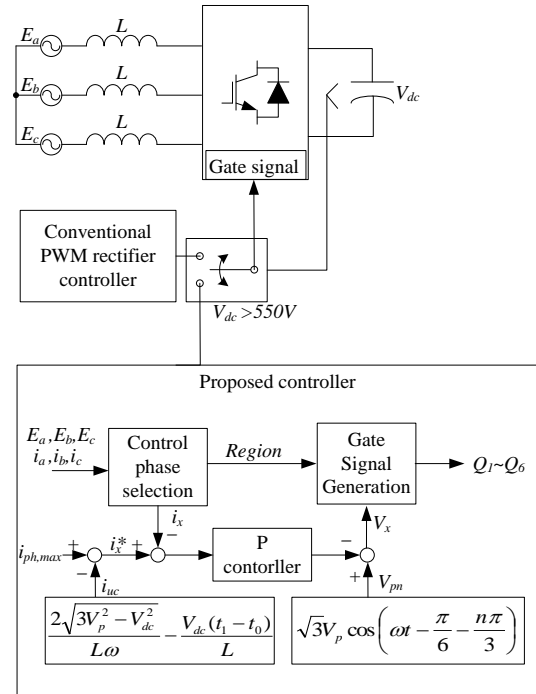

Fig. 9. Block diagram of the proposed control method.

where t_0 and t_1 satisfy $V_{pn}(t_0)=V_{dc}$, $V_{pn}(t_1)=V_{dc}$, $t_0<t_1$ and $\sqrt{3}V_p > V_{dc}$. If V_{dc} is bigger than $\sqrt{3}V_p$, the uncontrolled current does not exist ($i_{uc}=0$). From (9), $t_1 - t_0$ can be obtained as follows

$$i_x^* \leq i_{ph,\max} - i_{uc}$$

$$= i_{ph,\max} + \frac{2}{L\omega}\left[V_{dc}\cos^{-1}\left(\frac{V_{dc}}{\sqrt{3}V_p}\right) - \sqrt{3V_p^2 - V_{dc}^2}\right] \tag{12}$$

The uncontrolled current i_{uc} is the uncontrollable current quantity. Fig. 8 shows plots of V_{pn}, V_{dc}, and i_{uc}. To limit the grid phase current, i_{uc} is added to the current command generation.

$$i_x^* \leq i_{ph,\max} - i_{uc}$$

$$= i_{ph,\max} + \frac{2}{L\omega}\left[V_{dc}\cos^{-1}\left(\frac{V_{dc}}{\sqrt{3}V_p}\right) - \sqrt{3V_p^2 - V_{dc}^2}\right], \tag{13}$$

where $i_{ph,max}$ denotes the phase current limitation value. By considering i_{uc}, the current controller can limit the phase current under the phase current limitation.

Fig. 9 shows a block diagram of the proposed method. When the PWM rectifier starts, the proposed method performs until the DC link voltage increases to a certain level, it set to 550V in this figure.
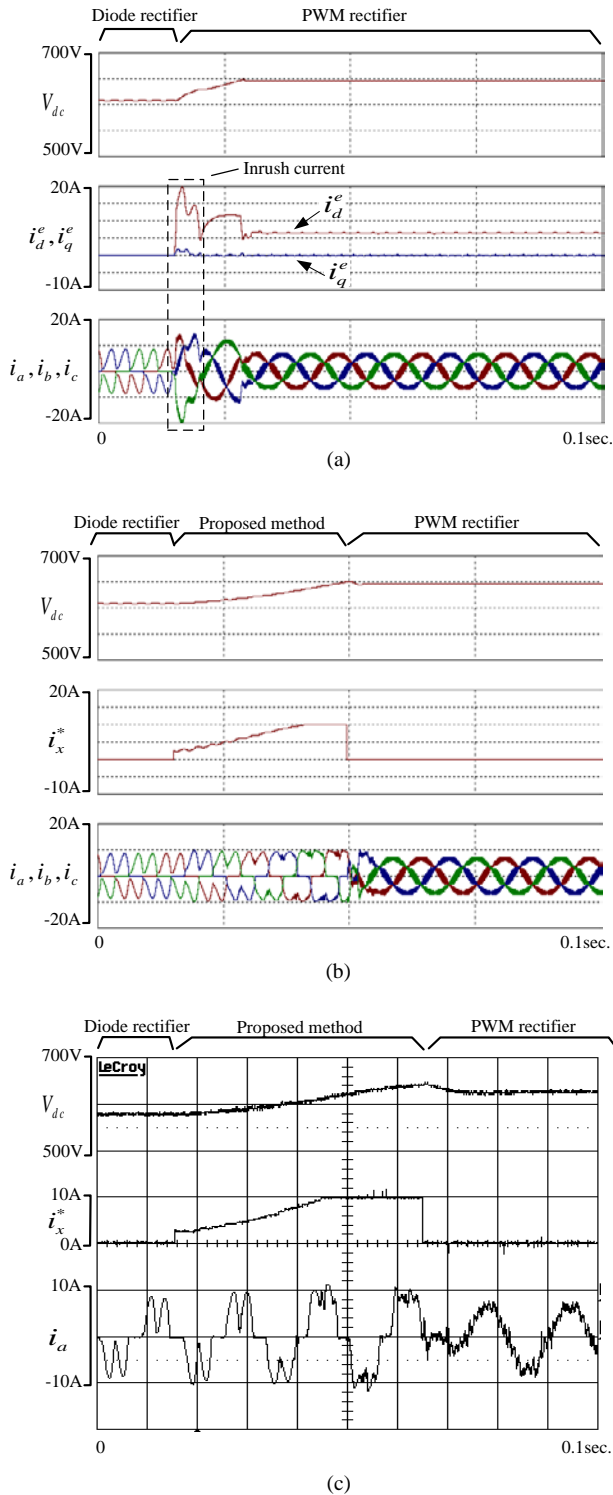
V. EXPERIMENTAL RESULTS

(a)

(b)

(c)

Fig. 10. Simulation and experimental results with resistor load, (a) simulation result with conventional d-q rectifier controller, (b) simulation result with proposed controller, (c) experimental result with the proposed method.

To validate the proposed control method, simulations are carried out. The system parameters are shown in Table 1. Resistors are utilized as a DC link load. The load power is about 2.6kW. Fig. 10(a) shows the simulation results with the conventional rectifier current controller. i_d^e is the control term to charge the DC-link capacitor, and i_q^e is controlled to be zero for a unity power factor. The rectifier starts to operate at $t=15msec$, with $V_{dc} \approx 510V$. For $t<15msec$, the system operates as a diode rectifier. The DC-link voltage is lower than with the unloaded condition. The DC-link voltage is 537V for the unloaded condition. After the PWM rectifier starts to operate, the input phase currents rise and are unregulated until the DC-link voltage rises to a certain level to generate enough of a high voltage vector to regulate them. These unregulated start-up currents might invoke the over current trip and make starting the converter operation difficult.

Fig. 10(b) shows the simulation results with the proposed current controller. From $t=15msec$, the proposed controller starts to operate. $i_{ph,max}$ is set to 10A and i_x^* is set to the maximum value which satisfies $i_x^* = i_{ph,\max} - i_{uc}$. At $t=15msec$, a low DC link voltage makes i_{uc} large which reduces i_x^* by (13). As the DC link voltage increases, i_x^* slowly increases. i_x^* is limited to the constant 10A by $i_{ph,max}$ for $V_{dc} > \sqrt{3}V_p$. When the DC-link capacitor is charged up to 550V, the proposed current controller operation stops and the conventional rectifier controller starts at about $t=50msec$. Since the DC-link voltage is high enough to generated the conventional current controller's output, no unregulated phase currents exist.

Fig. 10(c) shows the experimental results. Since the actual grid voltage is about 365V_{rms}, the initial DC-link voltage is 480V which is lower than in the simulation. After the proposed control method starts at $t=15msec$, the DC-link voltage rises and the phase currents are regulated under 10A. At $t=65msec$, the conventional converter controller starts to operate. Due to a low input voltage, the time that the conventional converter controller starts to operate is delayed when compared with the simulation results.

VI. CONCLUSIONS

By utilizing one phase current controller, a method of charging the dc link capacitor to a certain level without current fluctuations or overcurrent problems is proposed. Simulation results support the performance of the proposed scheme. The proposed method has been shown to be a stable current control scheme in terms of the rectifier start problems caused by a low available rectifier voltage vector as well as a low initial DC link voltage.

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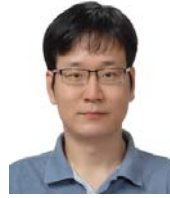
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