JPE-12-4-14

http://dx.doi.org/10.6113/JPE.2012.12.4.643

Analysis, Design and Implementation of an Interleaved DC/DC Converter with Series-Connected Transformers

Bor-Ren Lin† and Chih-Chieh Chen *

†*Dept. of Electrical Eng., National Yunlin University of Science and Technology, Yunlin, Taiwan

Abstract

An interleaved DC/DC converter with series-connected transformers is presented to implement the features of zero voltage switching (ZVS), load current sharing and ripple current reduction. The proposed converter includes two half-bridge converter cells connected in series to reduce the voltage stress of the switches at one-half of the input voltage. The output sides of the two converter cells with interleaved pulse-width modulation are connected in parallel to reduce the ripple current at the output capacitor and to achieve load current sharing. Therefore, the size of the output chokes and the capacitor can be reduced. The output capacitances of the MOSFETs and the resonant inductances are resonant at the transition instant to achieve ZVS turn-on. In addition, the switching losses on the power switches are reduced. Finally, experiments on a laboratory prototype (24V/40A) are provided to demonstrate the performance of the proposed converter.

Key words: DC Converter, Soft Switching.

I. INTRODUCTION

Power factor correction (PFC) schemes have been widely used in the front stage to reduce reactive power reduction and to eliminate line current harmonics at the utility side. For a three-phase 380V PFC converter, the DC bus voltage may be higher than 600V. Therefore, MOSFETs with 600V of voltage stress cannot be adopted in the second stage DC/DC converter. To overcome this voltage limitation of MOSFETs, three-level DC/DC converters [1]-[4] have been proposed with more power switches, split capacitors and clamp diodes. Thus the voltage stress of the MOSFETs can be reduced to one-half of the DC bus voltage so that high frequency MOSFETs with 600V of voltage stress can be used in second stage DC/DC converters. However, the main drawbacks of three-level converters are their complicated control schemes and high circuit costs. In addition, high circuit efficiency and high power density are demanded for modern switching mode power supplies. To achieve high circuit efficiency, light weight and a compact size, power converters with soft-switching techniques [5]-[17] have been developed for more than twenty years. Active clamped converters [5]-[8], full-bridge phase-shift converters [9]-[10] and series resonant converters [11]-[13] have been developed to achieve zero voltage switching (ZVS) turn-on for switches. The active-clamping topology is one kind of soft switching technique to achieve ZVS turn-on by utilizing the energy stored in the leakage and magnetizing inductances. Thus the voltage rating of the power switch is clamped to the input voltage and the clamping capacitor voltage. Full-bridge phase-shift converters can achieve soft switching for power switches with a PWM phase shift between the leading and lagging legs. However, it is difficult to realize ZVS turn-on in wide load ranges for MOSFETs in the lagging leg due to the limited energy in the leakage inductance. Resonant converters can regulate the output voltage and realize ZVS turn-on with a variable switching frequency. Although the switches can be turned on with zero voltage switching (ZVS), the disadvantages of the resonant converters are a variable switching frequency and high voltage or current stresses on the power semiconductors. This is especially true for high voltage or high current applications. Asymmetrical pulse-width modulation (PWM) [14]-[15] has been proposed to realize the magnetizing flux reset. Thus the voltage spike on power MOSFETs can be reduced to a safety region.

Manuscript received Jan. 5, 2012; revised May 2, 2012
Recommended for publication by Associate Editor Honnyong Cha.
†Corresponding Author: linbr@yuntech.edu.tw
Tel: +886-5-5517456, Fax: +886-5-5312065, Nat'l Yunlin Univ. of Sci. and Tech.
*Dept. of Electrical Eng., National Yunlin University of Science and Technology, Taiwan

This paper presents an interleaved DC/DC converter for high input voltage applications. The main advantages of the proposed converter are low switching losses, ZVS turn-on, low voltage stress on the MOSFETs and less ripple current at the output side. Two capacitors and two half-bridge converters are connected in series in the primary side to reduce the voltage stress of the MOSFETs at one-half of the DC bus voltage. The two converter cells are operated with interleaved PWM to reduce the output ripple current. Thus the size of the output chokes and the output capacitor can be reduced. For each of the converter cells, there are two asymmetric half-bridge circuit cells with the same MOSFETs to regulate the output voltage at a desired voltage level. The transformer secondary windings of the two circuits are connected in series to balance the primary winding currents. Thus the size of the transformer core and bobbin is reduced. Based on the resonant behavior by the output capacitance of the MOSFETs and the resonant inductance, the MOSFETs can be turned on under ZVS. The circuit configuration, the principle of operation, the circuit characteristics and a design example of the proposed converter are presented in detail. Experiments with a 960W prototype are presented to verify the effectiveness of the proposed converter.

II. CIRCUIT CONFIGURATION

Fig. 1 gives the circuit configuration of the proposed interleaved DC/DC converter. The input DC bus voltage is obtained from a three-phase 380V AC utility voltage with a diode rectifier. The normal DC input voltage V_{in}=480V~600V. Two input voltages and two half-bridge circuits are connected in series at the high voltage side to reduce the voltage stress of each switch at one half of the DC bus voltage. The output sides of the two half-bridge circuits are connected in parallel to reduce the current rating of the transformer windings and to share the load current. The interleaved PWM scheme is adopted to control the two half-bridge circuits so that the ripple currents of the output inductors are partially cancelled and the size of the output magnetic core is decreased. There are several ways to solve the problem of balancing two input capacitor voltages. Two capacitor voltages can be balanced by a PFC converter with two output voltage balance control or by adding a balanced resistor parallel to each of the input capacitors. Parallel balanced resistors are mostly used in UPS systems with a half-bridge inverter. The components of circuit 1 include V_{in1}, S_1, S_2, C_{r1}, C_{r2}, C_1, C_2, L_{r1}, L_{r2}, T_1, T_2, D_1, D_2 and L_{o1}. Similarly, the components of circuit 2 include V_{in2}, S_3, S_4, C_{r3}, C_{r4}, C_3, C_4, L_{r3}, L_{r4}, T_3, T_4, D_3, D_4 and L_{o2}. C_o and R_o denote the output capacitance and the load resistance. C_1~C_4 are the DC blocking capacitances. The DC blocking voltages V_{C1}~V_{C4} are related to the duty ratio of the active switch. L_{r1}~L_{r4} are the resonant

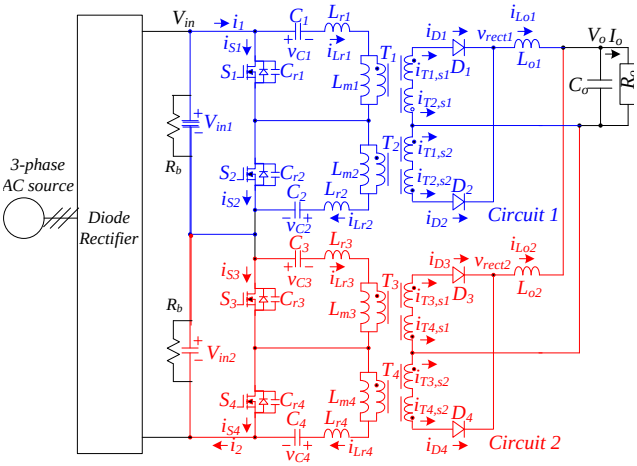


Fig. 1. Circuit configuration of the proposed interleaved converter.

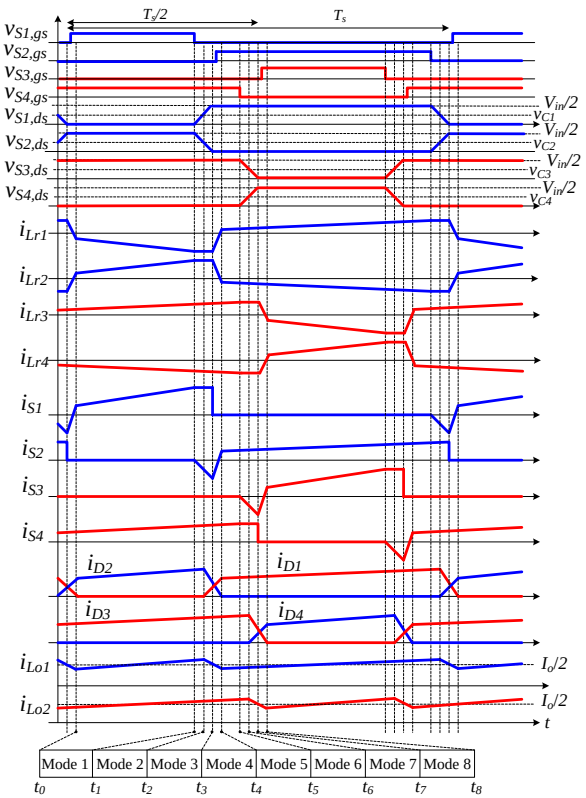


Fig. 2. Key waveforms of the proposed converter.

inductances. L_{m1}~L_{m4} are the magnetizing inductances of the transformers T_1~T_4, respectively. D_1~D_4 are the rectifier diodes and L_{o1} and L_{o2} are output inductances. C_{r1}~C_{r4} are the output capacitances of the MOSFETs S_1~S_4, respectively. To balance the primary currents and to reduce the winding turns of T_1 and T_2, the secondary windings of T_1 and T_2 are connected in series. The voltage stress of S_1~S_4 is clamped to V_{in}/2. The center-tapped rectifier is adopted to have only one diode conduction loss in the secondary side. The PWM

signals of S_1 and S_3 are phase-shifted by about one-half of a switching period to reduce the ripple current at the output capacitor. The gate signals of S_1 and S_2 in circuit 1 are complementary to each other with a dead time to achieve asymmetric PWM operation. In the same manner, the gate signals of S_3 and S_4 in circuit 2 are also complementary. Since the asymmetric PWM scheme is used in the proposed converter, the active switches S_1~S_4 can be turned on under ZVS at the transition interval.

III. Operation Principle

The theoretical waveforms of the proposed converter during one switching cycle are shown in Fig. 2. The duty cycles of S_1 and S_3, are δ, and the duty cycles of S_2 and S_4 are 1-δ. Before the system analysis, the following assumptions are made:

- Input voltages $V_{in1}=V_{in2}=V_{in}/2$;
- The power semiconductors S_1~S_4 and D_1~D_4 are ideal;
- $L_{m1}=L_{m2}=L_{m3}=L_{m4}=L_m$, $L_{r1}=L_{r2}=L_{r3}=L_{r4}=L_r<<L_m$ and $L_{o1}=L_{o2}=L_o$;
- Turns ratio of transformers T_1~T_4 is $n=n_p/n_s$;
- $C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r$ and $C_1=C_2=C_3=C_4=C_c >>C_r$;
- The energy stored in the resonant inductances L_{r1} and L_{r2} is greater than the energy stored in the resonant capacitances C_{r1} and C_{r2} so that the ZVS turn-on of the switches can be achieved.

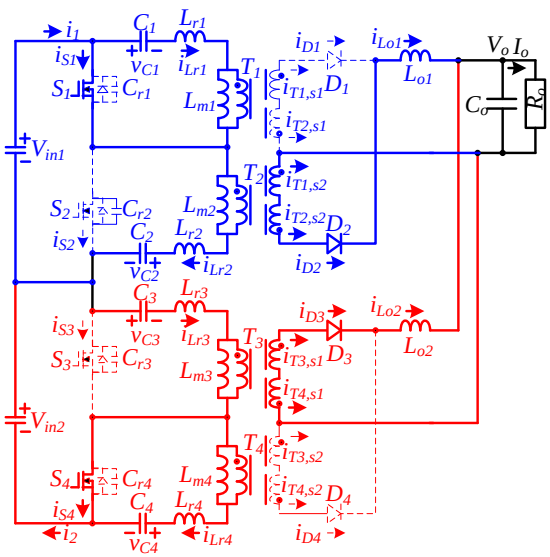
The asymmetric PWM scheme is used to control switches S_1~S_4. The two switch signals S_1 and S_2 are complementary and have a short dead time. In the same manner, switches S_3 and S_4 are also complementary. However, the gate signals of S_1 and S_3 are phase-shifted by one-half of a switching cycle. Based on the on/off states of S_1~S_4 and D_1~D_4, there are sixteen operation modes in a switching period. Since the PWM waveforms of two circuits are symmetrical, eight operation modes in first half cycle are discussed and shown in Fig. 3. Prior to t_0, switches S_1 and S_4 are in the on-state and the rectifier diodes D_1~D_3 are conducting.

***Mode 1* [$t_0 \le t < t_1$]:** At time t_0, $i_{D1}=0$. In this mode, S_1 and S_4 are in the on-state. The primary voltages $v_{Lm1}\approx -V_{C1}<0$, $v_{Lm2}\approx V_{in}/2-V_{C2}>0$, $v_{Lm3}\approx V_{in}/2-V_{C3}>0$ and $v_{Lm4}\approx -V_{C4}<0$. The magnetizing currents i_{Lm1} and i_{Lm4} decrease and the currents i_{Lm2} and i_{Lm3} increase in this mode. In circuit 1, the secondary winding voltages of T_1 and T_2 are negative and positive, respectively so that diode D_2 is forward biased. The inductor voltage $v_{Lo1}=(V_{in}/2-V_{C2}+V_{C1})/n-V_o>0$ so that the inductor current i_{Lo1} increases in this mode. Power is transferred from the input voltage source V_{in1} to the output load through S_1, T_2, L_{r2}, C_2, D_2, and L_{o1}. In circuit 2, the inductor voltage $v_{Lo2}=(V_{in}/2-V_{C3}+V_{C4})/n-V_o>0$ so that the inductor current i_{Lo2} increases in this mode. Power is transferred from V_{in2} to the output load through C_3, L_{r3}, T_3, S_4, D_3 and L_{o2}. This mode ends at time t_1, when S_1 is turned off.

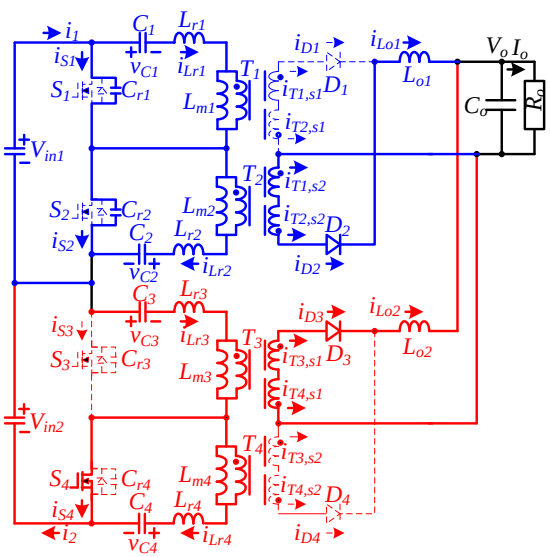
***Mode 2* [$t_1 \le t < t_2$]:** At time t_1, S_1 is turned off. Since $i_{Lr2}-i_{Lr1}>0$, C_{r1} and C_{r2} are charged and discharged, respectively in this mode. Because C_{r1} and C_{r2} << C_1 and C_2, v_{Cr1} and v_{Cr2} are approximately given as:

In this mode, i_{Lr1} and i_{Lr2} are almost constant. The operation behavior of circuit 2 in this mode is the same as the operation in mode 1. This mode ends at time t_2, when $v_{Cr1}=V_{C1}$ and $v_{Cr2}=V_{C2}$.

***Mode 3* [$t_2 \le t < t_3$]:** At time t_2, the capacitor voltages $v_{Cr1}=V_{C1}$ and $v_{Cr2}=V_{C2}$. At this instant, the primary and secondary winding voltages of transformers T_1 and T_2 are zero voltage. Thus diodes D_1 and D_2 are conducting to commutate the inductor current i_{Lo1}. The output inductor voltage $v_{Lo1}=-V_o$ so that the inductor current i_{Lo1} decreases. The diode current i_{D1} increases and the diode current i_{D2} decreases. Capacitors C_{r1} and C_{r2} are continuously charged and discharged in this mode.



(a)



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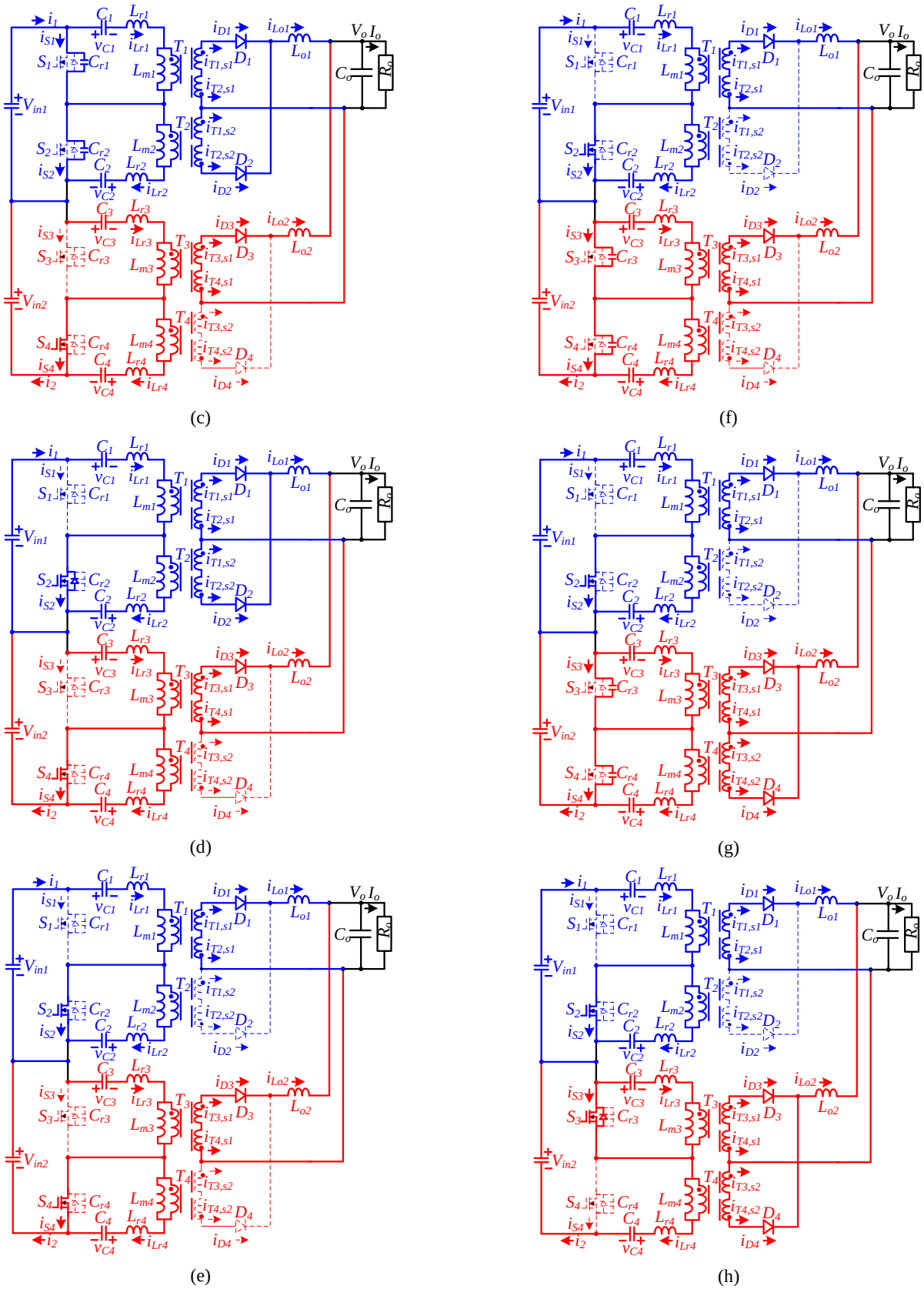


Fig. 3. Operation modes of the proposed converter during first half of switching cycle (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8.

$$v_{Cr1}(t) \approx V_{C1} + \frac{i_{Lr2}(t_2) - i_{Lr1}(t_2)}{2C_r}(t - t_2),$$

$$v_{Cr2}(t) \approx V_{C2} - \frac{i_{Lr2}(t_2) - i_{Lr1}(t_2)}{2C_r}(t - t_2) \quad (2)$$

If the energy stored in L_{r1} and L_{r2} is greater than the energy stored in C_{r1} and C_{r2}, then C_{r2} can be discharged to zero voltage. This mode ends at time t_3, when $v_{Cr2}=0$. Then the anti-parallel diode of S_2 conducts. The time interval in modes 2 and 3 is expressed as:

$$\Delta t_{13} = t_3 - t_1 \approx \frac{C_r V_{in}}{i_{Lr2}(t_1) - i_{Lr1}(t_1)} \quad (3)$$

In order to achieve ZVS turn-on for switch S_2, the dead time t_d between switches S_1 and S_2 must be greater than the time interval Δt_{13}.

Mode 4 **[$t_3 \le t < t_4$]:** At time t_3, $v_{Cr2}=0$. Since $i_{S2}(t_2)=i_{Lr1}(t_2)-i_{Lr2}(t_2)<0$, the anti-parallel diode of S_2 is conducting. Before the switch current i_{S2} becomes positive, S_2 can be turned on under ZVS. Since D_1 and D_2 in the secondary side are still in the commutation interval, the resonant inductor voltages $v_{Lr1}=V_{in}/2-V_{C1}$ and $v_{Lr2}=-V_{C2}$. Thus i_{Lr1} increases and i_{Lr2} decreases in this mode. This mode ends at time t_4 when diode current $i_{D2}=0$. If the load current I_o is equally supplied from two circuits, then the inductor current variation Δi_{Lr1} in this mode is approximately equal to I_o/n. The time interval in this mode is given as:

$$\Delta t_{34} = t_4 - t_3 \approx \frac{L_r I_o}{n(V_{in}/2 - V_{C1})} \quad (4)$$

In this mode, switch S_2 is in the on-state and the inductor voltage $v_{Lo1}=-V_o$. No power is delivered from V_{in1} to the output load. Thus the duty loss of circuit 1 in this mode is given as:

$$\delta_{loss,4} = \frac{\Delta t_{34}}{T_s} \approx \frac{L_r I_o f_s}{n(V_{in}/2 - V_{C1})} \quad (5)$$

where T_s and f_s are the switching period and the switching frequency, respectively.

Mode 5 **[$t_4 \le t < t_5$]:** At time t_4, $i_{D2}=0$ and D_2 is turned off. The magnetizing voltages $v_{Lm1}\approx V_{in}/2-V_{C1}>0$, $v_{Lm2}\approx -V_{C2}<0$, $v_{Lm3}\approx V_{in}/2-V_{C3}>0$ and $v_{Lm4}\approx -V_{C4}<0$. Therefore, the magnetizing currents i_{Lm1} and i_{Lm3} increase and the magnetizing currents i_{Lm2} and i_{Lm4} decrease in this mode. The output inductor voltages $v_{Lo1}=(V_{in}/2-V_{C1}+V_{C2})/n-V_o>0$ and $v_{Lo2}=(V_{in}/2-V_{C3}+V_{C4})/n-V_o>0$. Thus the inductor currents i_{Lo1} and i_{Lo2} increase in this mode. Power is transferred from V_{in1} to the output load through C_1, L_{r1}, T_1, S_2, D_1 and L_{o1} in circuit 1. In the same manner, power is transferred from V_{in2} to the output load through C_3, L_{r3}, T_3, S_4, D_3 and L_{o2} in circuit 2. This mode ends at time t_5, when switch S_4 is turned off.

Mode 6 **[$t_5 \le t < t_6$]:** At time t_5, S_4 is turned off. Since $i_{Lr3}(t_5)-i_{Lr4}(t_5)>0$, capacitors C_{r3} and C_{r4} are discharged and charged, respectively. The capacitor voltages v_{Cr3} and v_{Cr4} are approximately expressed as:

$$v_{Cr3}(t) \approx \frac{V_{in}}{2} - \frac{i_{Lr3}(t_5) - i_{Lr4}(t_5)}{2C_r}(t - t_5),$$

$$v_{Cr4}(t) \approx \frac{i_{Lr3}(t_5) - i_{Lr4}(t_5)}{2C_r}(t - t_5) \quad (6)$$

The inductor currents i_{Lr3} and i_{Lr4} are almost constant in this mode. This mode ends at time t_6, when $v_{Cr3}=V_{C3}$ and $v_{Cr4}=V_{C4}$.

Mode 7 **[$t_6 \le t < t_7$]:** At time t_6, $v_{Cr3}=V_{C3}$ and $v_{Cr4}=V_{C4}$. The primary and secondary winding voltages of T_3 and T_4 are equal to zero voltage. Thus diodes D_3 and D_4 are both conducting to commutate the inductor current i_{Lo2} and the output inductor voltage $v_{Lo2}=-V_o$. The inductor current i_{Lo2} decreases. The diode current i_{D3} decreases and i_{D4} increases. The capacitor voltages v_{Cr3} and v_{Cr4} in this mode are approximately expressed as:

$$v_{Cr3}(t) \approx V_{C3} - \frac{i_{Lr3}(t_6) - i_{Lr4}(t_6)}{2C_r}(t - t_6),$$

$$v_{Cr4}(t) \approx V_{C4} + \frac{i_{Lr3}(t_6) - i_{Lr4}(t_6)}{2C_r}(t - t_6) \quad (7)$$

If the energy stored in L_{r3} and L_{r4} is greater than the energy stored in C_{r3} and C_{r4}, then C_{r3} can be discharged to zero voltage. This mode ends at time t_7, when $v_{Cr3}=0$. The time interval in modes 6 and 7 are expressed as:

$$\Delta t_{57} = t_7 - t_5 \approx \frac{C_r V_{in}}{i_{Lr3}(t_5) - i_{Lr4}(t_5)} \quad (8)$$

In order to turn on S_3 under ZVS, the dead time t_d between switches S_3 and S_4 must be greater than the time interval Δt_{57}.

Mode 8 **[$t_7 \le t < t_8$]:** At time t_7, $v_{Cr3}=0$. Since $i_{S3}(t_7)=i_{Lr4}(t_7)-i_{Lr3}(t_7)<0$, the anti-parallel diode of S_3 is conducting. Before i_{S3} is positive, switch S_3 can be turned on under ZVS. In this mode, diodes D_3 and D_4 in circuit 2 are still in the commutation state. The inductor voltages $v_{Lr3}=-V_{C3}$ and $v_{Lr4}=V_{in}/2-V_{C4}$. Thus the inductor current i_{Lr1} decreases and i_{Lr2} increases. This mode ends at time t_8, when the diode current $i_{D3}=0$. The inductor current variation Δi_{Lr3} is approximately equal to I_o/n. The time interval in this mode is given as:

$$\Delta t_{78} = t_8 - t_7 \approx \frac{L_r I_o}{n V_{C3}} \quad (9)$$

In this mode, switch S_3 is in the on-state and the output inductor voltage $v_{Lo2}=-V_o$. Thus the duty loss of circuit 2 in this mode is given as:

$$\delta_{loss,8} = \frac{\Delta t_{78}}{T_s} \approx \frac{L_r I_o f_s}{n V_{C3}} \quad (10)$$

The operating modes of the proposed converter in the first half of a switching cycle are complete. The operation modes 9-16 of circuit 1 are symmetrical to the operation modes 1-8 of circuit 2. In the same manner, the operation modes 9-16 of circuit 2 are symmetrical to the operation modes 1-8 of circuit 1.

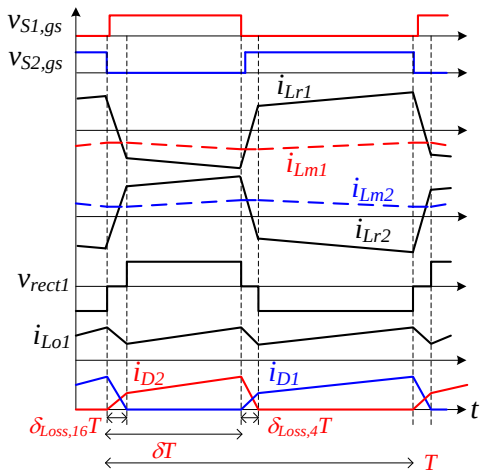


Fig. 4. Main key waveforms of the simplify main operation modes in converter 1.

IV. Circuit Characteristics

Since the transition intervals at the turn-on and turn-off instants are much less than the turn-on time of the power switches, the transition intervals at modes 2, 3, 6, 7, 10, 11, 14 and 15 are neglected in the analysis of the circuit characteristics. However, the effect of the duty cycle losses at modes 4, 8, 12 and 16 needs to be considered when the switch is in the on-state and the rectifier diodes at the secondary side are in the commutation mode. Fig 4 shows the main four operating modes in the circuit during one switching cycle. From the volt-second balance on the primary windings of T_1~T_4, the capacitor voltages V_{C1}~V_{C4} are expressed as:

$$V_{C1}=V_{C3}=\frac{(1-\delta)V_{in}}{2},\quad V_{C2}=V_{C4}=\frac{\delta V_{in}}{2} \tag{11}$$

where δ is the duty cycle of S_1 and S_3. Based on the key waveforms shown in Fig. 4 and the voltage-second balance on the output inductor L_{o1} at steady state, the DC voltage conversion ratio of the proposed converter can be obtained.

$$\frac{V_o+V_f}{V_{in}}=\frac{2\delta-2\delta^2+\delta(\delta_{loss,16}-\delta_{loss,4})-\delta_{loss,16}}{n} \tag{12}$$

where V_f is the voltage drop on diodes D_1~D_4. Since $\delta_{loss,8}=\delta_{loss,16}$, the final output voltage of the proposed converter can be obtained from (5) and (10)-(12).

$$V_o=\frac{2V_{in}}{n}[\delta(1-\delta)-\frac{2L_rI_of_s}{nV_{in}}]-V_f \tag{13}$$

From (13), the output voltage V_o is related to the duty cycle δ, the input voltage V_{in}, the switching frequency f_s, the resonant inductance L_r and the load current I_o. In the steady state, the average output inductor currents I_{Lo1}=I_{Lo2}=I_o/2. The ripple currents on output inductors can be expressed as:

$$\Delta i_{Lo1}=\Delta i_{Lo2}\approx\frac{V_o\delta_{loss,4}T_s}{L_o}=\frac{2V_oL_rI_o}{n\delta V_{in}L_o} \tag{14}$$

The peak currents of L_{o1} and L_{o2} are given as:

$$i_{Lo1,\max}=i_{Lo2,\max}=\frac{I_o}{2}+\frac{V_oL_rI_o}{n\delta V_{in}L_o} \tag{15}$$

Since the average currents on capacitors C_1~C_4 are zero, the average magnetizing currents $I_{Lm,T1}$~$I_{Lm,T4}$ are obtained as:

$$I_{Lm,T1}=I_{Lm,T3}\approx(2\delta\text{-}1)I_o/(2n),\ I_{Lm,T2}=I_{Lm,T4}\approx(1\text{-}2\delta)I_o/(2n) \tag{16}$$

The ripple currents of L_{m1}~L_{m4} can be expressed as:

$$\Delta i_{Lm}\approx\frac{V_{C1}(\delta-\delta_{loss,16})T_s}{L_m}=\frac{\delta(1-\delta)V_{in}T_s}{2L_m}-\frac{L_rI_o}{nL_m} \tag{17}$$

Thus the maximum magnetizing currents can be obtained from (16) and (17).

$$i_{Lm1,\max}=i_{Lm3,\max}=\frac{(2\delta-1)I_o}{2n}+\frac{\delta(1-\delta)V_{in}T_s}{4L_m}-\frac{L_rI_o}{2nL_m},$$

$$i_{Lm2,\max}=i_{Lm4,\max}=\frac{(1-2\delta)I_o}{2n}+\frac{\delta(1-\delta)V_{in}T_s}{4L_m}-\frac{L_rI_o}{2nL_m} \tag{18}$$

The average and root-mean-square (*rms*) currents on the rectifier diodes D_1~D_4 are expressed as:

$$I_{D1,\text{av}}=I_{D3,av}\approx(1-\delta)I_o/2,\quad I_{D2,\text{av}}=I_{D4,av}\approx\delta I_o/2,$$

$$i_{D1,\text{rms}}=i_{D3,rms}\approx\frac{I_o}{2}\sqrt{1-\delta},\ i_{D2,\text{rms}}=i_{D4,rms}\approx\frac{I_o}{2}\sqrt{\delta} \tag{19}$$

In modes 1 and 5, the voltage stresses of rectifier diodes D_1~D_4 can be expressed as:

$$v_{D1,\text{stress}}=v_{D3,\text{stress}}\approx2(1-\delta)V_{in}/n,$$

$$v_{D2,\text{stress}}=v_{D4,\text{stress}}\approx2\delta V_{in}/n \tag{20}$$

The peak current of switch S_1 at time t_1 is approximately expressed as:

$$i_{S1,peak}=i_{S3,peak}\approx i_{Lr2,\max}-i_{Lr1,\min}$$

$$\approx\frac{I_o}{n}+\frac{2V_oL_rI_o}{n^2\delta V_{in}L_o}+\frac{(1-2\delta)I_o}{n}+\frac{\delta(1-\delta)V_{in}T_s}{2L_m}-\frac{L_rI_o}{nL_m} \tag{21}$$

Similarly, the peak currents of S_2 and S_4 are expressed as:

$$i_{S2,peak}=i_{S4,pek}\approx2i_{Lo1,\max}/n+i_{Lm1,\max}-i_{Lm2,\min}$$

$$=\frac{I_o}{n}+\frac{2V_oL_rI_o}{n^2\delta V_{in}L_o}+\frac{(2\delta-1)I_o}{n}+\frac{\delta(1-\delta)V_{in}T_s}{2L_m}-\frac{L_rI_o}{nL_m} \tag{22}$$

The *rms* currents of switches S_1~S_4 can be approximately expressed as:

$$i_{S1,rms}=i_{S3,rms}\approx2(1-\delta)I_o\sqrt{\delta}/n,$$

$$i_{S2,rms}=i_{S4,rms}\approx2\delta I_o\sqrt{1-\delta}/n \tag{23}$$

The voltage stresses of S_1~S_4 are clamped at V_{in}/2. At time t_2 in mode 3, the inductor currents $i_{Lr1}(t_2)$ and $i_{Lr2}(t_2)$ are approximately given as:

$$i_{Lr1}(t_2)=i_{Lr3}(t_{10})=-\frac{i_{Lo1,\max}}{n}+i_{Lm1,\min}$$

$$\approx-\frac{I_o}{2n}-\frac{V_oL_rI_o}{n^2\delta V_{in}L_o}+\frac{(2\delta-1)I_o}{2n}-\frac{\delta(1-\delta)V_{in}T_s}{4L_m}+\frac{L_rI_o}{2nL_m},$$

$$i_{Lr2}(t_2)=i_{Lr4}(t_{10})=\frac{i_{Lo1,\max}}{n}+i_{Lm2,\max}$$

$$\approx\frac{I_o}{2n}+\frac{V_oL_rI_o}{n^2\delta V_{in}L_o}+\frac{(1-2\delta)I_o}{2n}+\frac{\delta(1-\delta)V_{in}T_s}{4L_m}-\frac{L_rI_o}{2nL_m} \tag{24}$$

Similarly the inductor currents $i_{Lr3}(t_6)$ and $i_{Lr4}(t_6)$ in mode 7 are approximately given as:

$$\begin{aligned} i_{Lr3}(t_6) &= i_{Lr1}(t_{14}) = \frac{i_{Lo2,\max}}{n} + i_{Lm3,\max} \\ &\approx \frac{I_o}{2n} + \frac{V_o L_r I_o}{n^2 \delta V_{in} L_o} + \frac{(2\delta - 1) I_o}{2n} + \frac{\delta(1-\delta) V_{in} T_s}{4 L_m} - \frac{L_r I_o}{2 n L_m} \\ i_{Lr4}(t_6) &= i_{Lr2}(t_{14}) = -\frac{i_{Lo2,\max}}{n} + i_{Lm4,\min} \\ &\approx -\frac{I_o}{2n} - \frac{V_o L_r I_o}{n^2 \delta V_{in} L_o} + \frac{(1-2\delta) I_o}{2n} - \frac{\delta(1-\delta) V_{in} T_s}{4 L_m} + \frac{L_r I_o}{2 n L_m} \end{aligned} \quad (25)$$

The ZVS conditions of S_1~S_4 are given in (26).

$$L_{r,S1} \ge \frac{(1-\delta) C_r V_{in}^2}{2[i_{Lr1}^2(t_{14}) + i_{Lr2}^2(t_{14})]}, L_{r,S2} \ge \frac{\delta C_r V_{in}^2}{2[i_{Lr1}^2(t_2) + i_{Lr2}^2(t_2)]},$$

$$L_{r,S3} \ge \frac{(1-\delta) C_r V_{in}^2}{2[i_{Lr3}^2(t_6) + i_{Lr4}^2(t_6)]}, L_{r,S4} \ge \frac{\delta C_r V_{in}^2}{2[i_{Lr3}^2(t_{10}) + i_{Lr4}^2(t_{10})]} \quad (26)$$

Since $i_{Lr3}(t_6)=i_{Lr1}(t_{14})$, $i_{Lr4}(t_6)=i_{Lr2}(t_{14})$, $i_{Lr3}(t_{10})=i_{Lr1}(t_2)$, and $i_{Lr4}(t_{10})=i_{Lr2}(t_2)$, the ZVS condition of S_1~S_4 can be further expressed as:

$$L_r \ge \max\{\frac{\delta C_r V_{in}^2}{2[i_{Lr1}^2(t_2) + i_{Lr2}^2(t_2)]}, \frac{(1-\delta) C_r V_{in}^2}{2[i_{Lr1}^2(t_{14}) + i_{Lr2}^2(t_{14})]}\} \quad (27)$$

V. Design Procedure and Experimental Results

A prototype circuit with the design procedure is presented in this section. The specifications of the prototype circuit are V_{in}=480~580V, V_o=24V, and I_o=40A. The circuit efficiency is assumed to be 90%. The switching frequency of the proposed converter is f_s=100*kHz*. The nominal input terminal voltage $V_{in,nom}$ is 530V. The maximum duty cycle of switches S_1 and S_3 is equal to 0.48 at the minimum input voltage V_{in}=480*V* and the full load condition. The maximum duty cycle loss in modes 4 and 16 is assumed 15% under a full load with a duty cycle δ=*0.5*.

$$\delta_{loss} = \delta_{loss,4} + \delta_{loss,16} \approx \frac{8 I_o L_r f_s}{n V_{in}} \approx \frac{16 P_o L_r f_s}{\eta V_{in}^2} < 0.15 \quad (28)$$

From (29), the resonant inductance of L_r can be obtained as :

$$L_r < \frac{\eta V_{in,\min}^2 \delta_{loss}}{16 P_o f_s} = \frac{0.9 \times 480^2 \times 0.15}{16 \times 960 \times 100000} \approx 20.25 \mu H \quad (29)$$

The actual resonant inductance L_r=18μH is used in the prototype circuit. From (13), the turns ratio of T_1~T_4 is obtained as:

$$\begin{aligned} n \approx [&\delta_{\max}(1-\delta_{\max}) V_{in,\min} + \\ &\sqrt{[\delta_{\max}(1-\delta_{\max}) V_{in,\min}]^2 - 4(V_o + V_f) I_o L_r f_f}\,] \\ &/(V_o + V_f) \approx 8.315 \end{aligned} \quad (30)$$

where V_f=0.65V. A TDK EER-42 magnetic core with A_e=1.94cm^2 was used to design the transformers T_1 ~T_4. The primary turns of T_1~T_4 with ΔB=0.2T are given as:

$$N_{p,\min} \ge \frac{V_{C1}\delta}{A_e \Delta B f_s} = \frac{\delta_{\max}(1-\delta_{\max}) V_{in}/2}{A_e \Delta B f_s} \approx 15.4 \quad (31)$$

In the prototype circuit, the primary winding turns n_p=*25* and the secondary winding turns n_s=*3*. It is assumed that the magnetizing ripple current on L_m is 0.7A. The magnetizing inductacne can be obtained from (17).

$$L_m = \frac{\delta_{\max}(1-\delta_{\max}) V_{in,\min} T_s - \frac{2 L_r I_o}{n}}{2 \Delta i_{Lm}} \approx 733` \mu H \quad (32)$$

The actual magnetizing inductance L_m of T_1~T_4 in the prototype circuit is 750μH. From (13), the minimum duty cycle at the maximum input voltage and the full load condition is obtained as:

$$\delta_{\min} = \frac{1 - \sqrt{1 - \frac{2n(V_o + V_f)}{V_{in,\max}} - \frac{8 L_r I_o f_s}{n V_{in,\max}}}}{2} \approx 0.29 \quad (33)$$

In (14), the ripple current on L_{o1} and L_{o2} is set to 10%. Thus the output inductances L_{o1} and L_{o2} can be obtained as:

$$L_o \ge \frac{2 V_o L_r I_o}{n \delta_{\max} V_{in,\min} \Delta i_{Lo}} \approx 9 \mu H \quad (34)$$

The actual output filter inductance L_o=L_{o2}=L_{o1}=20μH. Based on (19) and (20), the average currents and the voltage stresses on the rectifier diodes are given as:

$$\begin{aligned} I_{D1,\text{av}} &= I_{D3,av} = (1-\delta_{\min}) I_o / 2 = 14.2A, \\ I_{D2,\text{av}} &= I_{D4,av} = \delta_{\max} I_o / 2 = 9.6A, \\ v_{D1,\text{stress}} &= v_{D3,\text{stress}} = 2(1-\delta_{\min}) V_{in,\max} / n \approx 98.8V, \\ v_{D2,\text{stress}} &= v_{D4,\text{stress}} = 2\delta_{\max} V_{in,\min} / n \approx 66.8V \end{aligned} \quad (35)$$

U30D20C diodes with V_{RRM}=200V and I_F=30A are used for D_1~D_4 at the secondary side. Based on (24), the *rms* currents and the voltage stress of S_1~S_4 are given as:

$$\begin{aligned} i_{S1,rms} &= i_{S3,rms} \approx 2(1-\delta_{\min}) I_o \sqrt{\delta_{\min}} / n \approx 3.67A, \\ i_{S2,rms} &= i_{S4,rms} \approx 2\delta_{\max} I_o \sqrt{1-\delta_{\max}} / n \approx 3.32A, \\ v_{S1,stress} &= v_{S2,stress} = v_{S3,stress} = v_{S4,stress} = V_{in,\max}/2 = 290V \end{aligned} \quad (36)$$

In the prototype circuit, IRFP460 MOSFETs with V_{DS}=500V, $I_{D,rms}$=20A, $R_{DS,on}$=0.27Ω and C_{oss}=480pF at 25V are used for switches S_1~S_4. In the proposed circuit, the power switches S_1~S_4 are desinged to have ZVS operation from 50% load to the full load condition under a nominal input voltage. The duty cycle at 50% load and the nominal input voltage can be given as:

$$\delta_{50\%} = \frac{1 - \sqrt{1 - \frac{2n(V_o + V_f)}{V_{in,nom}} - \frac{8 L_r I_{o,50\%} f_s}{n V_{in,nom}}}}{2} \approx 0.3 \quad (37)$$

The output capacitance C_{oss} of the IRFP460 MOSFETs is 480pF at 25V. The equivalent output capacitance C_r at V_{in}=530*V* is given as:

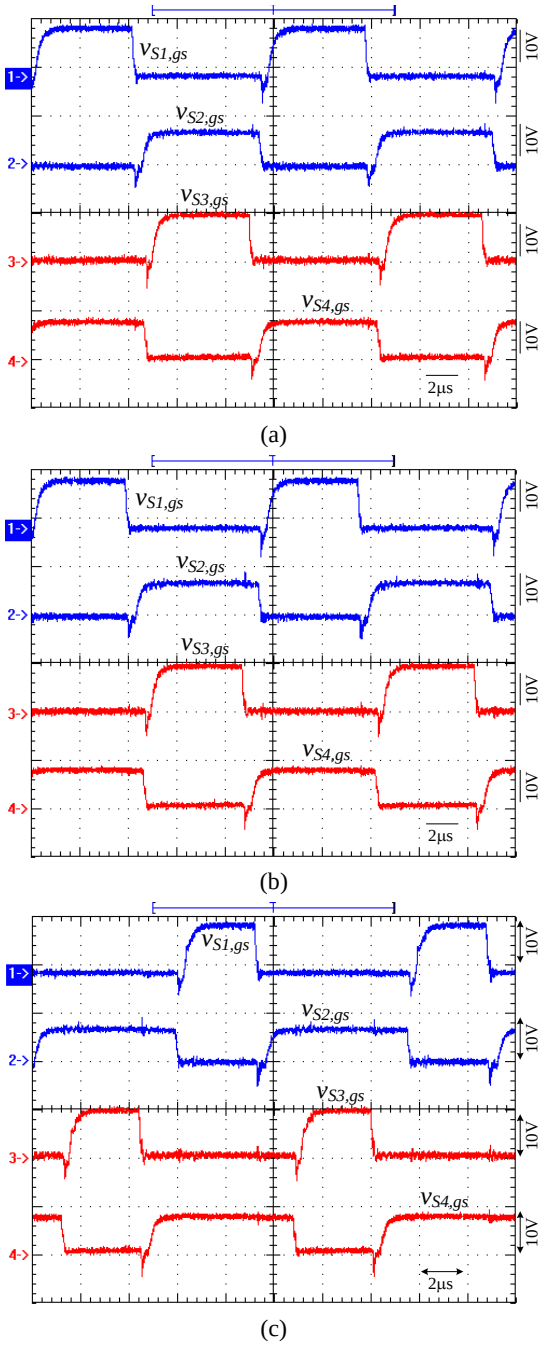


Fig. 5. Measured waveforms of the switch gate-to-source voltages at full load and (a) V_{in}=480V (b) V_{in}=530V (c) V_{in}=580V.

$$C_r \approx \frac{4}{3}C_{oss,25}\sqrt{\frac{25}{v_{S1,ds}}} = \frac{4}{3}\times 480\times\sqrt{\frac{25}{530/2}} \approx 197\,pF \quad (38)$$

From (24) and (25), the inductor currents $i_{Lr1}(t_2)$, $i_{Lr2}(t_2)$, $i_{Lr1}(t_{14})$ and $i_{Lr2}(t_{14})$, at 50% load and $\delta_{50\%}$=0.3 can be obtained as:

$$\begin{aligned}
i_{Lr1}(t_2) &= -\frac{I_{o,50\%}}{2n} - \frac{V_o L_r I_{o,50\%}}{n^2\delta_{50\%}V_{in,nom}L_o} + \frac{(2\delta_{50\%}-1)I_{o,50\%}}{2n} \\
&- \frac{\delta_{50\%}(1-\delta_{50\%})V_{in,nom}T_s}{4L_m} + \frac{L_r I_{o,50\%}}{2nL_m} \approx -2.06A \\
i_{Lr2}(t_2) &= \frac{I_{o,50\%}}{2n} + \frac{V_o L_r I_{o,50\%}}{n^2\delta_{50\%}V_{in,nom}L_o} + \frac{(1-2\delta_{50\%})I_{o,50\%}}{2n} \\
&+ \frac{\delta_{50\%}(1-\delta_{50\%})V_{in,nom}T_s}{4L_m} - \frac{L_r I_{o,50\%}}{2nL_m} \approx 2.02A \\
i_{Lr1}(t_{14}) &= \frac{I_{o,50\%}}{2n} + \frac{V_o L_r I_{o,50\%}}{n^2\delta_{50\%}V_{in,nom}L_o} + \frac{(2\delta_{50\%}-1)I_{o,50\%}}{2n} \\
&+ \frac{\delta_{50\%}(1-\delta_{50\%})V_{in,nom}T_s}{4L_m} - \frac{L_r I_{o,50\%}}{2nL_m} \approx 1.1A \\
i_{Lr2}(t_{14}) &= -\frac{I_{o,50\%}}{2n} - \frac{V_o L_r I_{o,50\%}}{n^2\delta_{50\%}V_{in,nom}L_o} + \frac{(1-2\delta_{50\%})I_{o,50\%}}{2n} \\
&- \frac{\delta_{50\%}(1-\delta_{50\%})V_{in,nom}T_s}{4L_m} + \frac{L_r I_{o,50\%}}{2nL_m} \approx -1.1A
\end{aligned} \quad (39)$$

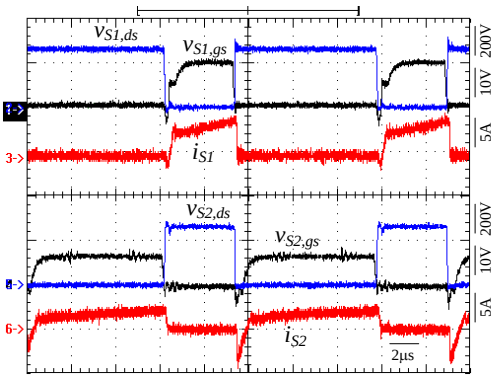
In order to achieve ZVS of S_1~S_4 from 50% load to the full load under a nominal input voltage, the necessary resonant inductance L_r is obtained as:

$$L_r \geq \max\{\frac{\delta_{50\%}C_r V_{in}^2}{2[i_{Lr1}^2(t_2)+i_{Lr2}^2(t_2)]}, \frac{(1-\delta_{50\%})C_r V_{in}^2}{2[i_{Lr1}^2(t_{14})+i_{Lr2}^2(t_{14})]}\} \approx 8\mu\text{H} \quad (40)$$

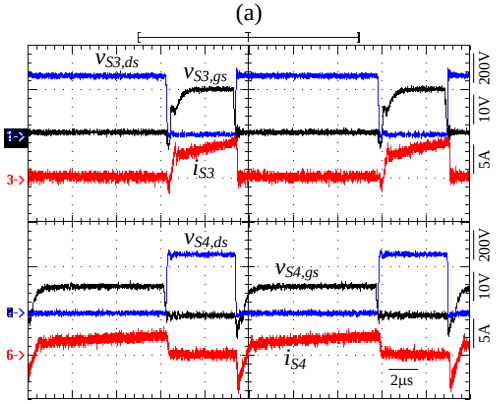
From (29) and (40), the selected resonant inductor L_r=18μH can meet the ZVS condition of S_1~S_4 from the 50% to the 100% load conditions. The selected capacitance of C_1~C_4 is 0.47μF. The capacitance of the output capacitor C_o is 5400μF.

Experimental results with the circuit parameters derived in the previous section were provided to verify the effectiveness of the proposed converter. The measured PWM signals of S_1~S_4 under a full load and different input voltages are shown in Fig. 5. The PWM signals of S_1 and S_3 are phase-shifted by one-half of a switching cycle. Fig. 6 gives the measured gate voltage, the drain voltage and the switch current of switches S_1~S_4 under half and full loads with a nominal input voltage. The drain voltages decreased to zero before switches S_1~S_4 are turned on. Thus, S_1~S_4 are turned on under ZVS from a half load to a full load.

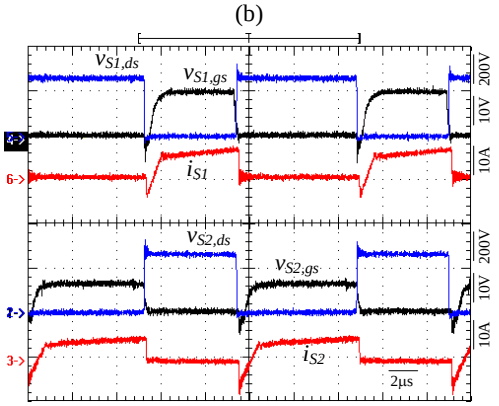
Fig. 7 illustrates the measured waveforms of the inductor currents i_{Lr1}~i_{Lr4} under full load and a nominal input voltage. When switch S_1 is in the on-state, the inductor current i_{Lr1} decreases and i_{Lr2} increases. On the other hand, the inductor current i_{Lr1} increases and i_{Lr2} decreases if switch S_2 is in the on-state. Fig. 8 gives the measured waveforms of v_{C1}, v_{C2}, v_{C3} and v_{C4} under the full load condition. Fig. 9 gives the measured waveforms of $v_{S1,gs}$, i_{D1}, i_{D2} and i_{Lo1} under the full load condition. Fig. 10 shows the experimental results of i_{Lo1}, i_{Lo2} and i_{Lo1}+i_{Lo2} under the full load condition. Fig. 11 shows the measured efficiencies of the proposed converter at



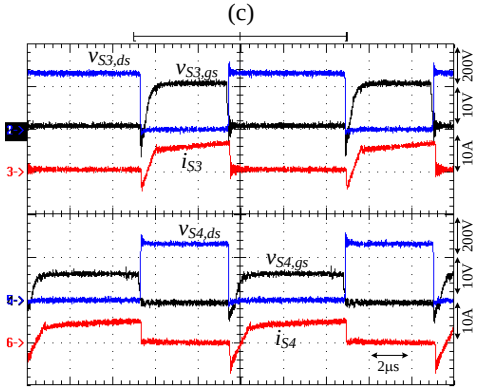
(a)



(b)



(c)



(d)

Fig. 6. Measured waveforms of the gate voltages, drain voltages and switch current at nominal input voltage V_{in}=530V and (a) S_1 and S_2 with 480W load (b) S_3 and S_4 with 480W load (c) S_1 and S_2 with 960W load (d) S_3 and S_4 with 960W load .

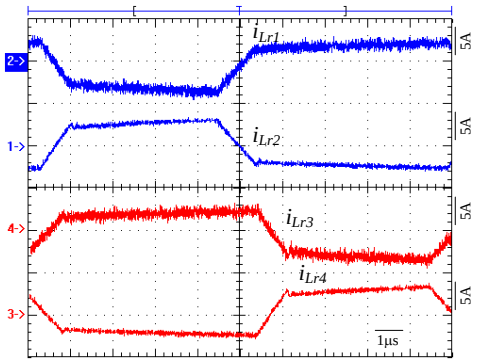


Fig. 7. Measured waveforms of inductor currents i_{Lr1}~i_{Lr4} at full load and nominal input voltage.

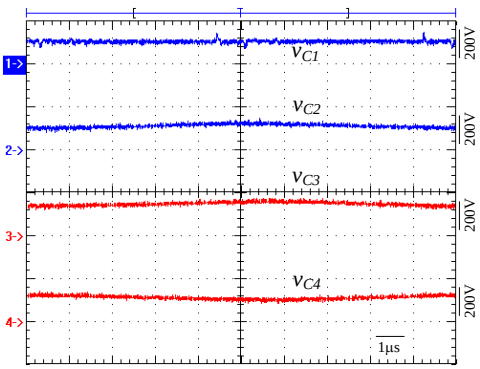


Fig. 8. Measured waveforms of v_{C1}, v_{C2}, v_{C3} and v_{C4} at full load condition.

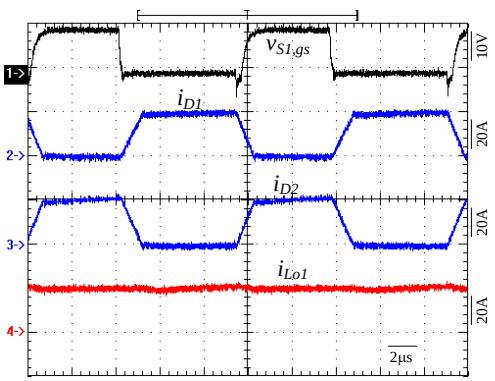


Fig. 9. Measured waveforms of $v_{S1,gs}$, i_{D1}, i_{D2} and i_{Lo1} at full load condition.

VI. CONCLUSION

An interleaved DC/DC converter with series-connected transformers is presented to achieve the following functions: 1) ZVS turn-on for all of the power switches, 2) magnetic flux reset using the asymmetric PWM scheme, 3) low voltage stress of the power switches with a series half-bridge converter, and 4) a low ripple current at the output capacitor with the interleaved PWM scheme. Two split capacitors and

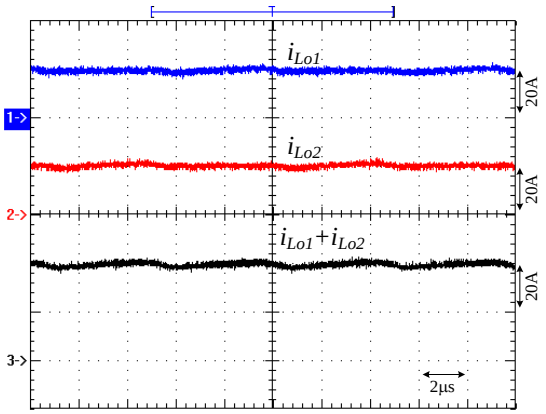


Fig. 10. Experimental results of i_{Lo1}, i_{Lo2} and $i_{Lo1}+i_{Lo2}$ at full load condition.

Fig. 11. Measured efficiencies of the proposed converter at different loads with nominal input voltage condition.

two half-bridge converter circuits connected in series are used in the proposed circuit to limit the voltage stress of the power switches at one-half of the input voltage. Thus the MOSFETs can be used in high input voltage applications to achieve a high switching frequency, a low converter size and a high circuit efficiency. Two half-bridge circuits are operated with the interleaved PWM scheme so that the resulting ripple current at the output capacitor can be partially cancelled. Finally, experimental results are provided to verify the effectiveness of the proposed converter.

ACKNOWLEDGMENT

The project is supported by the National Science Council of Taiwan, ROC, under Grant NSC101-2221-E-224-MY2.

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Bor-Ren Lin received his B.S. in Electronic Engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 1988, and his M.S. and Ph.D. in Electrical Engineering from the University of Missouri, USA, in 1990 and 1993, respectively. From 1991 to 1993, he was a Research Assistant with the Power Electronic Research Center, University of Missouri. Since 1993, he has been with the Department of Electrical Engineering, National Yunlin University of Science and Technology, Douliou, Taiwan, where he is currently a Professor. He has authored more than 200 published technical journal papers in the area of power electronics. His current research interests include power-factor correction, multilevel converters, active power filters, and soft-switching converters. Dr. Lin is an Associate Editor of the IEEE Transactions on Industrial Electronics, The Institution of Engineering and Technology Proceedings—Power Electronics and the Journal of Power Electronics. He was the recipient of Research Excellence Awards in 2004, 2005, 2007 and 2011 from the College of Engineering, National Yunlin University of Science and Technology. He received best paper awards from the IEEE Conference on Industrial Electronics and Applications 2007 and 2011, from the Taiwan Power Electronics 2007 Conference, and from the IEEE Power Electronics and Drive Systems 2009 Conference.

Chih-Chieh Chen is currently working toward his M.S. in Electrical Engineering from the National Yunlin University of Science and Technology, Yunlin, Taiwan (ROC). His current research interests include the design and analysis of power factor correction techniques, switching mode power supplies and soft switching converters.