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Single-Stage Half-Bridge Electronic Ballast Using a Single Coupled Inductor

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Abstract

This paper proposes a single-stage half-bridge electronic ballast with a high power factor using only a single coupled inductor. Compared to conventional high power factor electronic ballasts, the proposed ballast is a simpler circuit with a low cost and a high reliability. The proposed ballast is made up of a power-factor-correction (PFC) circuit and a self-oscillating class-D inverter. The PFC and inverter stages of the proposed ballast are simplified by sharing only a single coupled inductor and two common switches. The proposed PFC circuit can achieve a high power factor and low voltage stresses of the switches. A saturable transformer in the self-oscillating class-D inverter determines the switching frequency of the ballast. Experimental results obtained on a 30W fluorescent lamp are discussed.

Key words: Coupled inductor, Power-factor-correction, Self-oscillating class-D inverter

I. INTRODUCTION

Fluorescent lamps provide a large percentage of today's lighting needs, even though they are considerably larger than incandescent lamps and require a larger fixture. Fluorescent lamps have negative impedance characteristics in the desired operation region. They produce an unstable condition if a tube is connected across a voltage source large enough to cause ionization. Therefore, they cannot be connected directly to a utility line. They require a current-limiting device called a ballast to provide the necessary high voltage for starting the lamp and to limit the lamp current during operation.

Generally, ballasts can be categorized into two major types: electromagnetic ballasts and electronic ballasts [1], [2]. The high frequency electronic ballast has several advantages, such as a higher luminous efficacy, a low audible noise, a long lifetime, an unnoticeable flickering, a small volume, and a light weight. Therefore, electronic ballasts have attracted a great deal of research interest in recent years [3]-[6].

In general, a high power factor electronic ballast can be implemented by using two power processing stages. The input stage, called the preregulator stage, is used to obtain a high power factor while maintaining a constant dc-link voltage. The preregulator stage consists of a full-bridge diode rectifier and a power-factor-correction (PFC) circuit that employs discontinuous conduction mode boost converters [7], [8]. The output stage, which is an inverter, produces a high frequency voltage to drive fluorescent lamps. The gate-drive methods used for the inverter can be largely categorized as the self-oscillating and IC-controlled types. The self-oscillating inverter has been widely used in the electronic ballast market because of its lower component count and greater cost-effectiveness [9].

However, two-stage electronic ballasts have increased costs and reduced reliability. Therefore, single-stage ballasts have attracted a great deal of research interest due to the disadvantages of two-stage electronic ballasts [10]-[18]. Single-stage electronic ballasts that are based on a full-bridge diode and combine the boost converter and inverter have been proposed. The discontinuous boost converters and their modified topologies, including single-stage and two-stage circuits, can achieve a high power factor with a simple control. However, their output voltages should be considerably higher than the peak amplitude of the line voltages. This increases the voltage stress on power semiconductor devices.

The conventional single-stage electronic ballasts require two or more inductors. Two or more inductors increase the volume, the costs and the conduction loss of the ballast. In addition, a large number of inductors makes mass production difficult. Therefore, this small number of circuit components is more

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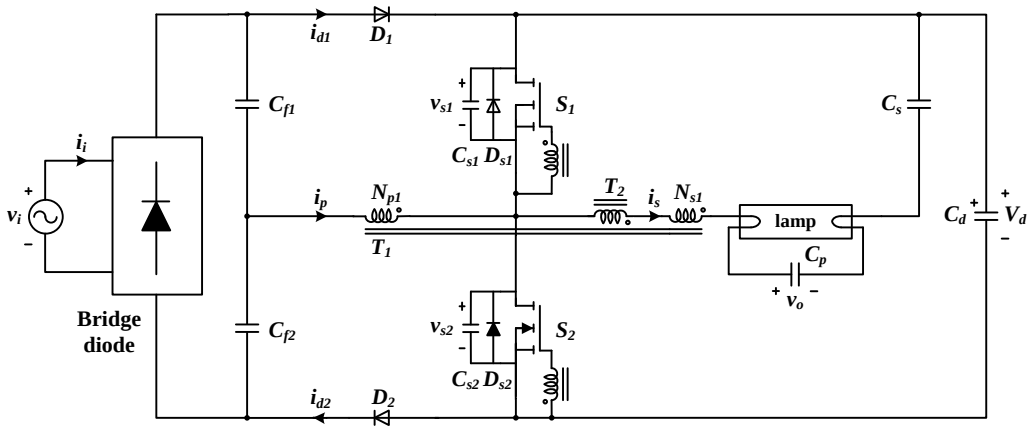

Fig. 1. Proposed single-stage half-bridge electronic ballast.

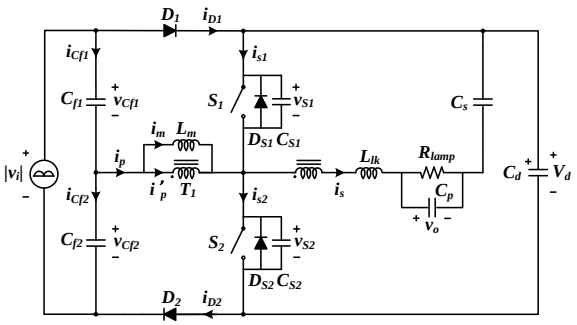

Fig. 2. Equivalent circuit of the proposed ballast at steady- state.

desirable in terms of reliability and cost.

A single-stage half-bridge electronic ballast with a high power factor that uses only a single coupled inductor is proposed, as shown in Fig. 1. The proposed ballast combines the PFC stage and the inverter stage to drive fluorescent lamps. These two stages are simplified by sharing only a single coupled inductor and two common switches. Therefore, when compared to conventional electronic ballasts, the proposed ballast is a simpler circuit with low conduction losses. The proposed PFC stage gives a high power factor, a ripple-free input current, and low voltage stress on the power semiconductor devices. A saturable transformer, which constitutes a self-oscillating class-D inverter, drives the two switches and determines the switching frequency of the ballast. Therefore, the proposed ballast provides a simpler circuit, a lower cost, and a higher reliability than conventional electronic ballasts. Experimental results based on a 30W fluorescent lamp are obtained to show the performance of the proposed ballast.

II. Operational Principle and Analysis

The proposed ballast is shown in Fig. 1. This converter is composed of a PFC circuit and a self-oscillating class-D inverter. Fig. 2 shows an equivalent circuit of the proposed ballast in the steady-state. As can be seen Fig. 2, the coupled inductor T_1 is modeled by an ideal transformer with the magnetizing inductance L_m connected in parallel with the primary winding N_{p1} and the leakage inductance L_{lk} connected in series with the secondary winding N_{s1}. i_{Cf1} and i_{Cf2} are the currents flowing through the filter capacitors C_{f1} and C_{f2} (C_{f1}=C_{f2}=C_f), respectively. The steady-state operation of the proposed ballast includes twelve modes in one switching period T_s, as shown in Fig. 3. Theoretical waveforms are shown in Fig. 4. To illustrate the steady-state operation, several assumptions are made during one switching period T_s. All of the components are assumed to be ideal. The ripple component of the dc-link voltage V_d is negligible, because the dc-link capacitor C_d has a large value. It is assumed that v_i is constant for a switching period T_s. Then, the capacitor current i_{Cf1} is obtained as follows:

$$i_{Cf1} = C_{f1}\frac{dv_{Cf1}}{dt} = C_{f1}\frac{d(v_i - v_{Cf2})}{dt} = -C_{f1}\frac{dv_{Cf2}}{dt} = -i_{Cf2} \quad (1)$$

$$i_{Cf1} = i_{Cf2} + i_p = 0.5i_p \ . \quad (2)$$

Therefore, the same amount of current flows through each of the capacitors. When C_{f1} is charging, C_{f2} is discharging. Conversely, when C_{f2} is charging, C_{f1} is discharging. Since the filter capacitors C_{f1} and C_{f2} have large values, the ripple components of the filter capacitor voltages v_{Cf1} and v_{Cf2} are negligible. Under high frequency operation, the steady-state impedance of the fluorescent lamp can be regarded as a resistor R_{lamp}. Prior to *Mode 1*, the primary current i_p of the coupled inductor T_1 flows through S_2 and D_2 with the positive peak value I_p.

Mode 1 [t_0, t_1]: At t_0, the lower switch S_2 is turned off. Then, i_p starts to discharge C_{S1} connected in parallel with switch S_1 and charge C_{S2} connected in parallel with switch S_2. The voltage v_{S1} across the upper switch S_1 decreases and the voltage v_{S2} across the lower switch S_2 increases. Thus, i_p and the transition interval T_t are given by:

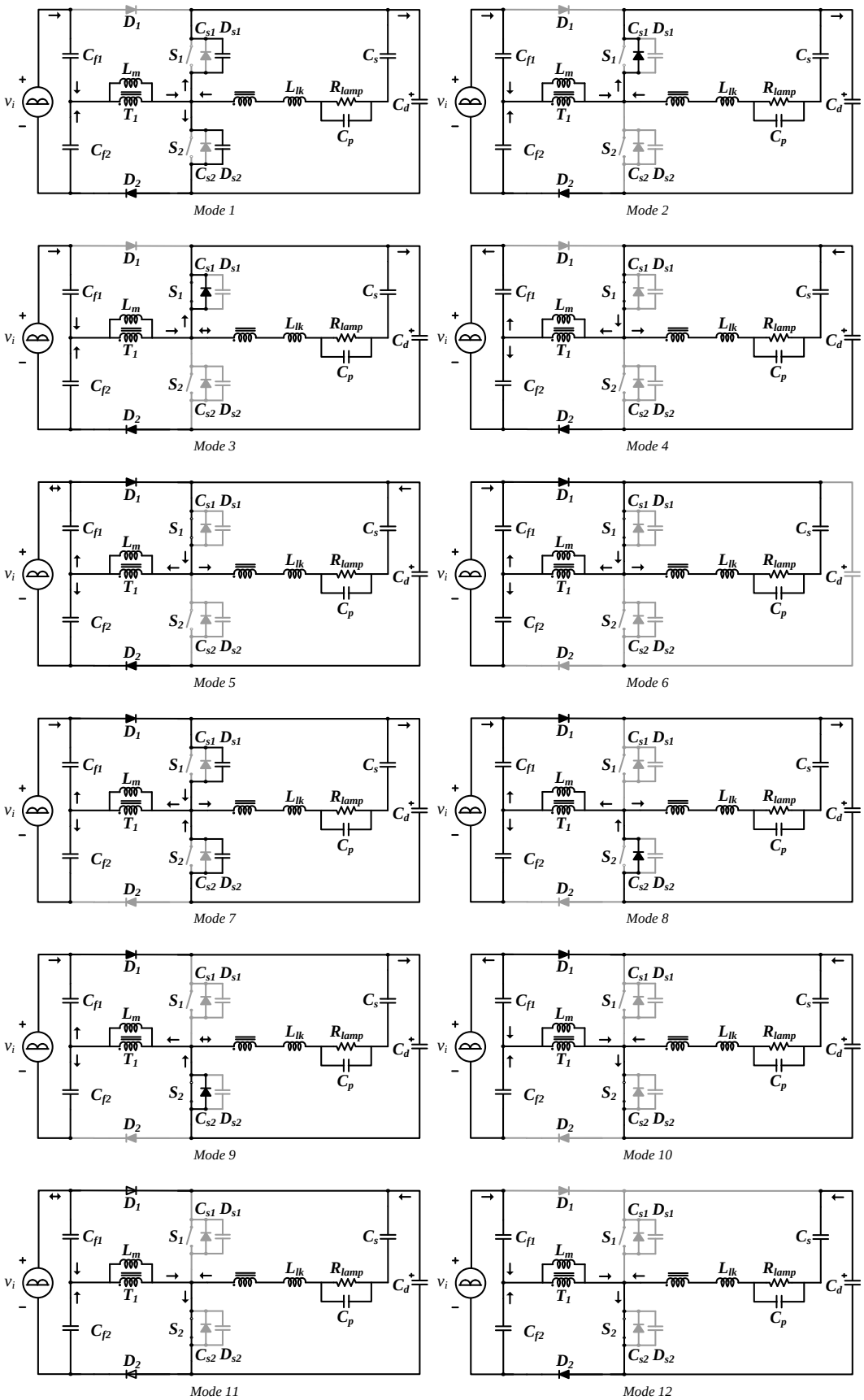

Fig. 3. Operating modes of the proposed ballast.

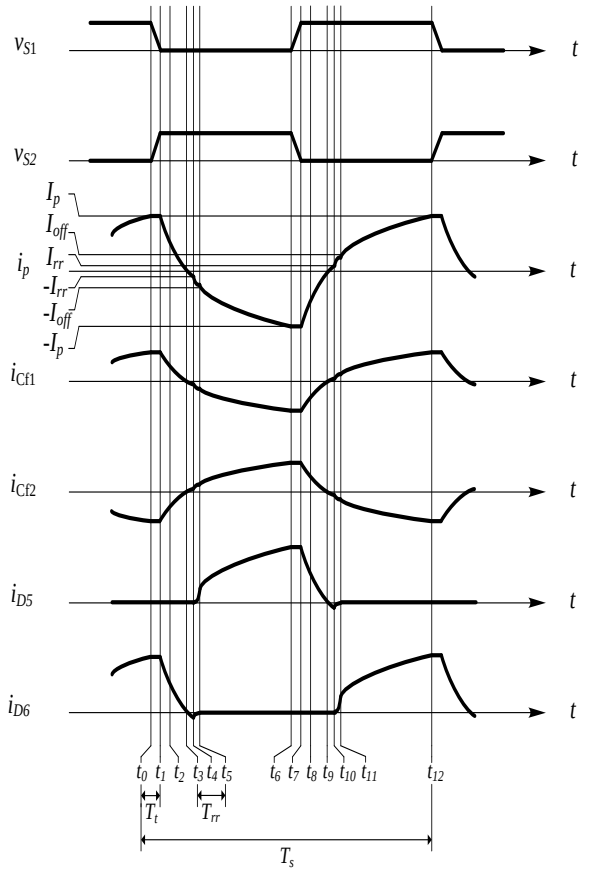

Fig. 4. Theoretical waveforms of the proposed ballast.

$$i_p(t) = I_p \tag{3}$$

$$T_t = \frac{2C_S V_d}{I_p} \ . \tag{4}$$

Since the switch capacitors C_{S1} and C_{S2} (C_{S1}=C_{S2}=C_S) have small capacitances, the transition interval T_t of the switches is negligible. Therefore, i_p has a constant value.

Mode 2 [t_1, t_2]: At t_1, the voltage v_{S1} across the upper switch S_1 becomes zero and the upper diode D_{S1} is turned on. Since the voltage across the primary winding of the coupled inductor T_1 is fixed to $0.5v_i$-V_d, the magnetizing current i_m decreases linearly with the following slope:

$$\frac{di_m}{dt} = -\frac{V_d - 0.5v_i}{Lm} \ . \tag{5}$$

The secondary current i_s begins to resonate by L_{lk}, the parallel resonant capacitor C_p, and the series resonant capacitor C_s. The series-parallel resonant network consisting of L_{lk}, C_s, R_{lamp}, and C_p operates as an inductive load under the steady-state. The parallel resonance disappears due to the small parallel-loaded quality factor. The series-loaded quality factor Q_s of the series-parallel resonant network is given by:

$$Q_s = \frac{1}{R_{lamp}} \sqrt{L_{lk} / C_s} \ . \tag{6}$$

Therefore, the secondary current i_s is obtained as follows:

$$i_s = I_S \sin[\omega_r (t - t_1) - \psi] \tag{7}$$

where I_S is the peak value of i_s. I_S and the phase ψ of the input impedance of the series-resonant circuit are given by:

$$I_S = \frac{2V_d}{\pi Z_r \sqrt{\left(\frac{R_{lamp}}{Z_r}\right)^2 + \left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s}\right)^2}} \tag{8}$$

$$\psi = \cos^{-1} \frac{1}{\sqrt{1 + Q_L^{\,2} \left(\frac{\omega_s}{\omega_r} - \frac{\omega_r}{\omega_s}\right)^2}} \tag{9}$$

where ω_s is the angular switching frequency. The angular resonant frequency ω_r and the resonant impedance Z_r are given by:

$$\omega_r = \frac{1}{\sqrt{LC}}, \ Z_r = \sqrt{\frac{L_{lk}}{C_s}} \ . \tag{10}$$

The secondary current i_s is reflected to the primary current i_p, given by:

$$i_p = i_m - n_1 i_s \tag{11}$$

where the turns ratio n_1 of the coupled inductor T_1 is given by N_{s1}/N_{p1}.

Mode 3 [t_2, t_3]: At t_2, the upper switch S_1 is turned on. The zero-voltage turn-on switching (ZVS) of S_1 is achieved because the current flowed through the upper diode D_{S1} before the upper switch S_1 was turned on. As in *Mode 2*, i_p decreases and approaches zero at the end of *Mode 3*. i_s changes its direction to positive. L_{lk} and C_s continue to resonate, similar to *Mode 2*.

Mode 4 [t_3, t_4]: At t_3, i_p and the diode current i_{d2} are zero. i_{d2} reverses for a reverse-recovery time and the slope of i_p is unchanged. The reverse current reaches its maximum reverse value I_{rr} at the end of *Mode 4*. It is assumed that the reverse current is reduced from zero to $-I_{rr}$ during $0.5T_{rr}$. Then, i_p and the maximum reverse current value I_{rr} are given by:

$$i_p(t) = -\frac{V_d - 0.5v_i}{L_m}(t - t_3) - n_1 i_s(t) \tag{12}$$

$$I_{rr} = \frac{(V_d - 0.5v_i)T_{rr}}{2L_m} + n_1 i_s(t_4) \ . \quad (13)$$

Mode 5 [t_4, t_5]: At t_4, diode D_2 begins to support a reverse voltage and the reverse current begins to decrease. The diode current i_{d2} reaches zero at the end of *Mode 5*. The voltage across the primary winding varies from -(V_d-0.5v_i) to -0.5v_i in *Mode 5*. Then, i_p is given by:

$$i_p(t) = -I_{rr} - \frac{V_d - 0.5v_i}{L_m}(t - t_4) + \frac{V_d - v_i}{L_b T_{rr}}(t - t_4)^2 - n_1 i_s(t) \ . \quad (14)$$

At t_5, i_p approaches -I_{off}, which is the offset current caused by the reverse-recovery of the diode. The offset current I_{off} is given by:

$$I_{off} = \frac{(3V_d - v_i)T_{rr}}{4L_m} + i_s(t_5) \ . \quad (15)$$

Mode 6 [t_5, t_6]: At t_5, since the voltage across the primary winding is fixed to -0.5v_i, the magnetizing current i_m decreases linearly from -I_{off}. I_p arrives at the negative peak value -I_P at the end of *Mode 6*, and the energy is stored by the magnetizing inductance. Therefore, i_p is given by:

$$i_p(t) = -I_{off} - \frac{0.5v_i}{L_m}(t - t_5) - n_1 i_s(t) \ . \quad (16)$$

Mode 7 [t_6, t_7]: At t_6, the upper switch S_1 is turned off and i_p starts to charge C_{S1} and discharge C_{S2}. The upper switch voltage v_{S1} increases and the lower switch voltage v_{S2} decreases. The transition interval T_t of the switch is the same as in *Mode 1*.

Mode 8 [t_7, t_8]: At t_7, v_{S2} becomes zero and diode D_{S2} is turned on. Since the voltage across the primary winding is fixed to V_d-0.5v_i, i_m increases linearly with the following slope:

$$\frac{di_m}{dt} = \frac{V_d - 0.5v_i}{Lm} \ . \quad (17)$$

The series-parallel resonant network resonates similar to *Mode 2*. Therefore, the secondary current i_s is obtained as follows:

$$i_s = -I_S \sin[\omega_r(t - t_7) - \psi] \ . \quad (18)$$

Q_s, I_S, ψ, ω_r, and Z_r are equal to (6), (8), (9), and (10), respectively. The secondary current i_s is reflected to the primary current i_p, and is given by:

$$i_p = i_m + n_1 i_s \ . \quad (19)$$

Mode 9 [t_8, t_9]: At t_8, S_2 is turned on. The ZVS turn-on of S_2 is achieved similar to *Mode 3*. i_m and i_p increase like in *Mode 8*. i_p approaches zero at the end of *Mode 9*. i_s changes its direction to negative. L_{lk} and C_s still resonate similar to *Mode 8*.

Mode 10 [t_9, t_{10}]: At t_9, i_p and the diode current i_{d1} are zero. i_{d1} reverses for a reverse-recovery time and the slope of i_p is unchanged. The reverse current has its maximum reverse value I_{rr} at the end of *Mode 10*. Then, i_m is given by:

$$i_p(t) = \frac{V_d - 0.5v_i}{L_m}(t - t_9) - n_1 i_s(t) \ . \quad (20)$$

Mode 11 [t_{10}, t_{11}]: At t_{10}, diode D_1 begins to support reverse voltage and the reverse current begins to decrease. The diode current i_{d1} arrives at zero at the end of *Mode 11*. As in *Mode 5*, the voltage across the primary winding varies from (V_d-0.5v_i) to 0.5v_i. Then, i_p is given by:

$$i_p(t) = I_{rr} + \frac{V_d - 0.5v_i}{L_m}(t - t_{10}) - \frac{V_d - v_i}{L_b T_{rr}}(t - t_{10})^2 - n_1 i_s(t) \ . \quad (21)$$

Mode 12 [t_{11}, t_{12}]: At t_{11}, since the voltage across the primary winding is fixed to 0.5v_i, i_m increases linearly from I_{off}. I_p arrives at the positive peak value I_P at the end of *Mode 12*. i_p is given by:

$$i_p(t) = I_{off} + \frac{0.5v_i}{L_m}(t - t_{11}) - n_1 i_s(t) \ . \quad (22)$$

III. Self-Oscillating Class-D Inverter

Under high-frequency operation, the series-parallel resonant network operates as an inductive load in the steady-state. If the parallel-loaded quality factor Q_p is high, the ballast output becomes very sensitive to the system parameters [18]. There is no extra conduction loss due to the circulating current as in the case of the parallel resonant circuit [19]. Thus it is desirable to remove the parallel resonance. In an *LC* series resonant circuit, the current flowing through the series resonant circuit will drive the lamp. Consequently, the inverter stage has the inductive load and operates above the resonant frequency. Because of the antiparallel diodes, the switches are turned on at zero voltage and the switching loss at turn-on is negligible.

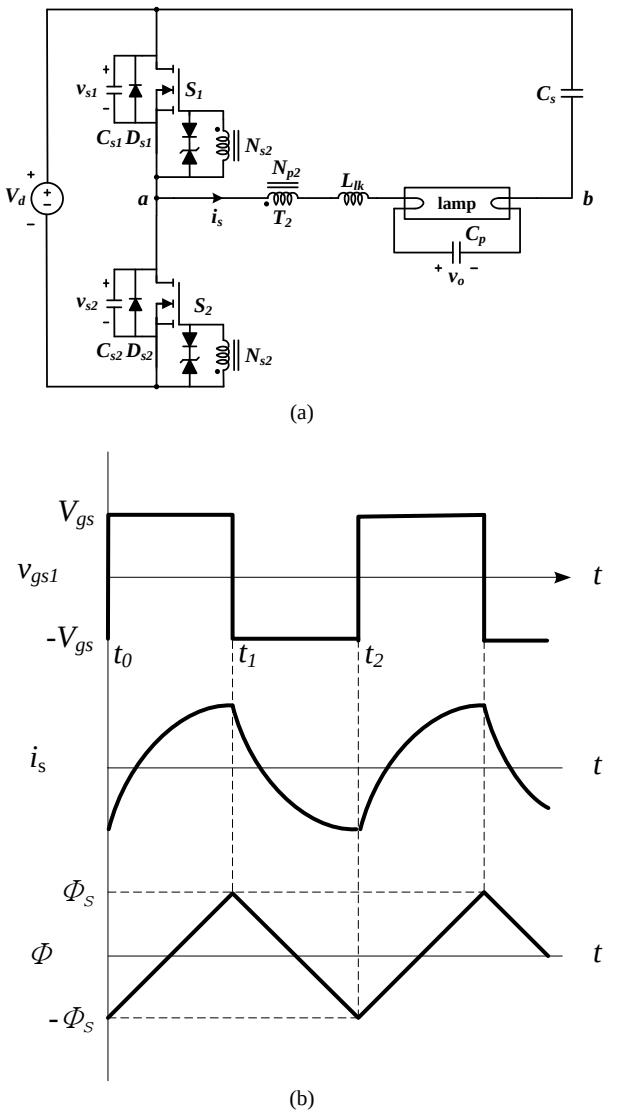

Fig. 5. Inverter stage. (a) Self-oscillating class-D inverter. (b) Waveforms of the self-oscillating class-D inverter.

Before lamp startup, the resistance of the lamp is so high that it can be considered to be an open circuit. Therefore, Q_s is almost zero during the startup. The influence of C_s on the resonant network is so small that it can be ignored. As a result, only the parallel resonance exists during the startup. The series resonance occurs after the ignition of the lamp.

Fig. 5(a) shows the self-oscillating class-D inverter using a saturable transformer T_2. The self-oscillating technique offers circuit simplicity, cost effectiveness, and inherent current-limiting control of the lamp. It also provides shutdown protection in the event of a lamp failure or lamp removal.

TABLE I
PARAMETERS OF THE PROTOTYPE

Parameter/Component	Symbols	Value
Input voltage	v_i	$220V_{rms}$
Filter capacitor	$C_{f1}=C_{f2}$	0.1μF
dc-link capacitor	C_d	10μF
Magnetizing inductance of T_1	L_m	4.6mH
Secondary leakage inductance of T_1	L_{lk}	4.9mH
Primary winding turns of T_1	N_{p1}	100turns
Secondary winding turns of T_1	N_{s1}	150turns
Primary winding turns of T_2	N_{p2}	6turns
Secondary winding turns of T_2	N_{s2}	11turns
Series resonant capacitor	C_s	0.1μF
Parallel resonant capacitor	C_p	1.5nF

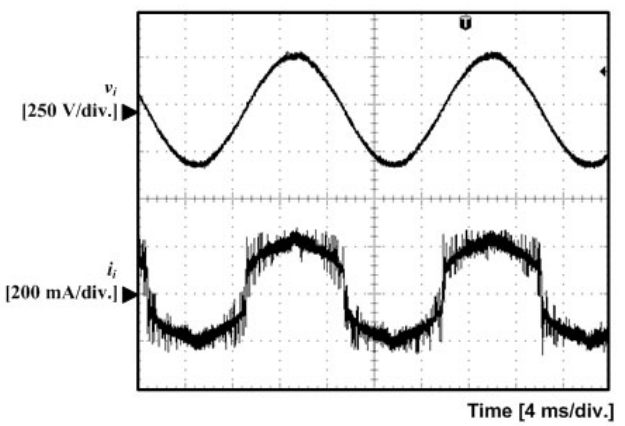

Fig. 6. Experimental waveforms of the input voltage v_i and current i_i.

The proposed electronic ballast is operated by using the self-oscillating drive circuit, which is composed of diodes and the saturable transformer T_2. T_2 is inserted in the resonant path and has three separate windings. The secondary current of T_2 is fed back through the saturable transformer T_2 and converted into a complementary voltage to drive the two switches S_1 and S_2. The switching frequency is determined by T_2. In view of the square hysteresis of the saturable cores, piecewise linear modeling can be adopted for T_2. On the assumption that S_1 is turned on and that the saturable transformer core is not saturated, the flux of the core is increased by the time integral of the voltage. When the core is saturated, the commutation from S_1 to the antiparallel diode of the lower switch S_2 occurs by a resonance between the saturating inductance and the parasitic gate capacitance. The series-parallel resonant network represents an inductive load and the secondary current lags the fundamental component of the voltage v_{ab}.

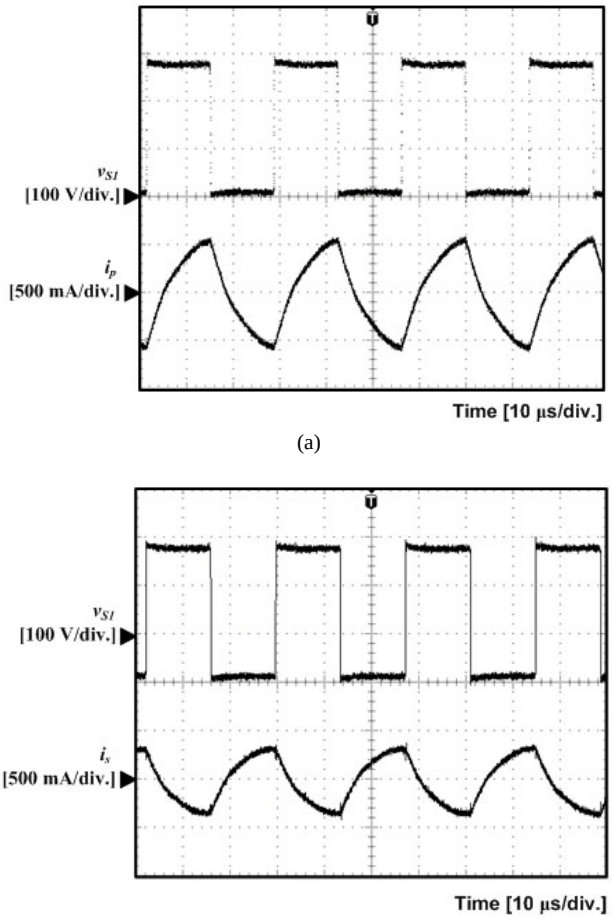

Fig. 7. Experimental waveforms. (a) v_{S1} and i_p. (b) v_{S1} and i_s.

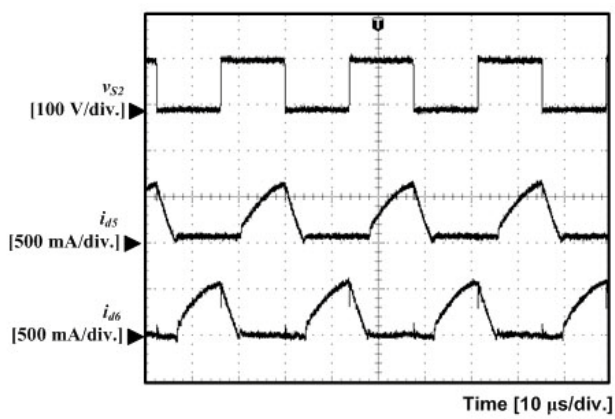

Fig. 8. Experimental waveforms of v_{S2}, i_{d5}, and i_{d6}.

Therefore, when S_1 is turned off, its drain-source voltage v_{S1} increases due to the positive secondary current i_s, causing a decrease in the drain-source voltage v_{S2} of the lower switch S_2. After the positive secondary current discharges the capacitor C_{S2} paralleled with S_2, the antiparallel diode D_{S2} of S_2 is turned on and i_s decreases. If S_2 is turned on before i_s reverses its direction, the ZVS turn-on of S_2 is achieved because the current flowed through the lower diode D_{S2} before S_2 was turned on. S_2 is turned off by a similar operation. Consequently, switch S_1 is complementary to switch S_2. The waveforms of the self-oscillating inverter are shown in Fig. 7(b). The switching frequency f_s is determined by:

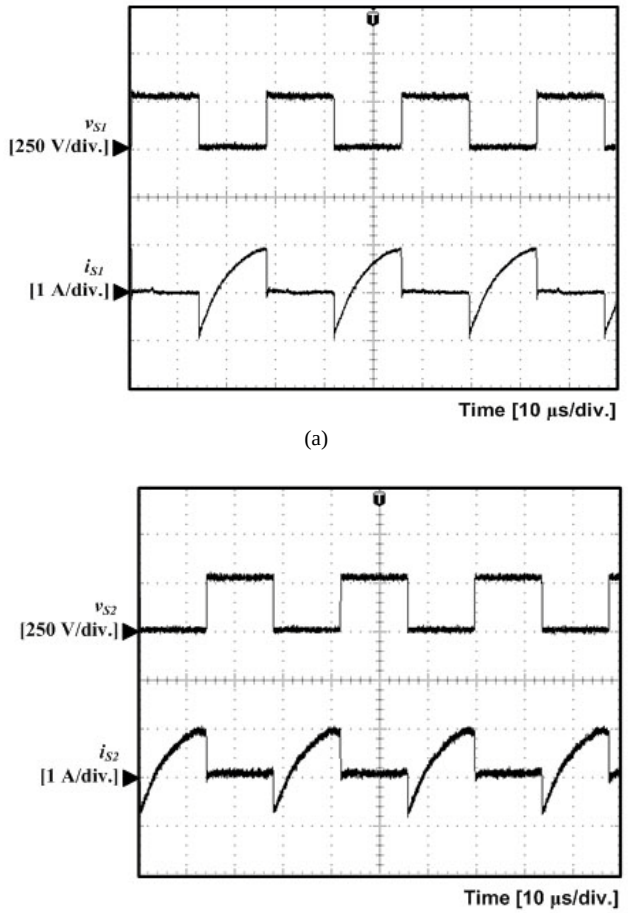

Fig. 9. Experimental waveforms for the ZVS turn-on of the switches. (a) v_{S1} and i_{S1}. (b) v_{S2} and i_{S2}.

$$f_s = \frac{V_{gs}}{4N_{s2}\phi_s} \tag{23}$$

where N_{s2} and Φ_s are the secondary winding turns and the saturation flux of T_2, respectively. v_{gs} denotes the gate voltage, which is given by the sum of the diode drop and the zener voltage, as shown in Fig. 5(a). The switching frequency is determined by v_{gs}, N_{s2}, and Φ_s. The duty ratio becomes 0.5 due to the symmetrical operation.

IV. Experimental Results

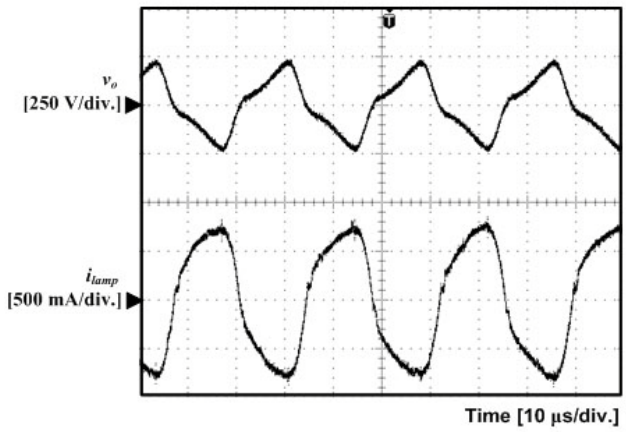

Fig. 10. Experimental waveforms of v_o and i_{lamp}.

The hardware circuit of the proposed electronic ballast in Fig. 1 is implemented for 30W fluorescent lamps. Experiments are carried out to verify the theoretical analysis. The prototype is tested at the ac input voltage of 220V. Table I shows the parameters of the prototype. The switching frequency is 36kHz and the duty ratio is 0.5.

Fig. 6 shows waveforms of the input voltage v_i and the current i_i. The measured power factor is 0.974. Therefore, the proposed electronic ballast gives a high power factor. Fig. 7(a) and (b) show the voltage v_{S1}, the current i_p, and the current i_s. Fig. 8 shows the voltage v_{S2}, the current i_{d5}, and the current i_{d6}. It can be seen that the experimental waveforms agree with the theoretical analysis. Fig. 9(a) and (b) show the voltage and current waveforms of the switches, where it is possible to see that each switch achieved ZVS at the moment of turn-on, assuring low switching losses. Fig. 10 shows the output voltage v_o and the lamp current i_{lamp}. The measured crest factor of i_{lamp} is 1.31.

V. CONCLUSIONS

This paper proposed a single-stage half-bridge electronic ballast with a high power factor using only a single coupled inductor. The PFC and the self-oscillating class-D inverter of the proposed ballast are simplified by sharing only a single coupled inductor and two common switches. Therefore, the proposed ballast is a simple circuit with low conduction losses. The proposed PFC stage gives a high power factor, a ripple-free input current, and low voltage stress on the power semiconductor devices. The secondary current i_s in the inverter stage is fed back through the saturable transformer T_2 and converted into a complementary voltage to drive the two switches. The switching frequency is determined by T_2. Therefore, the proposed electronic ballast provides a simple circuit with a low cost, a high power factor and high reliability when compared to conventional electronic ballasts.

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