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Hybrid Fuzzy PI-Control Scheme for Quasi Multi-Pulse Interline Power Flow Controllers Including the *P*-*Q* Decoupling Feature

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Abstract

Real and reactive power flows on a transmission line interact inherently. This situation degrades power flow controller performance when independent real and reactive power flow regulation is required. In this study, a quasi multi-pulse interline power flow controller (IPFC), consisting of eight six-pulse voltage source converters (VSC) switched at the fundamental frequency is proposed to control real and reactive power flows dynamically on a transmission line in response to a sequence of set-point changes formed by unit-step reference values. It is shown that the proposed hybrid fuzzy-PI commanded IPFC shows better decoupling performance than the parameter optimized PI controllers with analytically calculated feed-forward gains for decoupling. Comparative simulation studies are carried out on a 4-machine 4-bus test power system through a number of case studies. While only the fuzzy inference of the proposed control scheme has been modeled in MATLAB, the power system, converter power circuit, control and calculation blocks have been simulated in PSCAD/EMTDC by interfacing these two packages on-line.

Key words: Decoupled power flow control, FACTS, Hybrid fuzzy-PI controller, Interline power flow controller (IPFC), Multi-pulse converter, Simplex method

I. INTRODUCTION

Flexible alternating current transmission systems (FACTS) have emerged to enhance the controllability and increase the power transfer capacity of power transmission networks [1]. In a deregulated electricity market, FACTS devices are expected to play a very major role in increasing the efficient utilization and control of existing power transmission networks without changing the topology or re-dispatching the generating units [2]. Of the voltage source converter (VSC) based FACTS devices, the interline power flow controller (IPFC), first introduced by Gyugyi et al., is a multi-VSC series FACTS device that can control real and reactive power flows on two or more neighboring transmission lines simultaneously [3]. The dynamic performance of the IPFC suffers from a strong dynamic interaction between the real and reactive power flows due to inherent properties of AC power transmission. To reduce or eliminate this coupling effect, a number of studies on other types of FACTS devices are available in the literature. Firstly, Schauder et al. [4] proposed a *d*-*q* current controller with no-cross coupling for grid connected inverters. Later on, Papic et al. [5] developed a new control scheme originating from [4], in which a decoupled controller with an internal predictive loop for three-level unified power flow controllers (UPFC) was suggested. In the proposed control scheme, the reactance of the series coupling transformer and the system bandwidth are required for gain design. Other articles [6]-[12] proposed different types of decoupled controllers for the non-converter level models of UPFC where an equivalent ideal voltage source model of the UPFC is considered with no harmonics. For example, in [6] a decoupling controller was designed, but the control performance counts on the system parameters and the UPFC model. In [7], a dynamic decoupled compensator for UPFC was designed. The design relies on classical control design techniques which rely on an exact mathematical model of the system. Therefore, the exact damping ratio and the system bandwidth should be known. In [8] a decoupling matrix compensator consisting of four controllers was developed that relies on the ABCD parameters

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of an approximated UPFC model. In [9] a decoupled UPFC controller for dynamic control of the real and reactive power flows was considered. In [13], a UPFC was experimentally validated by 6-pulse VSCs where the pulse width modulation (PWM) switching technique was used. To achieve decoupling, the exact reactance values of the shunt and series coupling transformers should be known.

Most studies on decoupling rely on the parameters of the approximated FACTS device model or the converter-level model of elementary six-pulse VSCs driven by high frequency PWM methods. Hover, these methods are not realistic for high power applications. Therefore, when it comes to realistic IPFC models, such as the multi-pulse or multi-line methods, the literature is not rich.

In this study, the decoupling effect between the real and reactive power flows on a transmission line that is compensated by a quasi multi-pulse IPFC is reduced by a hybrid fuzzy-PI (HFPI) control scheme. The proposed controller is based on a conventional PI controller operating in conjunction with a Mamdani-type fuzzy inference system with linearly distributed linguistic rules. In this way, a fast response has been obtained with a minimal interaction to track the changes in the reference values of the real and reactive power flows. The design phase does not require exact mathematical description or a system transfer function. The PI controller gains are optimized by the simplex method. The fuzzy inference system developed in MATLAB is communicated online with PSCAD/EMTDC which is an efficient time-domain transient simulator for power systems. A module has been prepared in PSCAD/EMTDC to link the MATLAB m-file through FORTRAN scripts written in the module. The two programs exchange information at every time step in a continuous manner. The performance of the proposed HFPI controller is compared with both conventional PI control and PI control with feed-forwarded decoupled gains, which are analytically computed.

II. IPFC CONFIGURATION

The conceptual configuration of a 2-VSC IPFC, located on the two parallel transmission lines (Line-1 and Line-2) of a 4-generator, 4-bus test power system, is shown in Fig. 1. In general, each VSC synthesizes a three-phase controllable voltage such as V_X by employing self-commutative GTO thyristors. $P_{inj1\text{-}2}$ and $Q_{inj1\text{-}2}$ are the real and reactive power injections from VSC1-2 to the power system through the coupling transformers *Tr1-2*, respectively. The common DC link, conceptually represented by capacitor C, enables a real power exchange between the VSCs ($P_{t1\text{-}2}$) so that a set of operating constraints is defined in (1). $P_{loss1\text{-}2}$ is the sum of the switching losses and the coupling transformer losses of VSC1-2, respectively. As long as (1) is satisfied, so that the loss meeting function of the IPFC is assigned to the VSC1,

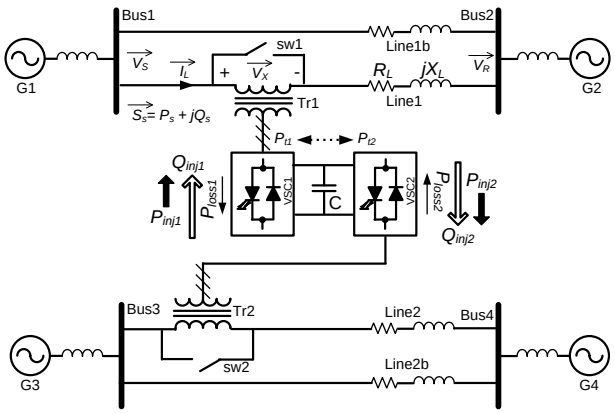


Fig. 1. IPFC configuration and its interaction with power system in terms of real and reactive power injections.

there is no upper limit to the number of series VSCs that can be utilized. Generally, the expression (*2n-1*) satisfies the total number of power system parameters that can be controlled by a *n*-VSCs IPFC. With this in mind, a total of three power system parameters are used for control in this study. These are the real and reactive power flows of Line-2 and the real power flow of Line-1.

$$\left.\begin{aligned} P_{inj1} - P_{t1} - P_{loss1} - P_{loss2} &= 0 \\ P_{inj2} - P_{t2} &= 0 \\ P_{t1} + P_{t2} &= 0 \end{aligned}\right\} \quad (1)$$

A. Quasi Multi-Pulse Converter Design

Each VSC can be constructed by combining four twelve-pulse units that are connected in parallel through their DC link to achieve multi-pulse IPFC operation. The configuration details are shown in Fig. 2. The VSC unit is divided into two groups (Group A and Group B) for the purpose of line frequency switching which will be explained later. Summing transformer for each phase (A-B-C) is used to connect the A1-B1-C1 terminals of Group A with those of Group B, respectively. In another words, it adds the voltage of the respective terminal outputs in series.

In this study, the multi-pulse structure is preferred over the multi-level structure due to advantages mentioned in [14] when back-to-back VSCs for FACTS applications are considered. Fortunately, the quasi multi-pulse configuration can be preferable to the true multi-pulse configurations due to three reasons [15]: 1) the total harmonic distortion (THD) is similar to that of the true 48-pulse one, 2) a simpler design without employing special phase-shifting transformers, 3) lower cost when practical aspects are considered. Fig. 3 shows the details of the twelve-pulse unit comprised of two 2-level six-pulse VSCs.

The switching element is selected as a GTO with an antiparallel diode. The AC terminals of the upper and lower VSC in Fig. 3 are connected in delta and wye configurations with a relative phase shift of 30º, respectively. Three

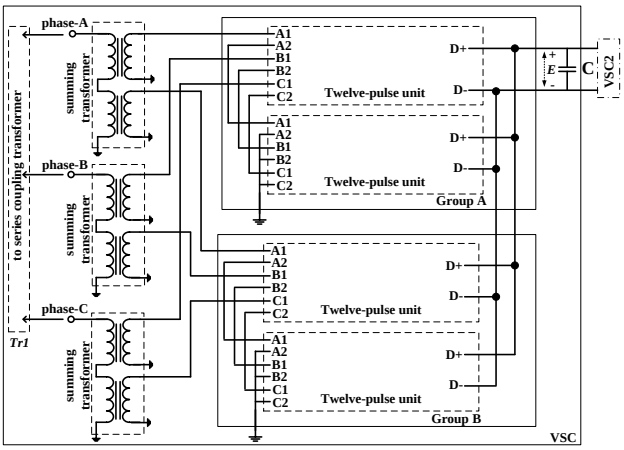


Fig. 2. Quasi-48 pulse configuration of VSC1 of IPFC.

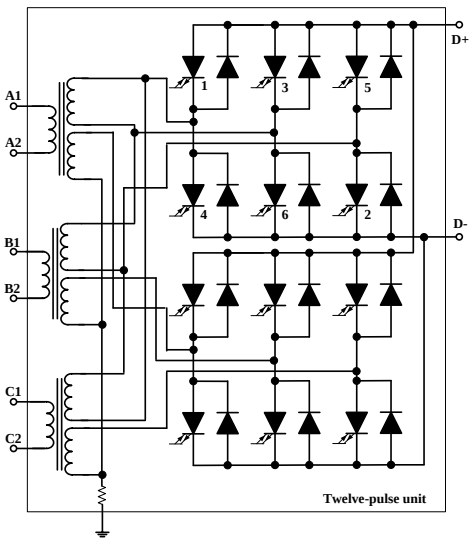


Fig. 3. Circuit details of twelve-pulse unit.

single-phase three-winding transformers are used as a magnetic structure. To achieve 48-pulse operation, each upper side VSC of the four twelve-pulse units is phase shifted by 7.5º. With this in mind, the following phase shifts; 7.5º, 0.0º, -7.5º, and -15º are applied to the gating signal of each twelve-pulse unit.

B. Pulse Generating Circuit

Due to high switching losses, fundamental or line frequency switching is employed where the GTOs are switched only once per cycle to realize multi-pulse operation. Gating signals to the GTOs are provided by 24 (3x8) 50-Hz square-wave generator circuits with the required phase shifts. A block diagram of the pulse generating circuit for the six-pulse VSC is shown in Fig. 4. Conventional phase shifts (0º,-120º, 120º) for producing three-phase voltage waveforms are applied to square-wave generators with the required external phase shifts (*phA* or *phB*) to produce a converter voltage with a desired magnitude and phase angle. These external phase shifts are calculated within the control scheme which will be discussed later.

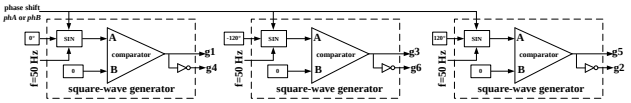


Fig. 4. Pulse generating circuit for six-pulse VSC.

III. IPFC CONTROL STRATEGY

A. Decoupled Controller Design

Assuming the series resistance and inductance of *Tr1* in Fig. 1 are included into the transmission line parameters R_L and X_L, the line current can be derived as:

$$I_L = \frac{V_S - V_R - V_X}{R_L + jX_L} \tag{2}$$

where V_X is the *line-to-neutral* rms voltage phasor of the series injected voltage, V_S and V_R are the line-to-neutral rms voltage phasors of the sending-end and receiving-end sides, respectively. The complex power at the sending-end side is:

$$S_s = P_s + jQ_s = 3V_S I_L{}^* \tag{3}$$

where the symbol (*) denotes the complex conjugate and P_S and Q_S denote the sending-end real and reactive power flows on Line-1, respectively. Assuming that V_R leads V_S by a small angle δ ($\cos\delta\approx1$, $\sin\delta\approx0$), P_S and Q_S can be expressed by the following equation:

$$\begin{bmatrix} P_s \\ Q_s \end{bmatrix} = A\frac{R_L{}^2 + X_L{}^2}{X_L{}^2}\begin{bmatrix} V_Q \\ -V_D \end{bmatrix} + \frac{R_L}{X_L}\begin{bmatrix} Q_s - Q_{s0} \\ -P_s + P_{s0} \end{bmatrix} + \begin{bmatrix} P_{s0} \\ Q_{s0} \end{bmatrix} \tag{4}$$

where $A=3V_S/(R_L+X_L)$, V_D and V_Q are the *d*- and *q*-axis components of V_X, which are in phase (real voltage) and the quadrature (reactive voltage) with line current in the rotating reference frame, $V_X=V_D+jV_Q$. P_{S0} and Q_{S0} are the uncompensated real and reactive power flows when there is no compensation ($V_D=V_Q=0$). In (4), the real and reactive power flows are naturally coupled and need to be decoupled for efficient dynamic power flow control. Taking the first-derivative of (4) with respect to time yields the following equation. Assuming that P_{S0} and Q_{S0} are at certain values and that V_S is regulated at a constant voltage.

$$\frac{d}{dt}\begin{bmatrix} P_S \\ Q_S \end{bmatrix} = A\frac{R_L{}^2 + X_L{}^2}{X_L{}^2}\frac{d}{dt}\begin{bmatrix} V_Q \\ -V_D \end{bmatrix} + \frac{R_L}{X_L}\frac{d}{dt}\begin{bmatrix} Q_S \\ -P_S \end{bmatrix} \tag{5}$$

The derivatives in (5) can be approximated using the forward difference operator with a small time Δt as represented below:

$$\frac{1}{\Delta t}\begin{bmatrix} \Delta P_S \\ \Delta Q_S \end{bmatrix} = A\frac{R_L{}^2 + X_L{}^2}{\Delta t X_L{}^2}\begin{bmatrix} \Delta V_Q \\ -\Delta V_D \end{bmatrix} + \frac{R_L}{\Delta t X_L}\begin{bmatrix} \Delta Q_S \\ -\Delta P_S \end{bmatrix} \tag{6}$$

where $df/dt\approx\Delta f/\Delta t$ with $\Delta f=f(t+\Delta t)-f(t)$ [16]. According to (6), the required changes in P_S and Q_S are respectively related to V_Q and V_D. The last summing terms are the coupling terms and can vanish if the following feed-forward gains are added to the

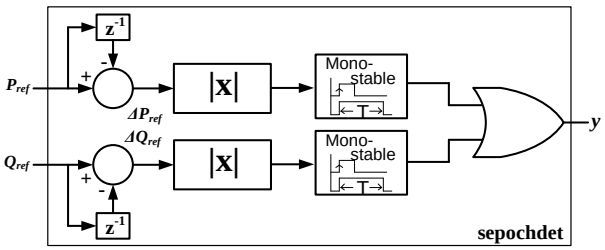


Fig. 5. Set-point change detector (SEPOCHDET).

conventional PI control scheme once the references of the power flows (P_S^{ref} and Q_S^{ref}) are externally defined by the user or supervisory control.

$$V_Q^{ref} = K_{p1}(P_S^{ref} - P_S) + \frac{1}{T_{i1}}\int (P_S^{ref} - P_S)dt - \frac{R_L}{X_L}Q_S \quad (7)$$

$$-V_D^{ref} = K_{p2}(Q_S^{ref} - Q_S) + \frac{1}{T_{i2}}\int (Q_S^{ref} - Q_S)dt + \frac{R_L}{X_L}P_S$$

where V_Q^{ref} and V_D^{ref} denote the desired *d-q* components of the series converter voltage. P_S and Q_S are, respectively, the current values of the real and reactive power flows measured at time *t*, K_{p1} and K_{p2} are the proportional gains of the real and reactive power flow controllers, respectively, T_{i1} and T_{i2} are the integration time constants of the real and reactive power flow controllers, respectively. In this case, the control scheme mentioned so far is regarded as a PI control scheme with decoupled gains (PI+DG).

B. Proposed Hybrid Fuzzy PI (HFPI) Controller

The decoupling gain design is made under some assumptions during system modeling. Moreover the dynamic performance of the PI+DG relies on exact knowledge of R_L and X_L which can change due to environmental factors. With this in mind, a HFPI controller is designed based on a set-point change detector (SEPOCHDET) and a fuzzy decoupler (FUDE) in support of the PI controllers. A fuzzy approach is implemented so that the power flow controller design is based on instantaneous system states rather than system parameters which are substantially liable to changes.

The SEPOCHDET shown in Fig. 5 keeps the advantages of simple PI controllers during start-up and in the steady-state by activating the FUDE when the first set-point change occurs in either P_S or Q_S. P_S^{ref} and Q_S^{ref} are first absolute valued and evaluated by a monostable multivibrator, which is a binary-logic, edge-triggered PSCAD/EMTDC component. A positive edge on its input results in the output going high and remaining high for the rest of the simulation, after being turned on. Consequently, the SEPOCHDET produces logic one to turn the switches on which connect the FUDE outputs to those of the PI controllers to reduce the interaction between the real and reactive power flow controllers during set-point changes.

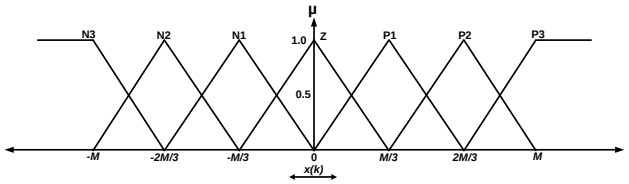


Fig. 6. Universe of Discourse.

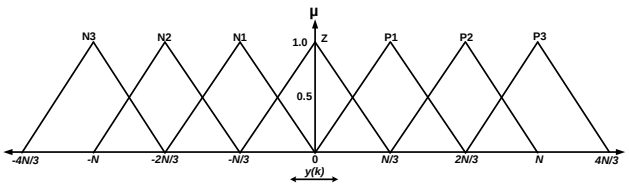


Fig. 7. MFs for FUDE output set.

TABLE I
RULE BASE FOR ΔV_Q

ΔPe/Pe	N3	N2	N1	Z	P1	P2	P3
N3	N3	N3	N3	N2	N2	N1	Z
N2	N3	N3	N2	N2	N1	Z	P1
N1	N3	N2	N2	N1	Z	P1	P2
Z	N2	N2	N1	Z	P1	P2	P2
P1	N2	N1	Z	P1	P2	P2	P3
P2	N1	Z	P1	P2	P2	P3	P3
P3	Z	P1	P2	P2	P3	P3	P3

A Mamdani-type fuzzy inference system is realized using heuristic information based on coupling characteristics. The system response is examined for the sequences of the set-point changes when only PI controllers with optimum parameters are employed. For example, if Q_S hugely deviates from its set-point while P_S^{ref} decreases sharply, a large control signal ΔV_D that pulls it toward to its set-point is expected. Similarly, when Q_S^{ref} is suddenly increased, P_S tends to decrease and a large control signal ΔV_Q is required. As a first step, x(*k*) is defined as the input set of crisp numerical signals *Pe*, Δ*Pe*, *Qe* and Δ*Qe* at the k^{th} sampling instant, limited to its universe of discourse. *Pe* and *Qe* are the real and reactive power flow errors, and Δ*Pe* and Δ*Qe* are the real and reactive power flow error rates, respectively. x(*k*) is then fuzzified according to seven linguistic characteristics, defined for each element. The abbreviations in Fig. 6 for the membership functions (MFs) that quantify the meaning of the linguistic characteristics are as follows: N3: big negative, N2: medium negative, N1: small negative, Z: zero, P1: small positive, P2: medium positive, and P3: big positive. The intersection point M is specific for each member in x(*k*).

The output set y(*k*) also needs fuzzification at the k^{th} sampling instant using the MF set for ΔV_Q and ΔV_D as depicted in Fig. 7. The intersection point N is specific for each member in y(*k*).

The rule base for the output ΔV_Q is listed in Table I which is

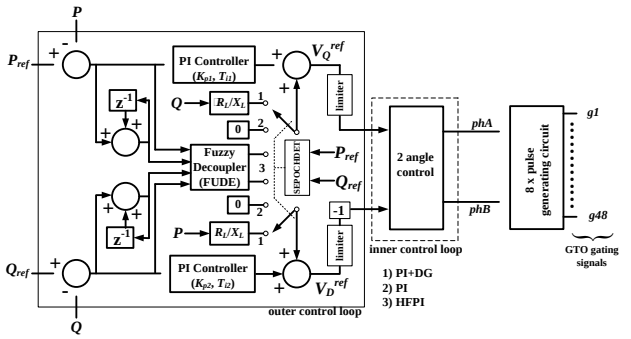


Fig. 8. Control scheme for the master VSC.

identical to that of ΔV_D, but designed for $\Delta Qe/Qe$. Every entity merges the error rate and the error fuzzy set values. For instance, first rule is:

R1: If ΔPe is P3 and Pe is P3 then ΔVQ is P3.

In next step, the min fuzzy operator is applied since the antecedent of the rule has more than one part that should be ANDed with each other. The min fuzzy operator is also used in the implication step, implemented for each rule. Here, the output fuzzy set is truncated by a real number given by the antecedent of the rule. The result of the implication is innately fuzzy. Therefore, to determine the crisp outputs (ΔV_Q, ΔV_D), the popular centroid defuzzification scheme has been utilized as the last step. Finally, the actual outputs of the FUDE are obtained. For instance, ΔV_Q at the k^{th} sampling instant can be written using (8). $\mu(i)$ and b_i are the aforementioned MF and the center of the MF of the consequent of rule i, respectively.

$$\Delta V_Q(k) = \frac{\sum_{i=1}^{49} b_i \int \mu(i)}{\sum_{i=1}^{49} \int \mu(i)} \tag{8}$$

Block diagrams of the HFPI controller and the PI+DG control scheme are shown in Fig. 8 for VSC2 or "the master VSC" of the IPFC. The control is implemented in two stages, the outer control loop by the i) HFPI controller, ii) PI+DG controller, iii) PI controller and the inner control loop to compute phase shift angles for the two converter groups. Limiters limit the values of the d-q voltage components by consideration of the maximum voltage generation capacity of the VSC.

VSC1 or "the slave VSC" regulates the DC link capacitor voltage and controls the real power flow on Line-1. The control scheme based on parameter optimized PI controllers is shown in Fig. 9. The error in DC link voltage drives the PI controller to produce the d-component of the VSC1 output voltage to achieve DC link voltage control. Similarly, the real power flow control on Line- 1 is carried out by the q-component of the VSC1 output voltage.

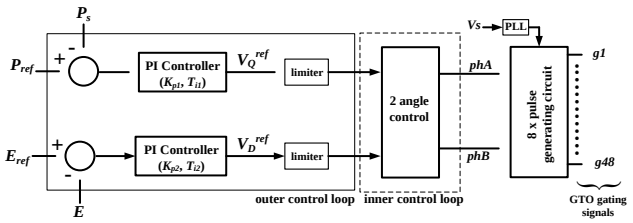


Fig. 9. Control scheme for the slave VSC.

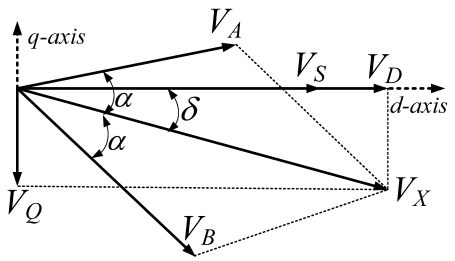


Fig. 10. Voltage vectors of Group A or B in rotating reference frame.

IV. 2-Angle Control

A 2-angle control method was proposed by Hagiwara et al. [17] to compute the desired phase shifts (*phA* and *phB*) for the converter groups (Group A and Group B in Fig. 2) using the d-q axis voltage components. If a PWM switching scheme is preferred to generate the GTO gating signals, the modulation index and the phase shift can be easily calculated in the inner control loop. The literature is rich with work in which approximated or simple converter models are employed. However, this is not realistic for high power applications. Fig. 10 shows V_X, which is the AC output voltage vector of a quasi multi-pulse converter.

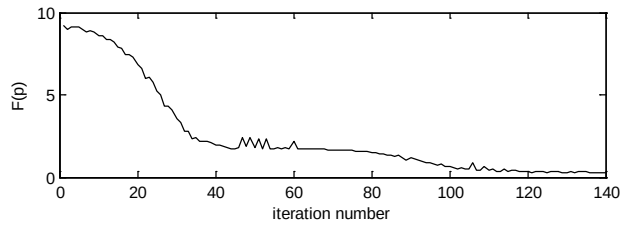
V_X can be obtained by summing V_A and V_B, which are the AC output voltage vectors of Group A and Group B, respectively. The voltage vector of Group A leads the d-axis by (α-δ) degrees, while voltage vector of Group B lags the q-axis by (α+δ) degrees. Thus the two voltage phasors are described by the following equations:

$$\begin{aligned} V_A &= |V_A| \angle (\alpha - \delta)^\circ \\ V_B &= |V_B| \angle -(\alpha + \delta)^\circ \end{aligned} \tag{9}$$

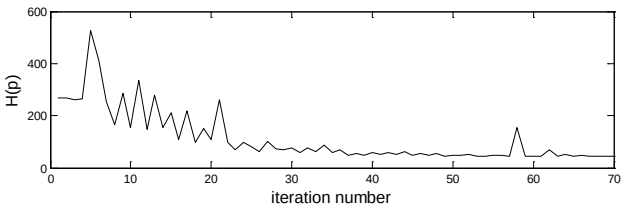
According to (9), since the magnitudes of V_A and V_B are constant, the desired magnitude and phase angle of V_X can only be obtained by controlling α and δ. Thus the desired phase angles α^* and δ^* are computed by the following equations in real-time:

$$\alpha^* = \tan^{-1} \sqrt{\frac{(2V_F)^2 - \left(V_D{}^{ref}\right)^2 - \left(V_Q{}^{ref}\right)^2}{\left(V_D{}^{ref}\right)^2 + \left(V_Q{}^{ref}\right)^2}} \tag{10}$$

$$\delta^* = \tan^{-1} \frac{V_Q{}^{ref}}{V_D{}^{ref}} \tag{11}$$



(a)



(b)

Fig. 11. (a) Master controller cost function minimization in simplex optimization routine. (b) Slave controller cost function minimization in simplex optimization routine.

TABLE II
SIMPLEX OPTIMIZED CONTROLLER PARAMETERS OF IPFC

Method	*F(p)*, VSC2	K_{p1}	T_{i1}	K_{p2}	T_{i2}
Non-optimized	9.1940	0.8	0.01	0.8	0.01
Simplex	0.2930	192	0.00086	192	0.00124
Method	*H(p)*, VSC1	K_{p1}	T_{i1}	K_{p2}	T_{i2}
Non-optimized	266.886	0.01	0.001	0.01	0.001
Simplex	43.7829	0.05154	0.00529	0.01489	0.00434

where V_F is the average converter voltage to minimize the measurement variations which is computed as:

$$V_F = \frac{1}{2}\left(V_A + V_B\right) \tag{12}$$

Synchronization with the *d*-axis is ensured with the following set of relations:

$$phA = \theta_S + (\alpha - \delta) + x_0$$
$$phB = \theta_S - (\alpha + \delta) + y_0 \tag{13}$$

where θ_S is the phase angle of the sending-end bus, obtained by a PLL, and x_0 and y_0 are respectively the phase-shifts for Group A and Group B, required for proper operation of the multi-pulse configuration.

V. FINDING OPTIMUM PI PARAMETERS

The simplex method iteratively finds the optimal parameter set $p=\{K_{p1}, K_{p2}, T_{i1}, T_{i2}\}$ for PI controllers of the master VSC and the slave VSC by minimizing the cost functions in (14) and (15) depending on sum of the integral square errors of the controlled variables.

$$F(p) = 100\int_{t=0}^{T}\left((P_2^{ref} - P_2)^2 + (Q_2^{ref} - Q_2)^2\right)dt \tag{14}$$

$$H(p) = 100\int_{t=0}^{T}\left((P_1^{ref} - P_1)^2 + (E^{ref} - E)^2\right)dt \tag{15}$$

where T is the total simulation time which was chosen to be much longer than the settling time of the control system. The simplex method is a direct search algorithm which is executable in PSCAD/EMTDC. It is based on a geometric figure called a "simplex" [18]. The vertices of the simplex are defined by variable numbers and the worst vertex, when the function is the largest, it is rejected and replaced by a new vertex. A new simplex is created until the function values at the vertices are the smallest. The simplex size is reduced iteratively and the coordinates of the minimum point are found. While the FUDE is off, the simplex method is executed for a sequence of unit step changes applied to P_2^{ref} and Q_2^{ref} for Line-2. During the optimization routine, the variation of $F(p)$ and $H(p)$ is plotted against the iteration number in Fig. 11a and Fig. 11b, respectively.

The optimum parameter set is listed in Table II. First, the parameters of the master control scheme are optimized using (14) under the condition that the slave controller is employed with pre-defined parameters providing a robust and stable IPFC performance. Here it is not ensured that these parameters are optimal, but they give satisfactory dynamic performance. Secondly, the parameters of the slave control scheme are optimized using (15) while the solution of first case result is applied to the master control scheme. The algorithm is executed for a tolerance of 1.0E-6.

VI. SIMULATION CASES

To test and evaluate the decoupling performances of different controllers, a 4-generator, 4-bus test power system embedded with an IPFC (Fig. 1), and the control loops except for the FUDE are simulated in PSCAD/EMTDC. Only FUDE is modeled in MATLAB which is communicated on-line through an interface written in PSCAD/EMTDC. The IPFC power circuit data and test system data are given in the Appendix. The solution time-step is set to 100 μs in PSCAD/EMTDC. While the IPFC is de-activated when the switches (sw1, sw2) are closed, the real and reactive power flows of Line-1 and Line-2 are measured to design reasonable set-point changes. The following control tasks and controllers are considered for the case studies:

- Line-1 sending-end real and reactive power flow control with optimized PI controllers
- IPFC DC link voltage control with optimized PI controllers
- Line-2 sending-end real and reactive power flow control with
  - Optimized PI controllers (with zero-decoupled gains)
  - Optimized PI controllers with decoupled gains (PI+DG)

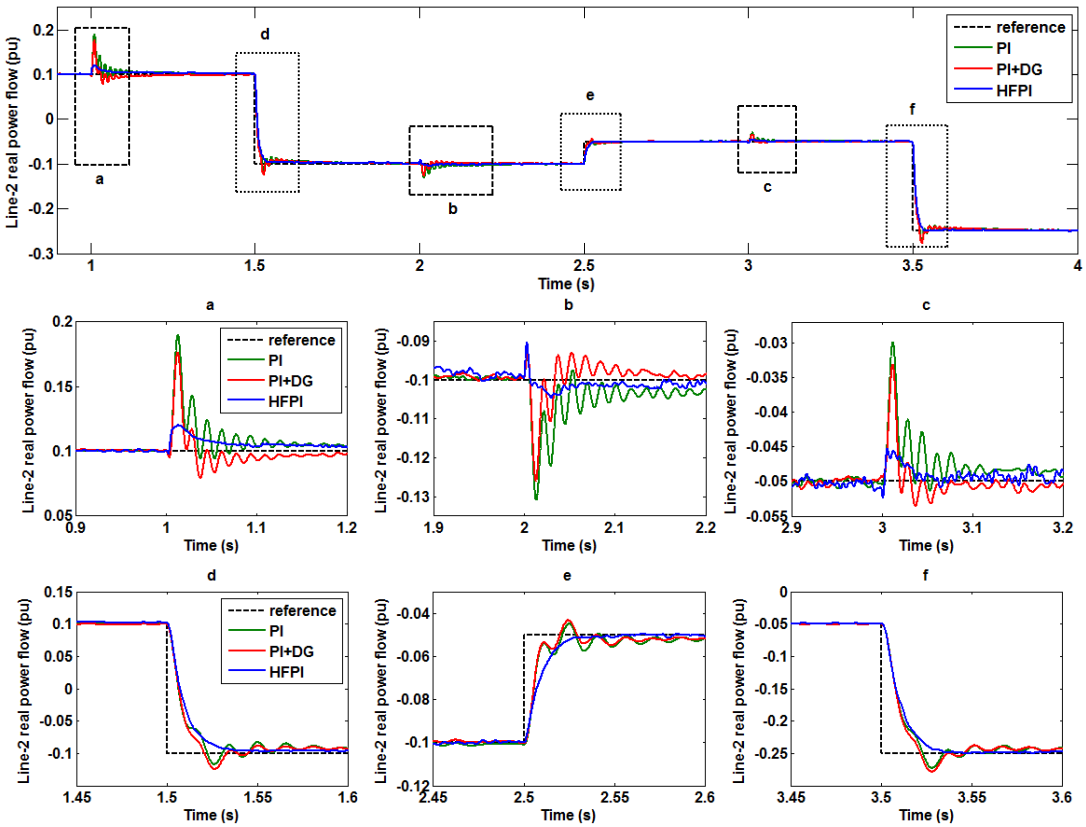


Fig. 12. Dynamic performance of real power flow controller for master VSC in case of three control schemes.

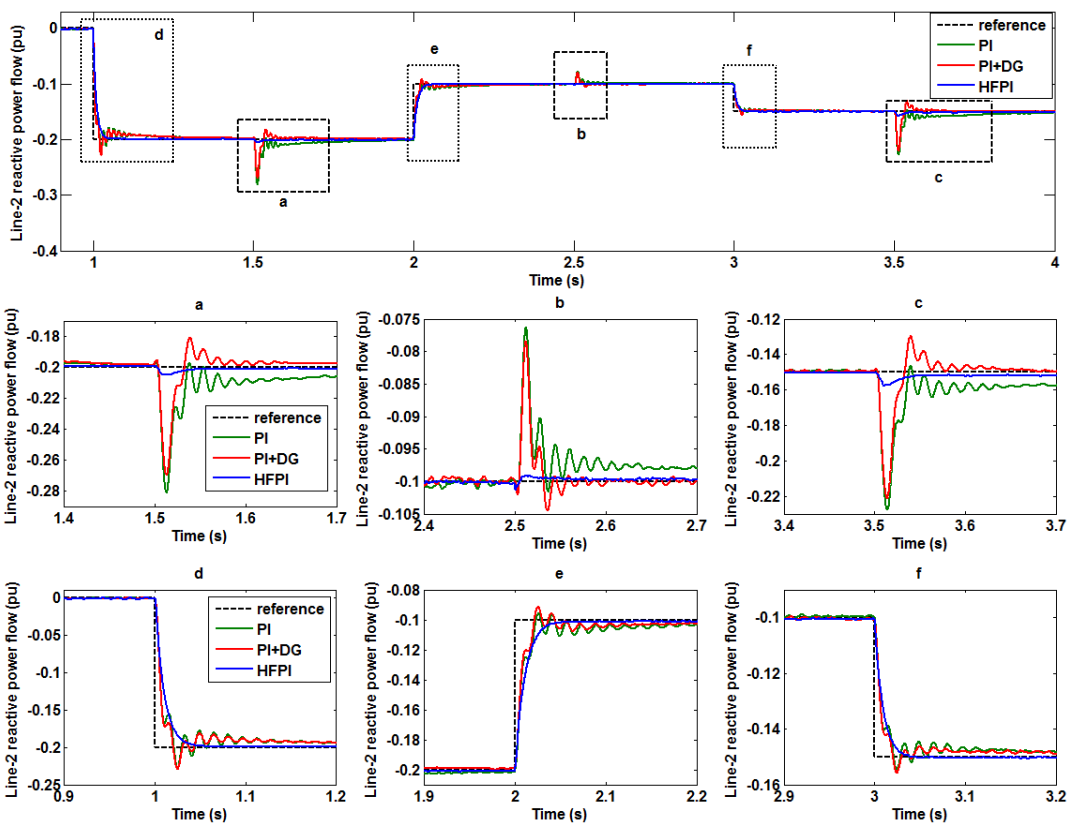


Fig. 13. Dynamic performance of reactive power flow controller for master VSC in case of three control schemes.

- Optimized PI controllers with FUDE (HFPI controller)

A. Case 1

In this case study, the IPFC is activated by opening the switches (sw1 and sw2) and the dynamic performances of the aforementioned controllers are simulated and compared when the system is subjected to a sequence of unit-step changes in the real and reactive power flow commands of Line-2. The reference for the real power flow on Line-1 is set as 2.3 pu and the IPFC DC link voltage is regulated at 1.0 kV throughout the case study. As observed in Fig. 12, the reactive power flow command has been altered to force the coupling during the instants when the real power flow command is constant. Although the PI controller is parameter optimized, relatively large fluctuations in the real power flow have been observed at the times, t=1.0 s, 2.0 s, and 3.0 s, respectively (Fig. 12(a)-(c)). The PI controller with decoupled gains (PI+DG) gives better results when the dynamic performance is compared to that of the PI controller only. Although the PI controller or the PI+DG give satisfactory steady-state tracking performance, the inherent coupling between the power flow control loops are not avoided and the IPFC dynamic performance is adversely affected. On the other hand, the HFPI controller has superior decoupling as can be seen from the response curves since the variation in the real power flow is effectively minimized when the reactive power flow command has been changed. Moreover, Fig. 12(d)-(f) gives a comparison between the responses of the different controllers to step-changes in the real power flow command. The HFPI controller responds with less oscillations and shows reduced overshoot characteristics. The dynamic performance of the reactive power flow control loop with different control schemes is also evaluated in this case study. Fig. 13 shows the traces of different reactive power flow controllers in response to unit-step changes in the real power flow command. As shown in Fig. 13(a)-(c), the HFPI controller performance is superior to either the PI controller or the PI+DG on tracking the reference signal and the HFPI controller effectively minimizes the coupling effect between the two power flow control loops. As a consequence of the unit-step command, the reactive power flow fluctuations are minimized better by a HFPI controller with less oscillatory and reduced overshoot response when compared to the other control schemes. Two commonly used measures for control system performance, namely the integral square error (ISE) and the integral absolute error (IAE), are calculated for ($0.9\ \text{s} \le t \le 5.0$ s) in Table III to provide a quantitative and exact comparison between the different control schemes. Fig. 14 shows the dynamic performance of the slave VSC real power flow controller and it is found that among the three controllers, the variations are the smallest in case of the HFPI controller. It gives a smoother response when compared to the PI+DG. The IPFC DC link voltage excursions for different control schemes are depicted in Fig. 15. The DC voltage controller is almost robust and gives a satisfactory response for all of the control modes. But when the comparisons are particularly made at the instants (t=1.0, 1.5, 2.0, 2.5, 3.0, 3.5 s), relatively smaller spikes are observed in the simulated waveforms in the case of the HFPI controller. Fig. 16 compares the *d-q* components of the injected current of the master converter in with the three controllers. Prominent time instants are marked with red rectangles when the real power flow reference is changed in case of i_D and when the reactive power flow reference is changed in case of i_Q. These spikes in the marked regions showing the interactions between the two power flow controllers are effectively reduced by the HFPI controller. Although the spikes caused by the HFPI controller are practically the same when compared to the ones caused by the PI controller, the HFPI controller weakens the spikes much better than the PI+DG. Fig. 17 shows the control signals (V_D^{ref} and V_Q^{ref}) for the inner control loop and the measured voltages (V_D and V_Q) of the master converter at the primary windings of the series coupling transformer *Tr1*. It has been ensured that the "2-angle control" block operates stably and that the orthogonal components of the master converter voltage perfectly trace their pertinent reference values in case of the HFPI controller. Fig. 18 shows the output signals of the inner control loop in case of the HFPI controller which produces the required phase shifts (*phA* and *phB*) to the converter Group A and the converter Group B, respectively. Fig. 19 depicts the anode-to-cathode voltage of the selected GTO from Group A of the master converter in case the HFPI controller is activated. As designed for quasi multi-pulse operation, the GTO is triggered only once in one fundamental cycle of 50 Hz.

B. Case 2

In this case study, the controller references are kept exactly the same as in Case 1 and the R_L/X_L ratio of Line-2 is increased by three times to investigate the parameter sensitivity of the three controllers. Fig. 20 and Fig. 21 show the comparative tracking performances of the controllers for the real and reactive power flow control loops, respectively. The ISE and IAE performance indices are listed in Table III for $0.9\ \text{s} \le t \le 5.0$ s. As shown in Fig. 20 (a)-(c), the real power flow control loop interacts adversely with the reactive power flow control loop when the PI+DG is employed. The PI+DG has the maximum overshoot of all of the controllers and it gives the slowest response when compared to the other control schemes. The same situation is also observed in Fig. 21 (a)-(c) when the reactive power flow of Line-2 is controlled by the PI+DG during set-point changes in the real power flow. As expected, the performance of the PI+DG for both the real and reactive power flow control loops degrades significantly, since the decoupled gains are designed offline using transmission line data. When comparing Case 1 and Case 2 quantitatively, an increase of 32.68% in the ISE and an increase of 80% in the IAE are computed for the real

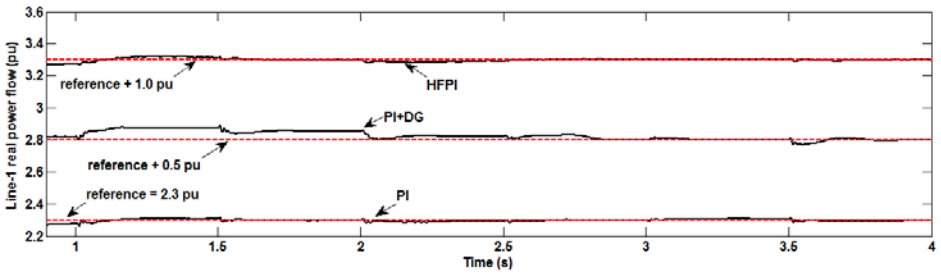


Fig. 14. Dynamic performance of real power flow controller for slave VSC interacting with the three control schemes for master VSC.

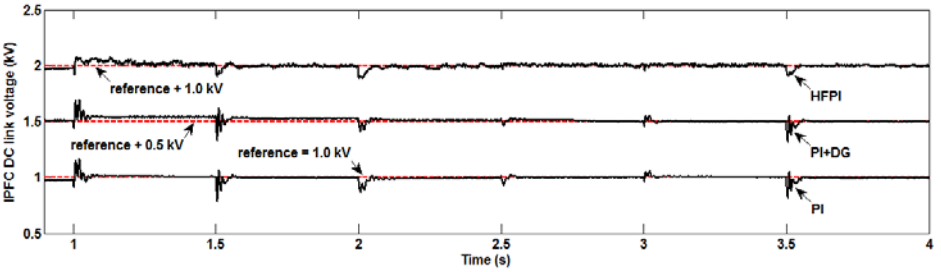


Fig. 15. Dynamic performance of DC voltage controller for slave VSC interacting with the three control schemes for master VSC.

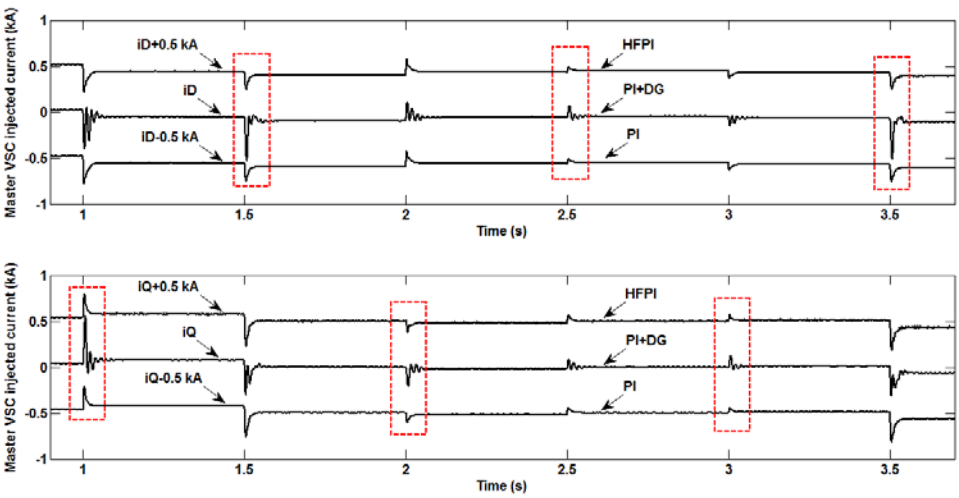


Fig. 16. *d-q* components of master VSC injected current in case of three control schemes for master VSC.

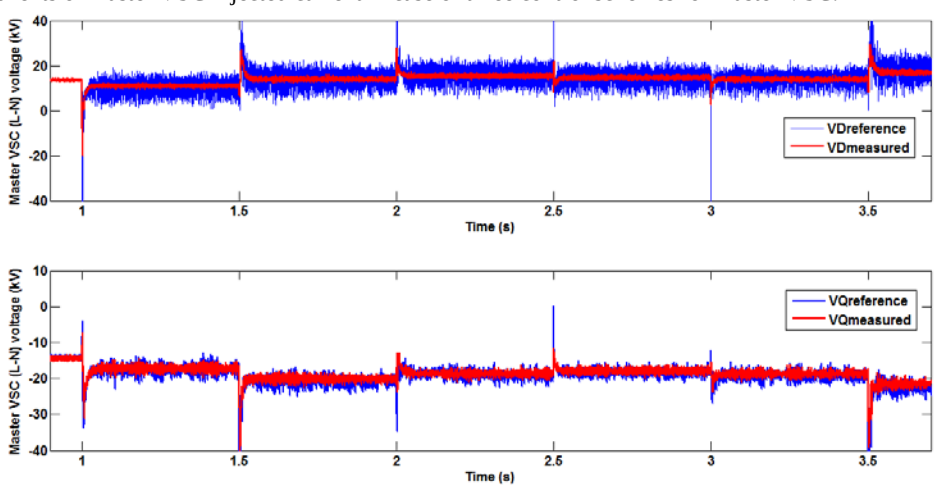


Fig. 17. *d-q* components of master VSC line-to-neutral voltage and reference voltages to inner control loop generated by HFPI controller.

power PI+DG controller. Similarly, an increase of 62.55% in the ISE and an increase of 127.18% in the IAE are computed for the reactive power PI+DG controller. Because the PI gains are optimized for the operating conditions in Case 1, the

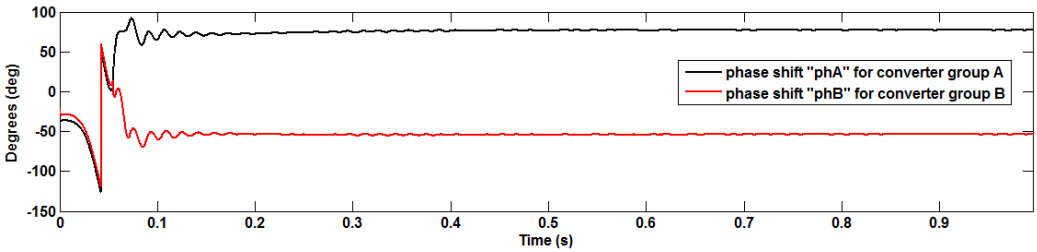


Fig. 18. Phase angles generated by inner control loop for two converter groups of master VSC in case HFPI controller is activated.

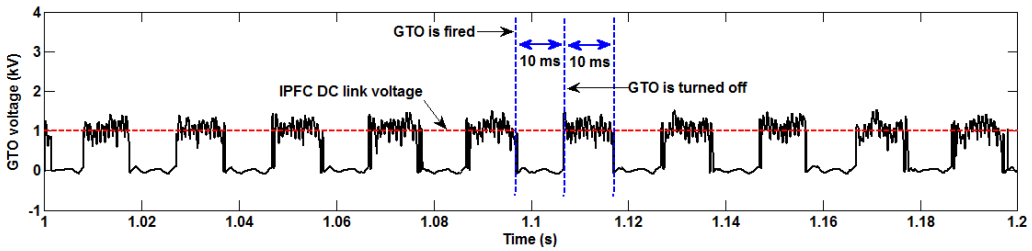


Fig. 19. Anode-to-cathode voltage of a selected GTO in Group A of the master VSC in case HFPI controller is activated.

TABLE III
QUANTITATIVE PERFORMANCE ANALYSIS OF DIFFERENT CONTROLLERS

Case 1				Case 2			
Control Action	Controller	ISE	IAE	Control Action	Controller	ISE	IAE
Line-2 real power flow	PI	5.8784	136.2015	Line-2 real power flow	PI	5.8918	140.4160
	PI+DG	5.3502	115.8114		PI+DG	7.0987	208.7502
	HFPI	4.5300	88.8933		HFPI	5.5127	112.5168
Line-2 reactive power flow	PI	4.5269	168.0034	Line-2 reactive power flow	PI	4.5761	172.4952
	PI+DG	3.6717	116.8833		PI+DG	5.9683	265.5316
	HFPI	2.6631	73.9114		HFPI	2.9794	69.4454

TABLE IV
THE HIGHEST THD VALUES IN CASE OF THREE CONTROL SCHEMES

Case 1			Case 2		
Controller	THD@Bus1	THD@Bus2	Controller	THD@Bus1	THD@Bus2
PI	0.48 %	0.75 %	PI	0.45 %	0.70 %
PI+DG	0.48 %	0.74 %	PI+DG	0.46 %	0.70 %
HFPI	0.46 %	0.71 %	HFPI	0.46 %	0.69 %
Controller	THD@Bus3	THD@Bus4	Controller	THD@Bus3	THD@Bus4
PI	0.91 %	0.98 %	PI	0.80 %	0.89 %
PI+DG	0.90 %	0.97 %	PI+DG	0.82 %	0.89 %
HFPI	1.3 %	1.51 %	HFPI	1.21 %	1.47 %

dynamic performance of the PI controller slightly weakens when compared to that of Case 1. Even though the system parameters are changed, the HFPI controller successfully reduces the interactions between the real and reactive power flows with the lowest ISE and IAE indices when compared to either the PI controller or the PI+DG. Furthermore, it has been observed in Fig. 20 (d)-(f) and in Fig. 21 (d)-(f) that the HFPI controller gives a smooth response and greatly improves the rise time and the settling time of the control loops when responding to set-point changes.

C. Discussions

The proposed HFPI controller minimizes the interactions between the control loops of the real and reactive power flows and gives a smoother response when compared to either the PI+DG or the PI controller. Even when the system coefficients change, it is still able to alleviate these interactions and have a robust response to uncertainty. On the other hand, the performance of the PI+DG strongly relies on knowledge of the system parameters and it only performs better than the PI controller under the condition that the model parameters match with the parameters of the decoupled gain design. The HFPI controller does not disturb the other IPFC control loops, such as power flow control on Line-1 and the dc link voltage control although it has introduced small voltage ripples to the DC interface. Therefore, the interactions between the controllers are minimal for multi-functioning FACTS device which is highly desirable.

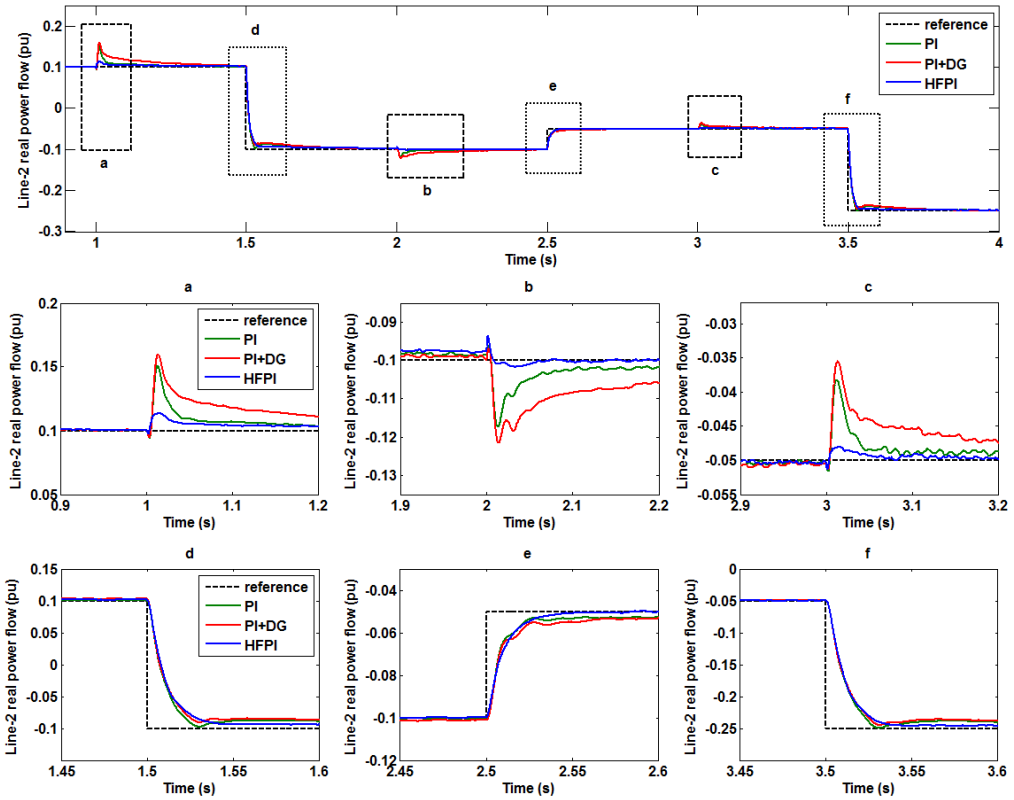


Fig. 20. Dynamic performance of real power flow controller for master VSC in case of three control schemes.

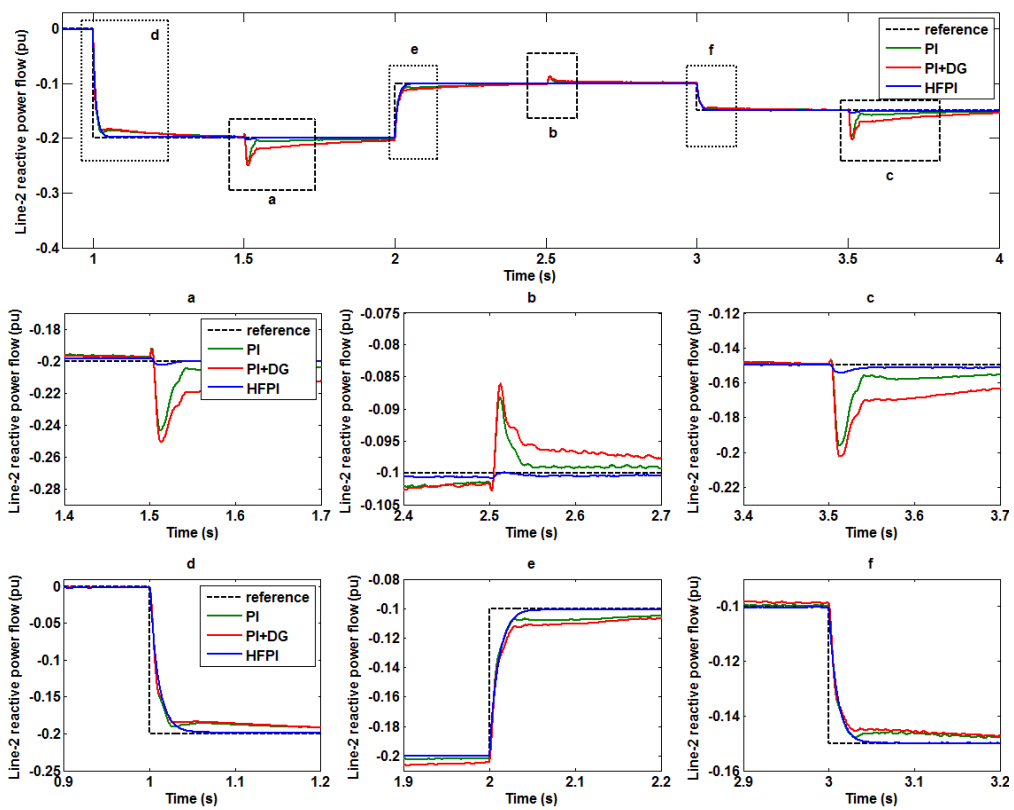


Fig. 21. Dynamic performance of reactive power flow controller for master VSC in case of three control schemes.

D. THD Content

Table IV lists the highest THD values computed using the first 63 harmonics at four common coupling points between the IPFC and the power system. Records for $1.0 \text{ s} \leq t \leq 5.0$ s confirm that the IPFC does not violate of the THD upper limit of 2.5 % for the 154 kV transmission level [19]. Consequently, filtering is not required even when the GTOs are switched at the fundamental frequency.

VII. CONCLUSIONS

In this paper, a new control scheme based on the conventional PI and fuzzy logic theory for a quasi multi-pulse IPFC has been designed and tested for decoupled real and reactive power flow control. It can also be generalized to UPFC to relieve the inherent real and reactive power flow coaction. Contrary to the decoupled gain design, the proposed control scheme does not rely on a system mathematical model. Consequently it adapts itself to parameter variations in the power system and performs better. SEPOCHDET is an option to activate the FUDE only when a change in the real and reactive power flow command occurs. Such coordination can yield an improved rise time and settling time for start-up transients in simulation environments. Moreover the quasi multi-pulse design brings two important advantages: 1) it injects a low THD content into power systems, which complies with international standards. 2) with fundamental frequency GTO switching, the converter losses are reduced.

APPENDIX

4-Generator 4-Bus System Data:

The base power is 100 MVA and the base voltage is 154 kV (line-to-line). The G1,G3 terminal voltage is 1.0 pu with a phase shift of 0.0º and G2,G4 terminal voltage is 0.974 pu with a phase shift of 10.0º. All of the series inductive reactances of the generators are 2.65% pu. The coupled pi-section line (All lines) resistance=1.938%pu, the inductive reactance=5.917% pu, and the susceptance =5.28% pu.

IPFC Data:

The VSCs are identical, the base power is 100 MVA, the base voltage is 46.84 kV (line-to-neutral), C = 0.2 F. The single-phase three winding transformer in the 12-pulse unit is rated at 8.33 MVA with a winding ratio of 10.0 kV/1.0 kV/0.5774 kV, and the leakage reactance is 10.0 % pu. The summing transformer is rated at 16.67 MVA with a winding ratio of 23.42 kV/23.42 kV, the leakage reactance is 10.0 % pu. The series coupling transformer is rated at 33.33 MVA, with a winding ratio of 23.42 kV/9.0 kV, and the leakage reactance is 1.0% pu. The GTO/diode turn on and turn off resistances are 0.005 Ω and 1.0E+8 Ω, respectively.

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