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Electrical Characteristics and Thermal Reliability of Stacked-SCRs ESD Protection Device for High Voltage Applications

Yong Seo Koo*, Dong Su Kim*, and Jin Woo Eo†

†*Dept. of Electronics and Electrical Eng., Dankook University, Jukjeon, Korea

Abstract

The latch-up immunity of the high voltage power clamps used in high voltage ESD protection devices is very becoming important in high-voltage applications. In this paper, a stacking structure with a high holding voltage and a high failure current is proposed and successfully verified in 0.18um CMOS and 0.35um BCD technology to achieve the desired holding voltage and the acceptable failure current. The experimental results show that the holding voltage of the stacking structure can be larger than the operation voltage of high-voltage applications. Changes in the characteristics of the stacking structure under high temperature conditions (300K-500K) are also investigated.

Key words: Electro-Static Discharge (ESD), Holding Voltage, Latch-up, Silicon Controlled Rectifier (SCR)

I. INTRODUCTION

With a rapid increase in the demands on high voltage applications in modern electronic circuits such as automotive, power management, power distribution and driver ICs, high voltage ICs are being widely used in IC products nowadays [1]. The LDMOSFET (Lateral Double Diffuse MOSFET) is widely used as a switching device, an output driver and for general ESD protection in high voltage ICs. However, when a LDMOSFET is used as an ESD protection device, the LDMOSFET is inherently weak with respect to both ESD robustness and ESD reliability [2]. Due to the strong snap-back characteristics of LDMOSFETs, the non-uniform turn-on of a parasitic bipolar junction transistor (BJT) is found out. Moreover, LDMOSFET based ESD protection devices also consume a relatively large silicon area and static or transient latch-up may occur due to the relatively low holding voltage [3]. Meanwhile, it is well known that the silicon controlled rectifier (SCR) has a superior ESD protection behavior for high failure current derived by hole and electron injection conductivity modulation. However, SCR based ESD protection devices have a relatively low holding voltage (about 1.5V~2V). Therefore, if these devices are applied as a power clamp between the VDD and the VSS then, there is a possibility that the SCR will be triggered by unwanted noise, which may cause latch-up stimuli to occur during normal operation. These issues can be overcome by increasing the holding voltage or the holding current. Consequently, SCR causes difficulties in the design of ESD protection in high voltage applications [4]-[7]. In this paper, an SCR based ESD protection device with a high holding voltage is introduced. Moreover, an SCR stacking structure that is comprised of an SCR with a high holding voltage is proposed. The electrical characteristic and thermal reliability of the staking structure has been effectively verified in a 0.18um CMOS and in a 0.35um BCD process.

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Recommended for publication by Associate Editor Hyung-Min Ryu.
†Corresponding Author: jweo@dankook.ac.kr
Tel: +82-31-8005-3625, Fax: +82-31-8005-4185, Dankook Univ.
*Dept. of Electronics and Electrical Eng., Dankook University, Korea

II. SINGLE SCR-BASED ESD PROTECTION DEVICE WITH A HIGH HOLDING VOLTAGE

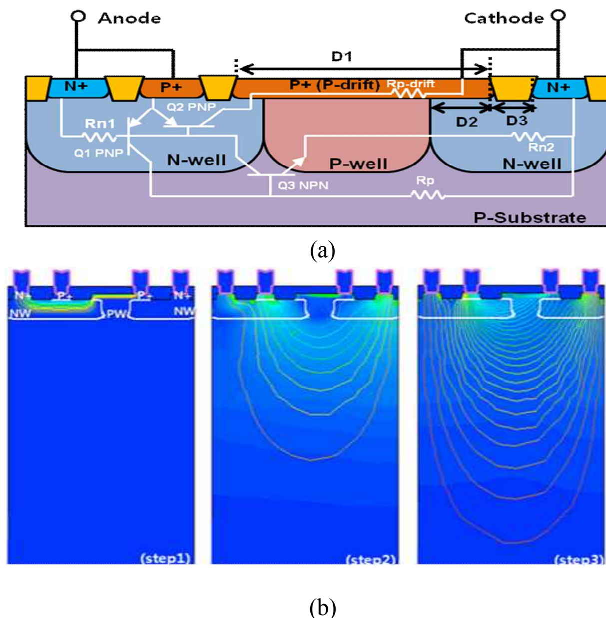
A. Device Description

The basic unit of the SCR device is formed by using a 4-layer PNPN configuration. This is made by extending a P+ cathode to the first N-well and then adding a second N-well wrapping around the N+ cathode of a conventional SCR. A cross-sectional view and an equivalent circuit of a basic SCR device are shown in Fig. 1 (a). In order to raise the holding voltage, the p+ cathode (p-drift) region and the second n-well

wrapping around the n+ cathode are formed. The basic unit device is triggered by an avalanche breakdown of the n-well – p-drift junction, or in other words, the collector-base region of Q2. As the pad (anode) voltage increases, n-well and p-drift junction becomes reverse biased. Eventually, n-well and p-drift junction goes into an avalanche breakdown due to the high electric-field between the two junctions, and subsequently, it generates electron–hole pairs. The whole current through the parasitic PNP-BJT Q2 flows into the p-drift junction [ref. Fig 1(b)-step1], and then, it increases the potential of the p-well. The emitter-base junction of the parasitic NPN-BJT Q3 becomes forward-biased by the potential in the p-well consequently turning it on [ref. Fig 1(b)-step2]. When the Q3 turns-on, the current of Q3 generates a voltage drop across Rn1 and turns on the PNP BJT Q1 as well. The current of Q1 creates a voltage drop across Rp. This, in turn helps to maintain the Q3 state. At this point, there is no need for the anode to provide the bias for Q3 due to the current of Q1 and the initiate SCR action [ref. Fig 1(b)-step3]. On the other hand, when a negative bias is applied to the pad with a ground line (negative ESD), the parasitic diode (p-drift/P-well – N-well/n+) becomes forward biased to discharge the negative ESD current.

B. Analysis of a Single SCR-based ESD Protection Device

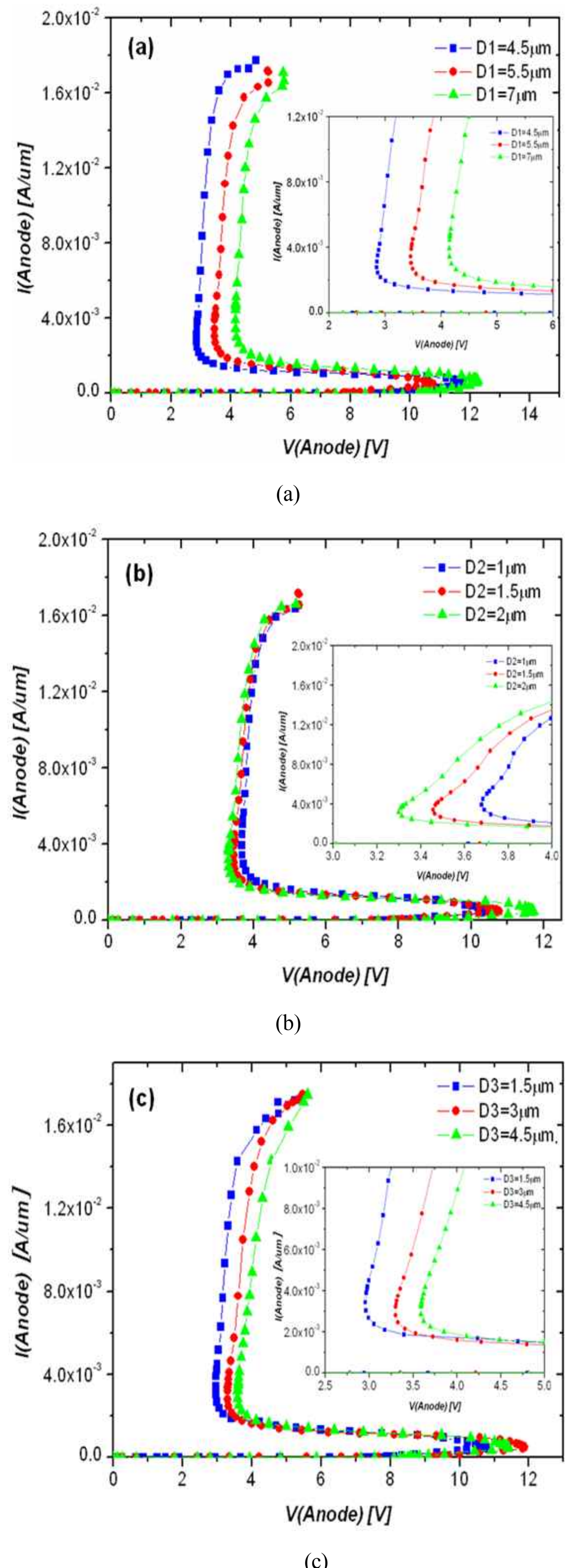
Before a stacked SCR-based device with a high holding voltage can be composed, the holding voltage trend of a single SCR-based ESD protection device with different design parameters, D1, D2 and D3 (shown in Fig. 1(a)) was analyzed. They are investigated by using the synopsys TCAD simulator and the I-V characteristics are measured using a TLP (Transmission Line Pulse) System.



(a)

(b)

Fig. 1. Single SCR-based ESD protection device (a) cross-sectional view and equivalent circuit, (b) current density and flow line



(a)

(b)

(c)

Fig. 2. The simulated I-V characteristics of a single SCR-based device with different design parameters of (a) D1 variation, (b) D2 variation and (c) D3 variation.

TABLE I

OVERVIEW ON PROCESS TECHNOLOGY CONSIDERED FOR EXPERIMENT

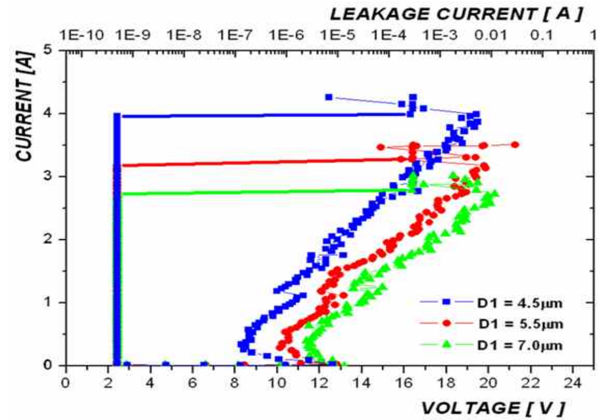
Minimum Feature Size	Junction Depth (N-well/P-well)	Junction Depth (n+/p+)	Substrate
0.18um	1.2um	0.25um~0.3um	Bulk
0.35um	1.8um	0.6um	Epi

The holding voltage is a voltage drop between the anode and cathode after the parasitic BJT is turned-on and it is written as in equation (1).

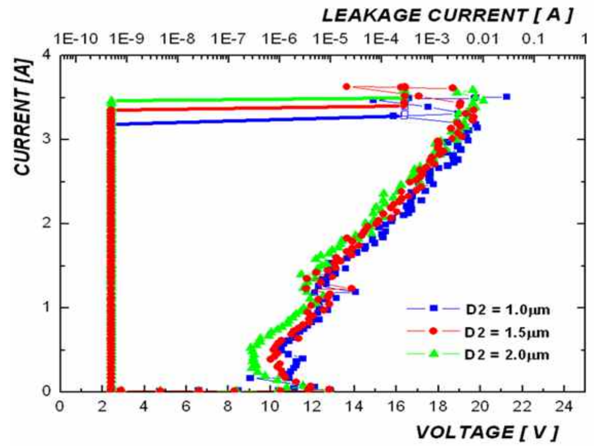
$$V_H = V_{BE}(Q1_{PNP}) + V_{BE}(Q3_{NPN}) + V_{Rn2}$$
$$= V_{BE}(Q2_{PNP}) + V_{Rp-drift} \quad (1)$$

At equation (1), V_{BE} ($Q1_{PNP}$) and V_{BE} ($Q3_{NPN}$) are the emitter-base voltages of Q1, and Q3, respectively. V_{Rn2} and $V_{Rp\text{-}drift}$ are the voltage in R_{n2} and $R_{p\text{-}drift}$, respectively. This is due to the free carriers that are injected from the emitter regions of the two BJTs. Therefore, the lateral dimension, which is associated with the base width of BJT, and resistances of R_{n2} and $R_{p\text{-}drift}$ are very important. The adjustment of the holding voltage is readily accomplished by adjusting the length of the p-drift junction (D1), which is associated with $R_{p\text{-}drift}$ and the length of the p+ cathode in the n-well region (D2) and the space of the two cathodes (D3), which are associated with the base width of NPN (Q3) and R_{n2}, respectively.

All of the design parameters of the SCR-based device in the simulation are fixed at similar values except for the design parameters D1, D2 and D3. The simulated I-V characteristics of a single SCR-based device with different design parameters are shown in Fig. 2. The holding voltage increases with increasing D1. Moreover, D2 is inversely proportional to the holding voltage. In additon, D3 is in direct proportion to the holding voltage. These results are shown in Figs. 2 (a), (b) and (c), respectively. A single SCR-based device is fabricated in the 0.35um BCD process. All of the design parameters of the SCR-based device are fixed at the same value except for the design parameters D1, D2 and D3. All of the devices have a width of 50um. Fig. 3. shows the TLP I-V characteristics and the DC leakage current of a single SCR-based device with different design parameters. The I-V characteristics and the DC leakage current have been measured using a TLP system with a pulse duration of 100ns and a rising time of 10ns. Fig. 3 (a) shows the measurement results for single SCR-based devices that have the same design parameters but different D1 values. The holding voltage is elevated from 8V to 12V by increasing the D1 dimension from 4.5um to 7um, while the trigger voltage is maintained the same at about 13V. Fig. 3 (b) shows that the holding voltage is elevated from 9V to 10.3V by decreasing the D2 dimension from 2um to 1um, while the trigger voltage is maintained the same at about 13V. Fig. 3 (c) shows that the holding voltage is elevated from 8.7V to 11.2V by increasing the D3 dimension from 1.5um to 4.5um, while the trigger voltage is maintained the same at about 13V. Consequently, when D1 is increased, the holding voltage is increased and D3 has the same tendency as D1. However, when D2 is increased, the holding voltage is also decreased.



(a)



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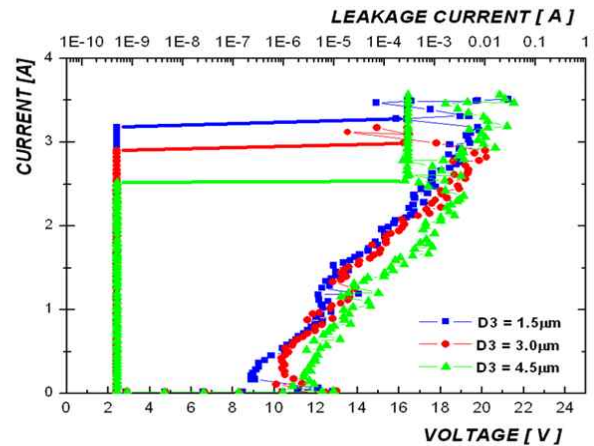


(c)

Fig. 3. Measured TLP I-V characteristics of a single SCR-based device with different design parameters of (a) D1 variation, (b) D2 variation and (c) D3 variation.

III. STACKED SCR-BASED ESD PROTECTION DEVICE

SCR stacking structures were successfully implemented in a 0.18um-CMOS technology and in a 0.35um BCD technology. Transmission line pulse (TLP) analysis results were obtained with a square pulse duration of 100ns and a default pulse rise time of 10ns. The temperature characteristics of the device have also been measured with a TLP tester by using a HOT CHUCK controller. Table I shows an overview of the process technologies that have been considered for the stacked SCR-based device design. These measurement results are presented in this work. The process condition (junction depth) of 0.18um and 0.35um technologies was selected for a comparison of the characteristics, and they are as shown in Table I.

A. 0.18um-CMOS Technology

Stacked SCR-based devices can be accomplished by connecting two or more of the aforementioned SCR-based devices. A cross sectional view of the stacking of two SCR-based devices is shown in Fig. 4(a). While stacking, the single SCR-based devices are isolated by an individual deep N-well from each device.

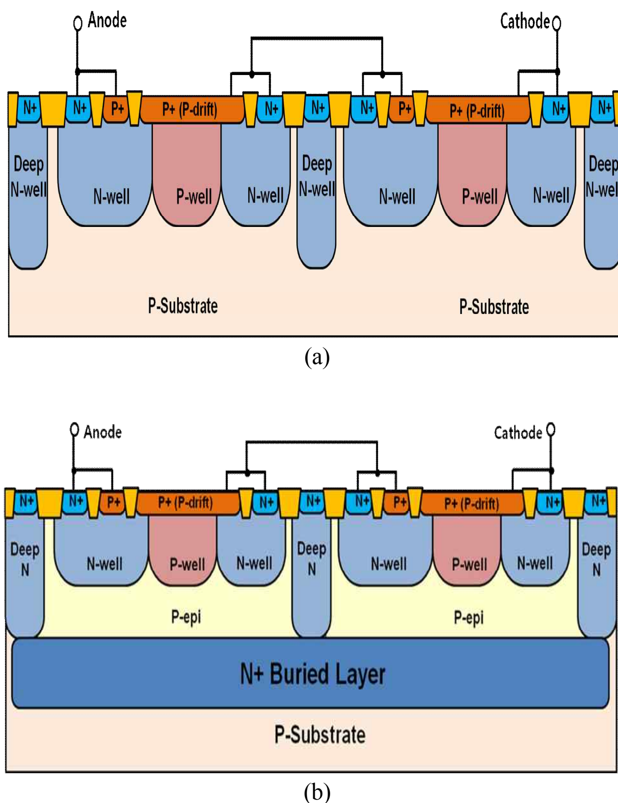


Fig. 4. Cross sectional view of 2-staking SCR-based structure in (a) 0.18um-CMOS process and (b) 0.35um-BCD process.

TABLE II

TO COMPARE SECOND BREAKDOWN TO AREA IN A 0.18UM CMOS TECHNOLOGY

	Second Breakdown (It2)	**Area (width * length)**	**It2/Area (mA/um^2)**
Unit	3.3A	60*23 um^2	2.4mA/um^2
2-stacked	2.9A	60*46 um^2	1.05mA/um^2
3-stacked	2.8A	60*49 um^2	0.67mA/um^2

The TLP measurement results of a basic single SCR-based device and a SCR stacking structure are depicted in Fig. 5 (a). The basic unit SCR device has a P-drift length of 5um (D1). Moreover, the P+ cathode has a 1.5um region in the n-well (D2), the spacing between cathodes p+ and n+ (D3) has a 2um region, and the device has a total width of 60um. From the measurement results shown in Fig. 5 (a), the measured trigger and holding voltage of unit the SCR are 13.8V and 6V, respectively. The SCR based device differs from a conventional SCR in its snapback characteristics (i.e., the holding voltage of a conventional SCR is about 2V).
The SCR stacking structure triggers at 13.8V (single), 29V (2-stacked) and 36.8V (3-stacked). The values of the holding voltage were 6V (single), 14V (2-stacked) and 20.5V (3-stacked) under the TLP test. The devices fail at a current level of more than 2.7A. By increasing the device width, the protection level according to the ESD product specifications can be easily adjusted. The measured second breakdown current and the area of the stacked SCR devices are as shown in Table II. The area is calculated as follows, (area = device width × unit device length × stack number), while ignoring the isolation spacing between each unit device.

B. 0.35um-BCD Technology

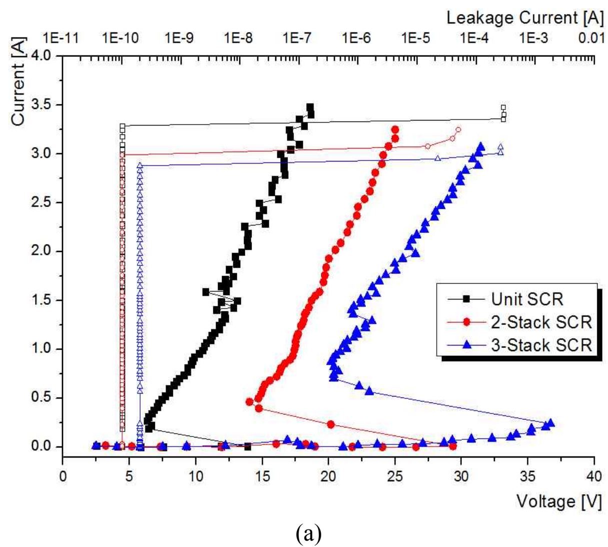
The SCR-based stacking structure was also realized in a 0.35um BCD technology. A cross sectional view of the stacking of two SCR-based devices is shown in Fig. 4(b). The N+ buried layer and deep N layer are used as an isolation ring. These processes (N+ buried layer and deep N layer) do not require an additional mask. These processes are essential for the vertical NPN bipolar transistor in 0.35um-BCD technology. In order to elevate the holding voltage of a basic unit SCR, the P-drift length of the unit device increases (D1=7um, D2=1.5um and D3=2um). Therefore, the unit SCR holding voltage is increased by an increment of the P-drift resistance, the ESD discharge path between the anode and the cathode, and a reduction of the parasitic NPN current gain. Moreover, the holding voltage also depends on the degree of the space charge neutralization in the base region of the NPN and PNP bipolar transistors, which is due to carriers being injected from the emitter regions of the two BJTs. If the n-well and the p-well of the device have a deep junction depth, the current gain of the parasitic bipolar required for operating the SCR is reduced and

the ESD discharge path resistance is increased between the anode and the cathode.

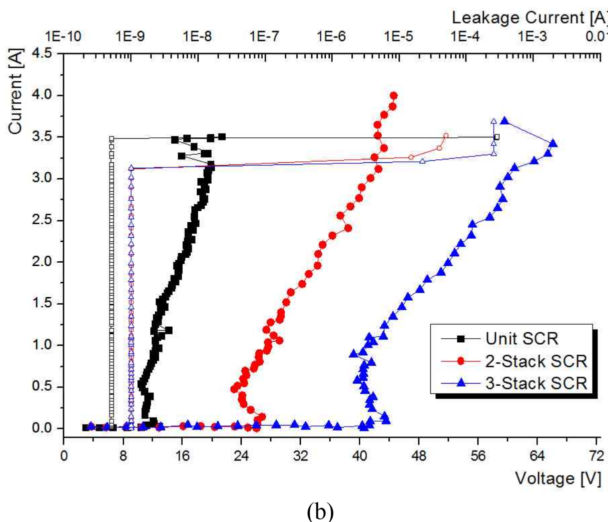
TABLE III

TO COMPARE SECOND BREAKDOWN TO AREA IN A 0.35UM BCD TECHNOLOGY

	Second Breakdown (It2)	Area (width * length)	It2/Area (mA/um^2)
Unit	3.5A	60*25 um^2	2.3mA/um^2
2-stacked	3.2A	60*50 um^2	1.06mA/um^2
3-stacked	3.2A	60*75 um^2	0.7mA/um^2



(a)



(b)

Fig. 5. The measured TLP I-V characteristics of stacked SCR devices with a width of 60um and three different stack numbers (1, 2, and 3) fabricated (a) in a 0.18um CMOS and (b) 0.35um BCD technology.

Therefore, 0.35um-BCD technology has a higher holding voltage when compared to 0.18um-CMOS technology. Experimental results are shown in Fig. 5 (b) for the three different variations of the stacked number (basic unit SCR, 2-stacked, 3-stacked). As can be seen in the plot, the holding voltage of the unit SCR can be elevated from 5V (holding voltage of unit device in a 0.18um CMOS) to 10V by increasing the p-drift length from 5um to 7um and the junction depth from 1.2um to 1.8um. The 2-stacked SCRs have a trigger voltage of 26V and the holding voltage can reach 21V with a small snapback. The 3-stacked SCRs have a trigger voltage of 44V and a holding voltage of 40V. By selecting the correct stacking number, the holding voltage of the stacking SCRs can be flexibly adjusted to meet the latch-up immunity requirements. The second breakdown currents of the different stacked SCRs (unit SCR, 2-stacked SCR, 3-stacked SCR) are 3.5A, 3.2A, and 3.2A, respectively. The three stacking SCRs still possess a high second breakdown current of more than 3A. The measured second breakdown current and the area of the stacked SCR devices are as shown in Table III. From the measured TLP I-V characteristics presented in Fig. 5, the trigger voltage (Vt1), the holding voltage (Vh) and the second breakdown current (It2) were extracted and they are shown in Fig. 6. For the three extracted parameters, the scaling behavior has been measured.

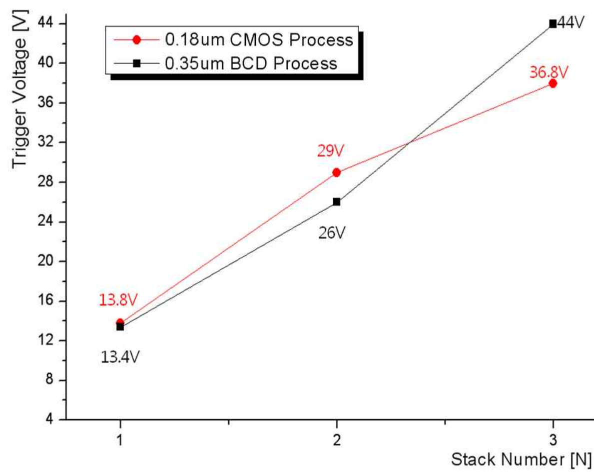
C. Temperature characteristics

In order to analyze the temperature dependency of the stacking structure, measurements were taken at various temperatures (300K-500K). The holding voltage at different temperatures is shown in Fig. 7. At higher temperature, the holding voltage of the stacking structures is reduced by the parasitic bipolar transistors. The holding voltage is the sum of the turn-on voltages (base-emitter voltage) of the parasitic bipolar transistors (i.e., $V_{BE}(Q1_{PNP})$, $V_{BE}(Q3_{NPN})$ in Fig. 1(a)). An elevation in temperature led to an increase in the diode saturation current of the parasitic bipolar transistor and this is a critical factor in ESD operation. As a result, the base-emitter voltage of the NPN and PNP transistors as well as the overall holding voltage were decreased.

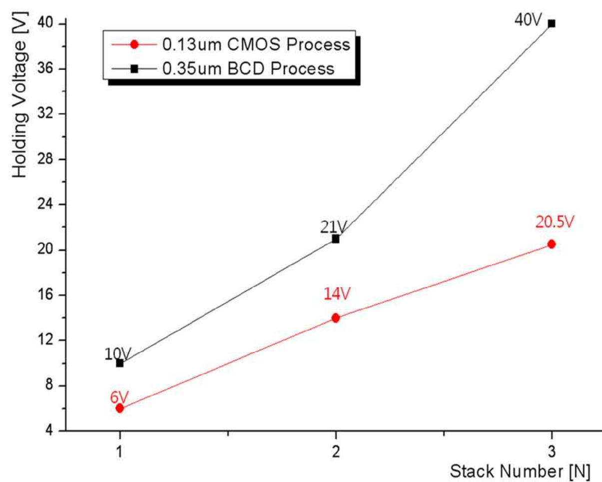
IV. CONCLUSIONS

This paper presented a SCR stacking structure with a high holding voltage for latch-up immune high voltage applications. Silicon proven results were obtained in 0.18um CMOS and 0.35um BCD technologies. The stacking structure was built by using individual SCRs that possess a high holding voltage and a high ESD robustness. By selecting the correct stacking number, the holding voltage of the stacking SCRs can be flexibly adjusted to meet the required latch-up immunity. Moreover, the temperature dependence of the holding voltage over a wide temperature range was investigated. A high temperature led to a reduction in the turn-on voltage, namely

the parasitic BJT emitter-base voltage. Therefore, the holding voltage decreased.



(a)



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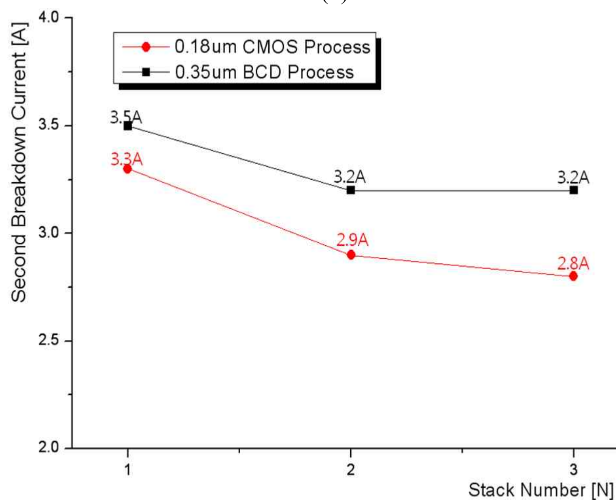
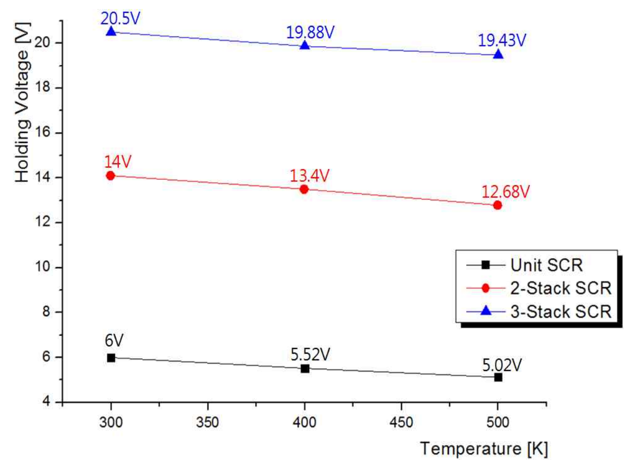


(c)

Fig. 6. Extracted (a) trigger voltage, (b) holding voltage and (c) second breakdown current values for the SCR-based device stacks.



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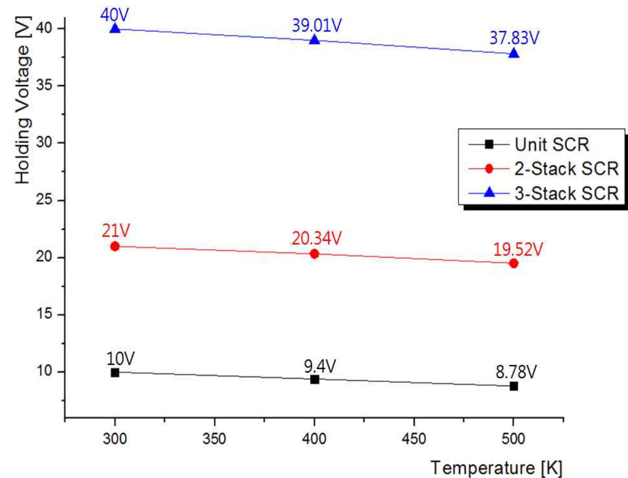

(b)

Fig. 7. Measurement of holding voltage dependence on the different temperatures (300K-500K) (a) in a 0.18um CMOS and (b) 0.35um BCD technology.

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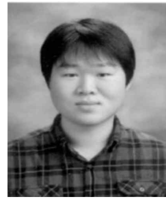
Yong Seo Koo was born in Seoul, Republic of Korea, in 1957. He received his B.S., M.S. and Ph.D. in Electronic Engineering from Sogang University, Seoul, Republic of Korea, in 1981, 1983 and 1992, respectively. He joined the Department of Electronics and Electrical Engineering, Dankook University as a Professor, in 2009. His current research interests include semiconductor devices, such as power BJTs, LDMOSs, and IGBTs; high-efficiency power management integrated circuits (PMICs), such as DC-DC converters; and electrostatic discharge (ESD) protection circuit design.



Dong Su Kim was born in Seoul, Republic of Korea, in 1986. He received his B.S. in Electronic Engineering from Seokyeong University, Seoul, Republic of Korea, in 2010. He is currently working toward his M.S. in Electrical and Electronics Engineering from Dankook University, Yongin, Republic of Korea. His current research interests include electrostatic discharge (ESD) protection and power devices.

Jin Woo Eo was born in JInhae, Republic of Korea, in 1955. He received his B.S. in Electrical Engineering from Seoul National University, Seoul, Republic of Korea, in 1979, and his M.S. and Ph.D. in Electrical and Computer Engineering from Oregon State University, Oregon, USA, in 1988 and 1992, respectively. He joined the Department of Electronics and Electrical Engineering, Dankook University, Yongin, Republic of Korea, as a Professor, in 1992. His current research interests include image signal processing, and analysis of electrical characteristics of electrostatic discharge (ESD) protection circuits.