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# Analysis, Design and Implementation of a Soft Switching DC/DC Converter

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**Abstract**

This paper presents a soft switching DC/DC converter for high voltage application. The interleaved pulse-width modulation (PWM) scheme is used to reduce the ripple current at the output capacitor and the size of output inductors. Two converter cells are connected in series at the high voltage side to reduce the voltage stresses of the active switches. Thus, the voltage stress of each switch is clamped at one half of the input voltage. On the other hand, the output sides of two converter cells are connected in parallel to achieve the load current sharing and reduce the current stress of output inductors. In each converter cell, a half-bridge converter with the asymmetrical PWM scheme is adopted to control power switches and to regulate the output voltage at a desired voltage level. Based on the resonant behavior by the output capacitance of power switches and the transformer leakage inductance, active switches can be turned on at zero voltage switching (ZVS) during the transition interval. Thus, the switching losses of power MOSFETs are reduced. The current doubler rectifier is used at the secondary side to partially cancel ripple current. Therefore, the root-mean-square (*rms*) current at output capacitor is reduced. The proposed converter can be applied for high input voltage applications such as a three-phase 380V utility system. Finally, experiments based on a laboratory prototype with 960W (24V/40A) rated power are provided to demonstrate the performance of proposed converter.

**Key words:** DC/DC converter, Soft Switching

## I. INTRODUCTION

The size reduction of the switching mode power converter has been demanded and researched for the compact high voltage converters such as medical imaging, aerospace and military electronics. Normally the switching converters are composed of an AC/DC converter and an isolated DC/DC converter. To eliminate the current harmonics and meet the harmonic limitation by international standards IEC 61000-3-2, power factor correction (PFC) topologies are used in the AC/DC conversion. Normally the output voltage of the AC/DC converter is higher than the peak value of the input high line AC voltage. To overcome the voltage limitation of power MOSFETs, the series connection of active switches or multilevel topologies can be used in high voltage applications. However, the voltage balance problem across the active switches is difficult to overcome in the series connection of active switches. Multilevel topologies [1]-[10] are more effective to solve the voltage limitation of MOSFETs. However, the drawback of the multilevel converters is too complicated to be implemented by using the commercial PWM IC. For the medium or high power applications, the interleaving techniques [11]-[14] with phase-shifting of the control signals of several cells connected in parallel can reduce the current stresses of power switches and further reduce the ripple current on input and output capacitors. Asymmetrical pulse-width modulation (PWM) [15]-[19] have been proposed to realize the magnetizing flux reset. Thus the voltage spike and the voltage stresses on power MOSFETs can be reduced to a safety region. Based on the resonant behavior at the transition interval of active switches, active switches can be turned on at zero voltage switching (ZVS). Thus the circuit efficiency can be improved.

This paper presents a soft switching converter to realize ZVS turn-on for all switches. There are two series-connected half-bridge converters in the proposed circuit to reduce the voltage stresses of power switches, to share the load current, and to reduce the ripple current on output capacitor. Based on the resonant behavior at the transition interval of power switches, MOSFETs can be turned on at ZVS. Two converter modules are connected in series at the input side and connected in parallel at the output side. Thus the voltage

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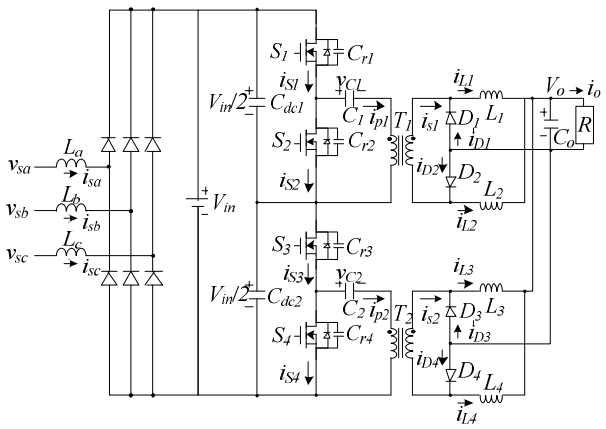


Fig. 1. Circuit configuration of the proposed interleaved ZVS converter.

stresses of active switches are reduced to one-half of the input voltage. The current doubler rectifiers are used in the secondary side to partially cancel the ripple current so that the size of the output chokes and the output capacitor can be reduced. Finally, experiments based on a 960W (24V/40A) prototype are presented to verify the theoretical analysis and the effectiveness of the proposed converter.

## II. CIRCUIT CONFIGURATION

Fig. 1 gives the circuit configuration of the proposed interleaved ZVS converter. Two split capacitors and two half-bridge converters are connected in series at the primary side to reduce the voltage stress of active switches at one-half of the DC bus voltage and connected in parallel at the secondary side to achieve load current sharing. Two half-bridge converters are operated with interleaved PWM scheme such that the ripple current on the output capacitor are reduced. Capacitances $C_{dc1}$ and $C_{dc2}$ are large enough to be considered as two constant input voltages. In the same manner, the output voltage $V_o$ is considered to be constant at the desired value. The first half-bridge converter includes $C_{dc1}$, $S_1$, $S_2$, $C_{r1}$, $C_{r2}$, $C_1$, $T_1$, $D_1$, $D_2$, $L_1$ and $L_2$. In the same manner, the components of the second half-bridge converter includes $C_{dc2}$, $S_3$, $S_4$, $C_{r3}$, $C_{r4}$, $C_2$, $T_2$, $D_3$, $D_4$, $L_3$ and $L_4$. $C_o$ and $R$ denote the output capacitance and load resistance. The PWM signals of $S_1$ and $S_3$ are phase-shifted by one-half of the switching period. The gate signals of $S_1$ and $S_2$ in the first half-bridge converter are complementary each other with a dead time. In the same manner, the gate signals of $S_3$ and $S_4$ in the second half-bridge converter are complementary. The output inductor currents in each current doubler rectifier are partially cancelled each other so that the output ripple current is reduced and the size of the output capacitance and inductances can be reduced. The leakage inductances of transformers and the capacitances $C_{r1}$-$C_{r4}$ are resonant during the transition interval. Thus power switches $S_1$-$S_4$ can be turned on at ZVS.

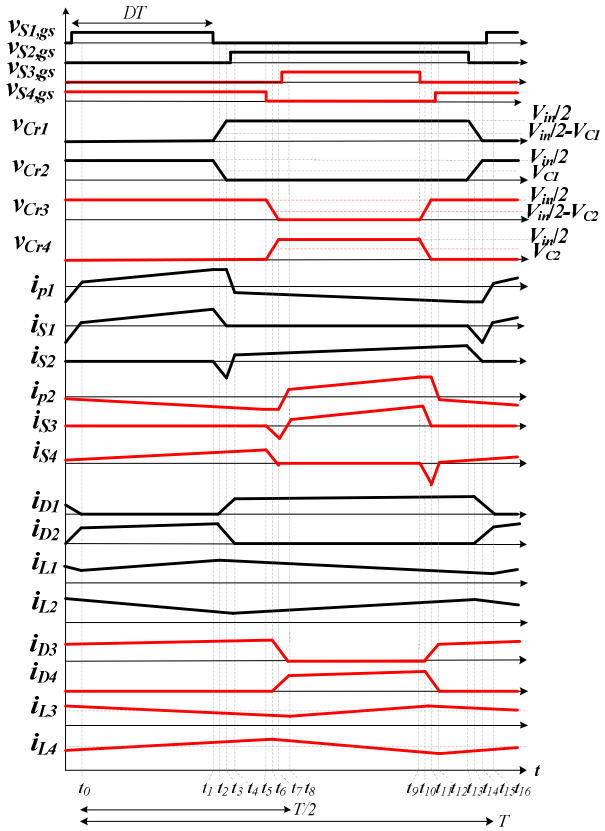


Fig. 2 Key waveforms of proposed converter.

## III. OPERATION PRINCIPLE

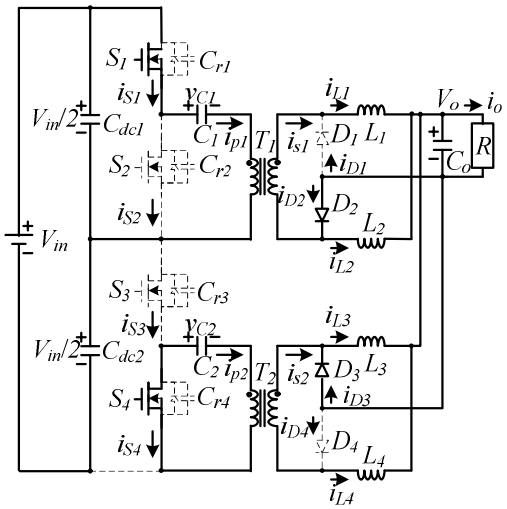
The theoretical waveforms of the proposed converter during one switching cycle are shown in Fig. 2. The duty cycles of switches $S_1$ and $S_3$ are $D$. The following assumptions are made to simplify the system analysis.

- Active switches $S_1$-$S_4$ and diodes $D_1$-$D_4$ are ideal.
- All the inductors and capacitors are ideal.
- $L_{lk1}=L_{lk2}=L_{lk}$, $L_{11}=L_{12}=L_{21}=L_{22}=L_o$, and $L_{m1}=L_{m2}=L_m$.
- The turns ratio of $T_1$ and $T_2$ is represented as $n=N_p/N_s$.
- The leakage inductance $L_{lk}<<L_m$ such that the voltage drop on $L_{lk}$ can be neglected.
- Resonant capacitances $C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_r$ and the clamp capacitances $C_1=C_2=C_c>>C_r$.

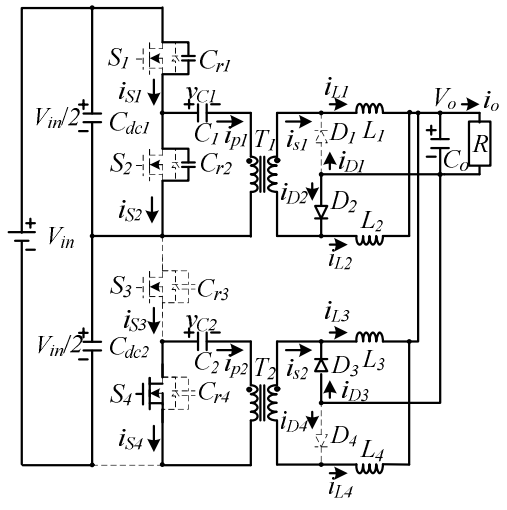
The proposed converter has sixteen operation modes during one switching period. Fig. 3 shows the equivalent circuits of the eight operation modes in the first half switching period. The PWM waveforms in the second half switching period are phase-shifted $T_s/2$ with respective to the PWM signals in the first half switching period. Before time $t_0$, $S_1$, $S_4$ and $D_1$-$D_3$ are conducting. Diode current $i_{D1}$ decreases and $i_{D2}$ increase.

**Mode 1 [$t_0 \le t < t_1$]:** This mode starts at $t_0$ and switches $S_1$ and $S_4$ are conducting. The primary voltages $v_{T1,p} \approx V_{in}/2 - V_{C1}$ and $v_{T2,p} \approx -V_{C2}$. Thus, the magnetizing currents $i_{Lm1}$ and $i_{Lm2}$ increase and decrease, respectively. The secondary winding

voltages of $T_1$ and $T_2$ are positive and negative, respectively, so that diodes $D_2$ and $D_3$ are forward biased. Since the inductor voltages $v_{L1}=(V_{in}/2n-V_{C1}/n-V_o)>0$ and $v_{L2}=-V_o<0$, the inductor current $i_{Lo1}$ increases and $i_{L2}$ decreases in this mode. The ripple currents on inductors $L_1$ and $L_2$ partially cancel so that the ripple current on the output of converter 1 is reduced. Power is transferred from $V_{in}/2$ to $R$ through $S_1$, $C_1$, $T_1$, $L_1$, $C_o$ and $D_2$. The switch current $i_{S1}=i_{p1}=i_{Lm1}+i_{s1}/n$. In the same manner, the inductor voltages $v_{L3}=-V_o<0$ and $v_{L4}=(V_{C2}/n-V_o)>0$. The inductor current $i_{L3}$ decreases and $i_{L4}$ increases in this mode so that the ripple current on the output of converter 2 is also reduced. Energy stored on the capacitor $C_2$ is transferred to output load through $S_4$, $T_2$, $L_4$, $C_o$, and $D_3$. The switch current $i_{S4}=-i_{p2}=-i_{Lm2}-i_{s2}/n$. This mode ends at $t_1$ when switch $S_1$ is turned off.




(a)

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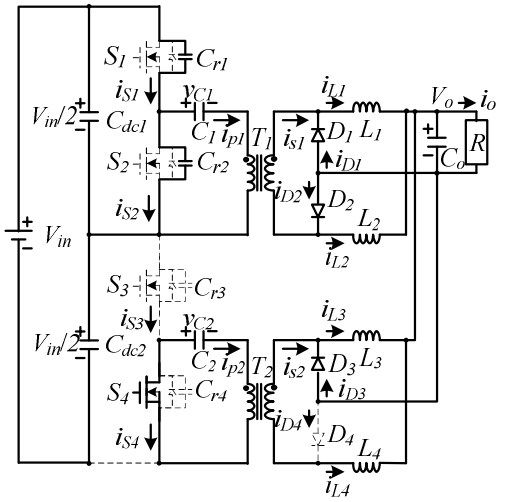


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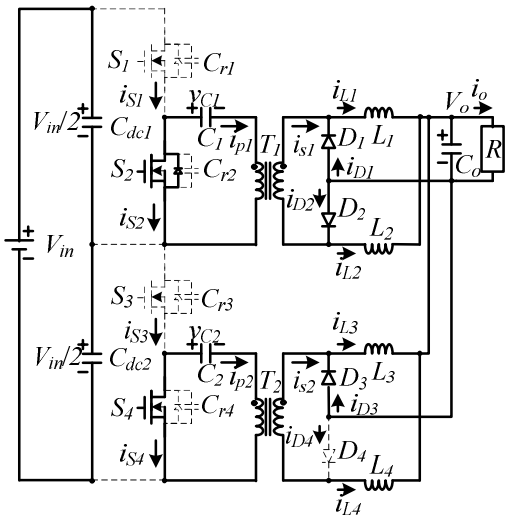


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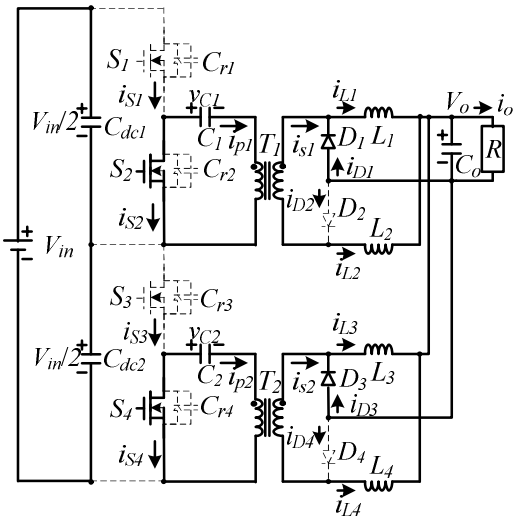


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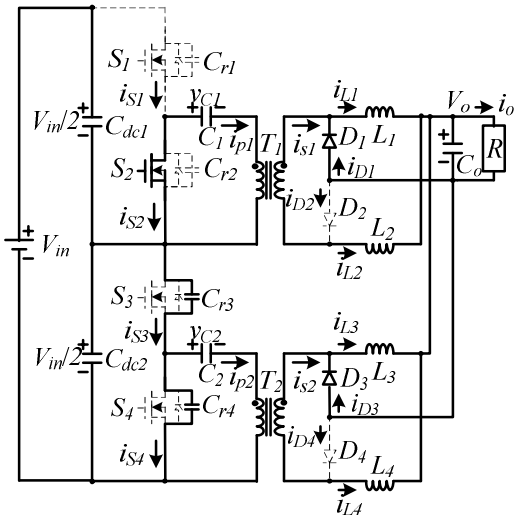
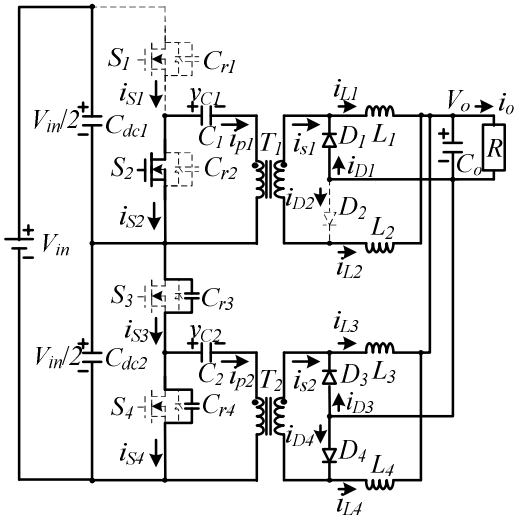



(f)

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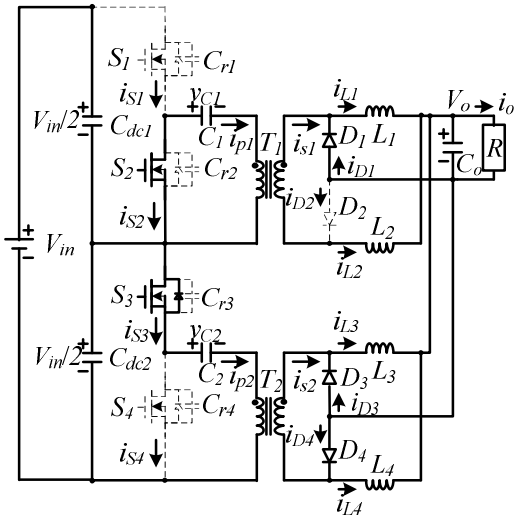


(h)

Fig. 3. Equivalent circuits of the proposed converter during first half of one switching period (a) mode 1 (b) mode 2 (c) mode 3 (d) mode 4 (e) mode 5 (f) mode 6 (g) mode 7 (h) mode 8.

**Mode 2 [$t_1 \le t < t_2$]:** At $t_1$, switch $S_1$ is turned off. The positive primary current $i_{p1}$ charges $C_{r1}$ and discharges $C_{r2}$. Since $C_{r1}$, $C_{r2} << C_1$, $v_{Cr1}$ and $v_{Cr2}$ are approximately increased and decreased linearly with the slope of $i_{p1}(t_1)/(2C_r)$. The primary current $i_{p1}$ is almost constant in this mode. The operation behavior of the second half-bridge converter in this mode is the same as the circuit operation in mode 1. This mode ends at $t_2$ when $v_{Cr2}=V_{C1}$. Then the primary voltage of $T_1$ is zero.

**Mode 3 [$t_2 \le t < t_3$]:** At $t_2$, the capacitor voltage $v_{Cr2}=v_{C1}$. At this instant, the primary and secondary winding voltages $v_{T1,p}=v_{T1,s}=0$. Thus diodes $D_1$ and $D_2$ are conducting to commutate the inductor currents $i_{L1}$ and $i_{L2}$. Thus the inductor voltages $v_{L1}=v_{L2}=-V_o$. The inductor currents $i_{L1}$ and $i_{L2}$ both decrease in this mode. The diode current $i_{D1}$ increases and diode current $i_{D2}$ decreases. $C_{r1}$ and $C_{r2}$ are continuously charged and discharged by the primary current $i_{p1}$ in this mode. The operation behavior of converter 2 in this mode is the same as the circuit operation in mode 1. If the energy stored in $L_{lk1}$ is greater than the energy stored in $C_{r1}$ and $C_{r2}$, then $C_{r2}$ can be discharged to zero voltage. This mode ends at $t_3$ when $v_{Cr2}=0$. At this instant, the anti-parallel diode of $S_2$ is conducting. The time interval in modes 2 and 3 can be approximately expressed as:

$$\Delta t_{13} = t_3 - t_1 \approx C_r V_{in} / i_{p1}(t_1) \tag{1}$$

The dead time $t_d$ between $S_1$ and $S_2$ must be greater than the time interval in (1) to achieve ZVS turn-on for switch $S_2$.

**Mode 4 [$t_3 \le t < t_4$]:** At $t_3$, $v_{Cr2}=0$. Since $i_{S2}=-i_{p1}=-(i_{Lm1}+i_{s1}/n)<0$, the anti-parallel diode of $S_2$ is conducting. Before $i_{S2}$ is positive, $S_2$ must be turned on to achieve ZVS. Since $D_1$ and $D_2$ are still in the commutation interval, the leakage inductance voltage of $T_1$ equals $-V_{C1}$. Thus, the primary current $i_{p1}$ decreases rapidly with the slope of $-V_{C1}/L_{lk}$. This mode ends at $t_4$ when $i_{D2}$ decreases to zero. The time interval in this mode is given as:

$$\Delta t_{34} = t_4 - t_3 \approx \frac{L_{lk} I_o}{2nV_{C1}} \tag{2}$$

In this mode, $S_2$ is in the on-state and the output inductor voltage $v_{L1}=v_{Lo2}=-V_o$. Thus, the duty loss in this mode is given as:

$$D_{loss,4} = \frac{\Delta t_{34}}{T_s} \approx \frac{L_{lk} I_o f_s}{2nV_{C1}} \tag{3}$$

where $T_s$ and $f_s$ are the switching period and switching frequency.

**Mode 5 [$t_4 \le t < t_5$]:** At $t_4$, $i_{D2}=0$. Thus, $D_2$ is off and the diode current $i_{D1}=i_{L1}+i_{L2}=I_o/2$. Since $S_2$ and $S_4$ are conducting, the primary voltages $v_{T1,p} \approx -V_{C1} < 0$ and $v_{T12,p} \approx -V_{C2} < 0$. Thus, the primary currents $i_{p1}$ and $i_{p2}$ both decrease in this mode. Energy stored in $C_1$ and $C_2$ is delivered to output load through transformers $T_1$ and $T_2$, respectively. The inductor voltages $v_{L1}=v_{L3}=-V_o$ so that the inductor currents $i_{L1}$ and $i_{L3}$ both decrease. However, the inductor voltages $v_{L2}=v_{C1}/n-V_o>0$ and $v_{L4}=v_{C2}/n-V_o>0$. Thus, the inductor currents $i_{L2}$ and $i_{L4}$ increase. This mode ends at $t_5$ when $S_4$ is turned off.

**Mode 6 [$t_5 \le t < t_6$]:** At $t_5$, $S_4$ is turned off. Since the primary current $i_{p2}(t_5)<0$, $C_{r3}$ and $C_{r4}$ are discharged and charged, respectively. Since $C_{r3}$ and $C_{r4}$ are much less than $C_2$, $C_{r3}$ and $C_{r4}$ decrease and increase linearly with the slope of $i_{p2}(t_5)/(2C_r)$. The primary current $i_{p2}$ is almost constant in this mode. The operation behavior of converter 1 in this mode is the same as the circuit operation in mode 5. This mode ends at $t_6$ when the capacitor voltage $v_{Cr4}=v_{C2}$. Then the primary voltage of $T_2$ is zero.

**Mode 7 [$t_6 \le t < t_7$]:** At $t_6$, $v_{Cr4}(t_6)=v_{C2}$. The primary and secondary winding voltages $v_{T2,p}=v_{T2,s}=0$ and diodes $D_3$ and $D_4$ are both conducting to commutate the inductor currents $i_{L3}$ and $i_{L4}$. The output inductor voltages $v_{L3}=v_{L4}=-V_o$ and the inductor currents $i_{L3}$ and $i_{L4}$ decrease in this mode. The diode current $i_{D3}$ decreases and $i_{D4}$ increases in this mode. The operation behavior of converter 1 in this mode is the same as the circuit operation in mode 5. If the energy stored in $L_{lk2}$ is greater than the energy stored in $C_{r3}$ and $C_{r4}$, then capacitor $C_{r3}$ can be discharged to zero voltage. This mode ends at $t_7$ when $v_{Cr3}=0$. At this instant, the anti-parallel diode of $S_3$ is conducting. The time interval in modes 6 and 7 can be approximately expressed as:

$$\Delta t_{57} = t_7 - t_5 \approx \frac{C_r V_{in}}{i_{p2}(t_5)} \tag{4}$$

The dead time $t_d$ between $S_3$ and $S_4$ must be greater than the time interval in (4) to achieve ZVS turn-on of $S_3$.

**Mode 8 [$t_7 \le t < t_8$]:** At $t_7$, $v_{Cr3}=0$. Since the primary current $i_{p2}(t_7)<0$, the anti-parallel diode of $S_3$ is conducting. Before $i_{S3}$ is positive, $S_3$ must be turned on to achieve ZVS. In this mode, the diodes $D_3$ and $D_4$ are still in the commutation state. The voltage across the leakage inductor of $T_2$ equals $V_{in}/2$. Thus the primary current $i_{p2}$ increases rapidly with the slope of $(V_{in}/2-V_{C2})/L_{lk}$. This mode ends at $t_8$ when $i_{D3}=0$. The time interval in this mode is approximately given as:

$$\Delta t_{78} = t_8 - t_7 \approx \frac{L_{lk} I_o}{2n(V_{in}/2 - V_{C2})} \tag{5}$$

In this mode, $S_3$ is in the on-state and the output inductor voltage $v_{L3}=v_{L4}=-V_o$. Thus the duty loss in this mode is given as:

$$D_{loss,8} = \frac{\Delta t_{78}}{T_s} \approx \frac{L_{lk} I_o f_s}{2n(V_{in}/2 - V_{C2})} \tag{6}$$

Then the operating modes of the proposed converter in the first half of switching period are completed.

## IV. Circuit Characteristics

Since the transition intervals at the turn-on and turn-off transition instants are much less than the turn-on time of active switches, the transition intervals can be neglected. From the volt-second balance on primary windings of $T_1$ and $T_2$, the capacitor voltages $V_{C1}$ and $V_{C2}$ are expressed as:

$$V_{C1} = V_{C2} = \frac{DV_{in}}{2} \tag{7}$$

where $D$ is the duty cycle of $S_1$ and $S_3$. Based on the volt-second balance on the output inductors $L_1$-$L_4$ at steady state, we can obtain the DC voltage conversion ratio of the proposed converter.

$$\frac{V_o + V_f}{V_{in}} = \frac{D(1 - D - D_{loss,4})}{2n} \tag{8}$$

where $V_f$ is the voltage drop on $D_1$-$D_4$, and $D_{loss,4}$ is the duty loss in mode 4. The duty loss in mode 4 can be obtained from (3) and (7).

$$D_{loss,4} \approx \frac{L_{lk} I_o f_s}{2nV_{C1}} = \frac{L_{lk} I_o f_s}{nDV_{in}} \tag{9}$$

From (8) and (9), the final output voltage of the proposed converter is expressed as:

$$V_o = \frac{V_{in}}{2n}\left[D(1-D) - \frac{L_{lk} I_o f_s}{nV_{in}}\right] - V_f \tag{10}$$

From (10), the output voltage $V_o$ is related to the duty cycle $D$, input voltage $V_{in}$, the switching frequency $f_s$, the leakage inductance $L_{lk}$ and load current $I_o$. In steady state, the average current on the secondary side of $T_1$ is zero and the sum of the average inductor currents $I_{L1}$ and $I_{L2}$ equal $I_o/2$. Thus, the average output inductor currents in converter 1 are given as:

$$I_{L1} = (1-D)I_o/2, \quad I_{L2} = DI_o/2 \tag{11}$$

In the same manner, the average output inductor currents in converter 2 are expressed as:

$$I_{L3} = (1-D)I_o/2, \quad I_{L4} = DI_o/2 \tag{12}$$

The ripple currents on output inductors can be given as:

$$\Delta i_{L1} = \Delta i_{L3} = \frac{V_o(1-D)T_s + \dfrac{V_o L_{lk} I_o}{nV_{in}(1-D)}}{L_1} \tag{13}$$

$$\Delta i_{L2} = \Delta i_{L4} = \frac{V_o D T_s + \dfrac{V_o L_{lk} I_o}{nDV_{in}}}{L_2} \tag{14}$$

Thus, the maximum and minimum output inductor currents are given as:

$$i_{L1,\max} = i_{L3,\max} = \frac{(1-D)I_o}{2} + \frac{V_o(1-D)T_s + \dfrac{V_o L_{lk} I_o}{nV_{in}(1-D)}}{2L_1} \tag{15}$$

$$i_{L1,\min} = i_{L3,\min} = \frac{(1-D)I_o}{2} - \frac{V_o(1-D)T_s + \dfrac{V_o L_{lk} I_o}{nV_{in}(1-D)}}{2L_1} \tag{16}$$

$$i_{L2,\max} = i_{L4,\max} = \frac{DI_o}{2} + \frac{V_o D T_s + \dfrac{V_o L_{lk} I_o}{nDV_{in}}}{2L_2} \tag{17}$$

$$i_{L2,\min} = i_{L4,\min} = \frac{DI_o}{2} - \frac{V_o DT_s + \frac{V_o L_{lk} I_o}{nDV_{in}}}{2L_2} \quad (18)$$

Based on the theoretical waveforms shown in Fig. 2, the switch current $i_{S1}=i_{p1}\approx I_{L1}/n+I_{Lm,T1}$ when $S_1$ is turned on. When $S_2$ is turned on with the time interval $(1\text{-}D)T$, the switch current $i_{S2}=I_{L2}/n\text{-}I_{Lm,T1}$. Since the average current on capacitor $C_1$ is zero, the average magnetizing current $I_{Lm,T1}$ can be obtained as:

$$I_{Lm,T1}=0 \quad (19)$$

In the same manner, we can obtain the average magnetizing current $I_{Lm,T2}=0$. The ripple currents of $L_{m1}$ and $L_{m2}$ can be expressed as:

$$\Delta i_{Lm} \approx [D(1-D)V_{in}T_s - \frac{L_{lk}I_o}{n}]/(2L_m) \quad (20)$$

Thus, the maximum and minimum magnetizing currents are given as:

$$i_{Lm,\max} = \frac{D(1-D)V_{in}T_s - \frac{L_{lk}I_o}{n}}{4L_m} \quad (21)$$

$$i_{Lm,\min} = -\frac{D(1-D)V_{in}T_s - \frac{L_{lk}I_o}{n}}{4L_m} \quad (22)$$

The average currents on $D_1$-$D_4$ are expressed as:

$$I_{D1,\text{av}} = I_{D3,av} = (1-D)I_o/2\,,\ I_{D2,\text{av}} = I_{D4,av} = DI_o/2 \quad (23)$$

The root-mean-square (*rms*) currents of $D_1$-$D_4$ are expressed as:

$$i_{D1,\text{rms}} = i_{D3,rms} = \frac{I_o}{2}\sqrt{1-D}\,,\ \ i_{D2,\text{rms}} = i_{D4,rms} = \frac{I_o}{2}\sqrt{D} \quad (24)$$

The voltage stresses of $D_1$-$D_4$ are given as:

$$v_{D1,\text{stress}} = v_{D3,\text{stress}} = (1-D)V_{in}/(2n) \quad (25)$$

$$v_{D2,\text{stress}} = v_{D4,\text{stress}} = DV_{in}/(2n) \quad (26)$$

The peak current of switch $S_1$ approximates the peak value of $i_{p1}$ and can be expressed as:

$$i_{S1,peak} \approx I_{L1}/n + \Delta i_{L1}/2 + \Delta i_{Lm,T1}/2 \quad (27)$$

where $\Delta i_{L1}$ and $\Delta i_{Lm,T1}$ are the ripple currents on $L_1$ and $L_{m,T1}$, respectively. In the same manner, the peak values of $S_2$-$S_4$ are expressed as:

$$i_{S2,peak} \approx I_{L2}/n + \Delta i_{L2}/2 + \Delta i_{Lm,T1}/2 \quad (28)$$

$$i_{S3,peak} \approx I_{L3}/n + \Delta i_{L3}/2 + \Delta i_{Lm,T2}/2 \quad (29)$$

$$i_{S4,peak} \approx I_{L4}/n + \Delta i_{L4}/2 + \Delta i_{Lm,T2}/2 \quad (30)$$

If the ripple currents on $S_1$-$S_4$ are negligible, the *rms* currents of switches $S_1$-$S_4$ are approximately given as:

$$i_{S1,rms} = i_{S3,rms} \approx (1-D)I_o\sqrt{D}/(2n) \quad (31)$$

$$i_{S2,rms} = i_{S4,rms} \approx DI_o\sqrt{1-D}/(2n) \quad (32)$$

The voltage stresses of $S_1$-$S_4$ are expressed as:

$$v_{S1,stress} = v_{S2,stress} = v_{S3,stress} = v_{S4,stress} = V_{in}/2 \quad (33)$$

At $t_2$ in mode 3, the inductor current $i_{p1}(t_2)$ is approximately given as:

$$i_{p1}(t_2) = i_{p2}(t_{10}) \approx i_{Lm1,\max} + \frac{i_{L1,\max}}{n} \approx \frac{D(1-D)V_{in}T_s - \frac{L_{lk}I_o}{n}}{4L_m} + \frac{(1-D)I_o}{2n} + \frac{V_o(1-D)T_s + \frac{V_o L_{lk} I_o}{nV_{in}(1-D)}}{2nL_1} \quad (34)$$

At $t_6$ in mode 7, the inductor current $i_{Lr2}(t_6)$ is approximately given as:

$$i_{p2}(t_6) = i_{p1}(t_{14}) \approx i_{Lm2,\min} - \frac{i_{L4,\max}}{n} \approx -\frac{D(1-D)V_{in}T_s - \frac{L_{lk}I_o}{n}}{4L_m} - \frac{DI_o}{2n} - \frac{V_o DT_s + \frac{V_o L_{lk} I_o}{nDV_{in}}}{2nL_2} \quad (35)$$

The ZVS conditions of $S_1$-$S_4$ are given in (36)-(39) respectively.

$$L_{lk1} \ge \frac{(1-D)C_r V_{in}^2}{2i_{p1}^2(t_{14})} \quad (36)$$

$$L_{lk1} \ge \frac{DC_r V_{in}^2}{2i_{p1}^2(t_2)} \quad (37)$$

$$L_{lk2} \ge \frac{(1-D)C_r V_{in}^2}{2i_{p2}^2(t_6)} \quad (38)$$

$$L_{lk2} \ge \frac{DC_r V_{in}^2}{2i_{p2}^2(t_{10})} \quad (39)$$

From (36)-(39), the ZVS condition of $S_1$-$S_4$ can be expressed as:

$$L_{lk} = L_{lk1} = L_{lk2} \ge \max\{\frac{DC_r V_{in}^2}{2i_{p1}^2(t_2)},\ \frac{(1-D)C_r V_{in}^2}{2i_{p1}^2(t_{14})}\} \quad (40)$$

We assume that the voltage ripple of DC blocking capacitors $C_1$ and $C_2$ is less than 20% of its average voltage.

$$\Delta v_{C1} = \frac{1}{C_c}\int_0^{DT} i_{p1}dt \approx \frac{D(1-D)I_o T_s}{2nC_c} < 0.2V_{C1} = \frac{DV_{in}}{10} \quad (41)$$

Thus, the DC blocking capacitance $C_c=C_1=C_2$ is given as:

$$C_c > \frac{5(1-D)I_o}{nV_{in}f_s} \quad (42)$$

## V. Design Procedure and Experimental Results

The design example of a laboratory prototype with 960W (24V/40A) is presented in this section. The nominal input terminal voltage $V_{in,nom}$ is 800V, and the minimum and maximum input voltages are 750V and 850V, respectively. The switching frequency of the proposed converter is $f_s$=130*kHz*. The assumed circuit efficiency is 90%.

*A. Leakage inductance of $T_1$ and $T_2$*

The maximum duty cycle of $S_1$ and $S_3$ is 0.45 at the minimum input voltage and full load condition. The maximum duty cycle loss in modes 4 and 16 is assumed to be 10% at full load with duty cycle $D=0.5$.

$$D_{loss,T} = D_{loss,4} + D_{loss,16} \approx \frac{4I_oL_{lk}f_s}{nV_{in}} \approx \frac{32P_oL_{lk}f_s}{\eta V_{in}^2} < 0.1 \quad (43)$$

Thus, the leakage inductances of $L_{lk1}$ and $L_{lk2}$ are expressed as :

$$L_{lk} < \frac{\eta V_{in,\max}^2 D_{loss,T}}{32P_of_s} = \frac{0.9\times 850^2\times 0.1}{32\times 960\times 130000} \approx 16.3\mu H \quad (44)$$

*B. Turns ratio and winding turns of $T_1$ and $T_2$*

The turns ratio of $T_1$~$T_4$ can be obtained from (10).

$$n \approx \frac{D_{\max}(1-D_{\max})V_{in,\min} + \sqrt{[D_{\max}(1-D_{\max})V_{in,\min}]^2 - 8(V_o+V_f)I_oL_{lk}f_f}}{4(V_o+V_f)} \quad (45)$$

$$\approx 3.23$$

We select the primary winding turns $N_p=88$ and the secondary winding turns $N_s=27$. We assume that the magnetizing ripple current on $L_m$ is 0.8A. The magnetizing inductacne can be obtained from (20).

$$L_m \approx \frac{D_{\max}(1-D_{\max})V_{in,\min}T_s - \frac{L_{lk}I_o}{n}}{2\Delta i_{Lm}} \quad (46)$$

$$= \frac{0.45\times(1-0.45)\times 750/130000 - \frac{16.3\times 10^{-6}\times 40}{88/27}}{2\times 0.8} = 0.77mH$$

From (10) and (45), the minimum duty cycle at the maximum input voltage and full load is given as :

$$D_{\min} \approx [1 - \sqrt{1 - \frac{8n(V_o+V_f)}{V_{in,\max}} - \frac{4L_{lk}I_of_s}{nV_{in,\max}}}]/2 \approx 0.33 \quad (47)$$

*C. Output inductance of $L_1$~$L_4$*

In (13)-(14), we set 30% ripple current on inductors $L_1$~$L_4$ at $D=0.5$ case. Thus, the output inductances $L_1$~$L_4$ can be obtained as:

$$L_1 = L_2 = L_3 = L_4 = \frac{V_o(1-D)T_s + \frac{V_oL_{lk}I_o}{nV_{in}(1-D)}}{\Delta i_{L1}} \quad (48)$$

$$\approx \frac{24\times(1-0.5)/130000 + \frac{24\times 16.3\times 10^{-6}\times 40}{(88/27)\times 850\times(1-0.5)}}{0.3\times 10} \approx 34.5\mu F$$

*D. Current and voltage stresses of $S_1$~$S_4$ :*

Based on (31)-(33), the *rms* currents and voltage stresses of $S_1$-$S_4$ are given as:

$$i_{S1,rms} = i_{S3,rms} \approx (1-D_{\min})I_o\sqrt{D_{\min}}/(2n) \quad (49)$$

$$= (1-0.33)\times 40\times\sqrt{0.33}/(2\times 88/27) \approx 2.36A$$

$$i_{S2,rms} = i_{S4,rms} \approx D_{\max}I_o\sqrt{1-D_{\max}}/(2n) \quad (50)$$

$$= 0.45\times 40\times\sqrt{1-0.45}/(2\times 88/27) = 2.05A$$

$$v_{S1,stress} = v_{S2,stress} = v_{S3,stress} = v_{S4,stress} = V_{in,\max}/2 = 425V \quad (51)$$

The IRFP460 MOSFETs with $V_{DS}$=500V, $I_{D,rms}$=20A, $R_{DS,on}$=0.27Ω and $C_{oss}$=480pF at 25V are used for switches $S_1$-$S_4$.

*E. Current and voltage stresses of $D_1$~$D_4$*

From (23)-(26), the average currents and the voltage stresses on the rectifier diodes are given as:

$$I_{D1,\text{av}} = I_{D3,av} = (1-D_{\min})I_o/2 = (1-0.33)\times 40/2 = 13.4A,$$
$$I_{D2,\text{av}} = I_{D4,av} = D_{\max}I_o/2 = 0.45\times 40/2 = 9A \quad (52)$$

$$v_{D1,\text{stress}} = v_{D3,\text{stress}} = (1-D_{\min})V_{in,\max}/(2n)$$
$$= (1-0.33)\times 850/(2\times 88/27) = 87.4V$$
$$v_{D2,\text{stress}} = v_{D4,\text{stress}} = D_{\max}V_{in,\min}/(2n) \quad (53)$$
$$= 0.45\times 750/(2\times 88/27) \approx 51.8V$$

The MUR1520 ultrafast diodes with $V_{RRM}$=150V and $I_F$=20A are used for the rectifier diodes at the secondary side.

*F. ZVS conditions of $S_1$~$S_4$*

We assume that the ZVS range of $S_1$-$S_4$ is at least from 50% load to 100% load at the nominal input voltage. The duty cycle at 50% load and the maximum input voltage is obtained as :

$$D_{50\%} \approx \frac{1 - \sqrt{1 - \frac{8n(V_o+V_f)}{V_{in,\max}} - \frac{4L_{lk}I_{o,50\%}f_s}{nV_{in,\max}}}}{2} \approx 0.286 \quad (54)$$

Since $C_{oss}$ of the IRFP460 MOSFETs is 480pF at 25V, the equivalent output capacitance $C_r$ at the maximum input voltage is given as:

$$C_r \approx \frac{4}{3}C_{oss,25}\sqrt{\frac{25}{v_{S1,ds}}} = \frac{4}{3}\times 480\times\sqrt{\frac{25}{850/2}} \approx 155pF \quad (55)$$

From (34) and (35), the inductor currents $i_{p1}(t_2)$ and $i_{p1}(t_{14})$ at 50% load and $D_{50\%}$=0.286 case can be obtained as:

$$i_{p1}(t_2) \approx \frac{D_{50\%}(1-D_{50\%})V_{in,\max}T_s - \frac{L_{lk}I_{o,50\%}}{n}}{4L_m} + \frac{(1-D_{50\%})I_{o,50\%}}{2n} \quad (56)$$
$$+ \frac{V_o(1-D_{50\%})T_s + \frac{V_oL_{lk}I_{o,50\%}}{nV_{in,\max}(1-D_{50\%})}}{2nL_1} \approx 3.2A$$

$$i_{p1}(t_{14}) \approx -\frac{D_{50\%}(1-D_{50\%})V_{in,\max}T_s - \frac{L_{lk}I_{o,50\%}}{n}}{4L_m} - \frac{D_{50\%}I_{o,50\%}}{2n} \quad (57)$$
$$- \frac{V_oD_{50\%}T_s + \frac{V_oL_{lk}I_{o,50\%}}{nD_{50\%}V_{in,\max}}}{2nL_2} \approx -1.6A$$

Thus, the minimum resonant inductance to achieve ZVS of $S_1$-$S_4$ is obtained as:

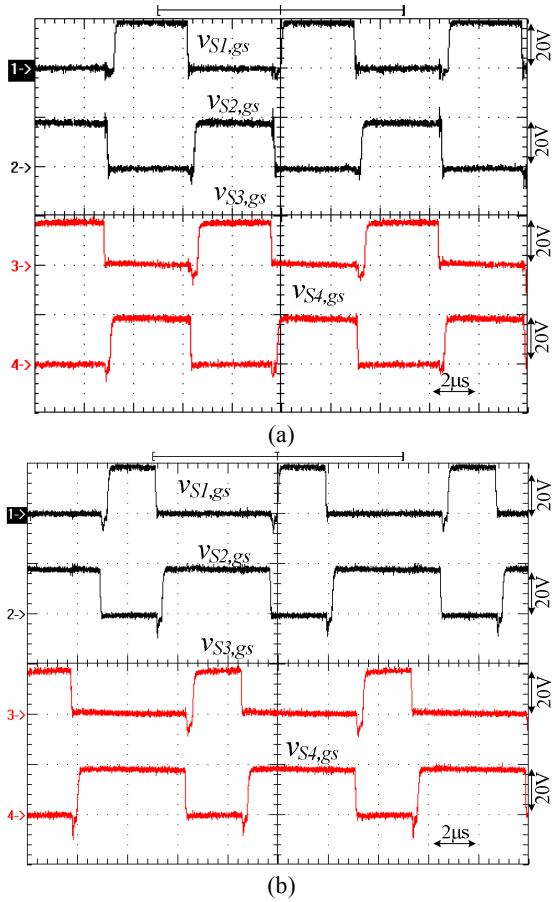


Fig. 4. Measured PWM signals of $S_1$~$S_4$ at (a) 100% load (b) 50% load.

$$L_{lk,ZVS,50\%} \geq \max\{\frac{D_{50\%}C_r V_{in,\max}^2}{2i_{p1}^2(t_2)}, \frac{(1-D_{50\%})C_r V_{in,\max}^2}{2i_{p1}^2(t_{14})}\} \quad (58)$$

$$= 15.6\mu H$$

From (44) and (58), the selected resonant inductor $L_{lk}$=16.3μH can meet ZVS condition of $S_1$-$S_4$ from 50% to 100% load conditions. The selected capacitance $C_1$ and $C_2$ is 0.44 $F$. The capacitance of output capacitor $C_o$ is 2200 $F$.

Experimental results based on a laboratory prototype rated at 960W (24V/40A) are provided to verify the effectiveness of the adopted converter. The circuit parameters of the adopted converter are obtained from the previous section. Fig. 4 gives the measured PWM signals of $S_1$~$S_4$ at 50% and 100% load conditions. The PWM signals of $S_1$ and $S_3$ are phase-shifted with half of switching cycle. The measured gate voltages and drain voltages of switches $S_1$ and $S_2$ in converter 1 at 50% and 100% load conditions are given in Fig. 5. Fig. 6 gives the measured results of the gate and drain voltages of $S_3$ and $S_4$ at 50% and 100% load conditions. From the measured results in Figs. 5 and 6, the drain voltages have been decreased to zero before switches $S_1$~$S_4$ are turned on. Thus, $S_1$~$S_4$ are all turned on at ZVS from 50% to 100% load. Fig. 7 shows the measured gate voltage $v_{S1,gs}$, switch currents $i_{S1}$ and $i_{S2}$, and the primary current $i_{p1}$ in converter 1 at full load.

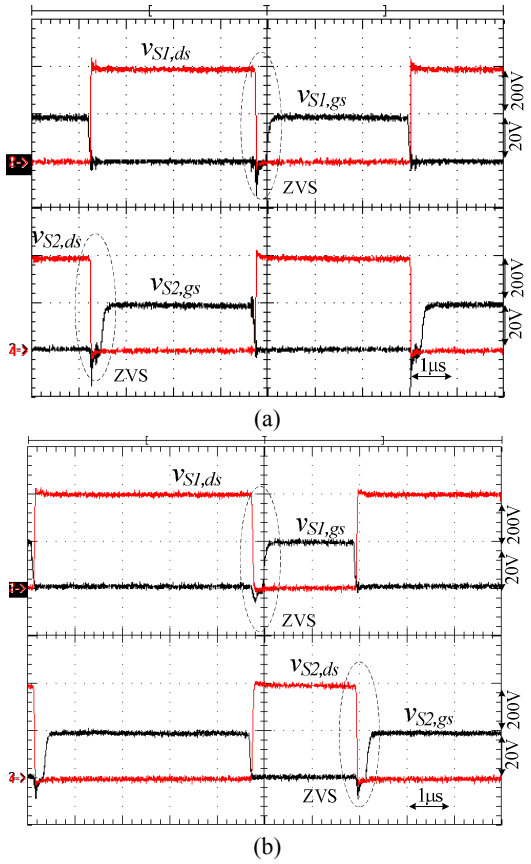


Fig. 5. Measured gate voltages and drain voltages of switches $S_1$ and $S_2$ at (a) 100% load (b) 50% load.

When switch $S_1$ is turned on, the primary current $i_{p1}$ equals the switch current $i_{S1}$. The primary current $i_{p1}$ increases. Power is transferred from input side to output load through transformer $T_1$. When $S_1$ is turned off, the primary current $i_{p1}$=-$i_{S2}$ and the primary current $i_{p1}$ decreases. In the same manner, the measured gate voltage $v_{S3,gs}$, switch currents $i_{S3}$ and $i_{S4}$ and primary current $i_{p2}$ in converter 2 at full load are shown in Fig. 8. Fig. 9 gives the measured waveforms of $v_{S1,gs}$, $i_{D1}$, $i_{D2}$, $i_{L1}$, $i_{L2}$, $i_{L1}$+$i_{L2}$, $i_{L3}$, $i_{L4}$ and $i_{L3}$+$i_{L4}$ at full load. The inductor currents $i_{L1}$ and $i_{L2}$ in converter 1 are partially cancelled each other. Therefore, the current ripple of the resultant output current, $i_{L1}$+$i_{L2}$, in converter 1 is reduced. In the same manner, the inductor currents $i_{L3}$ and $i_{L4}$ in converter 2 are also partially cancelled each other. From the measured results shown in Fig. 9, the output currents of two converter modules are almost balanced.

Fig. 10 gives the measured waveforms of gate voltage, the resultant inductor current, load current and output voltage at full load condition. In order to investigate the performance of the proposed converter, the circuit topology proposed in [19] (Fig. 11) is tested and compared with the proposed converter under the same circuit specifications and the same ZVS range (from 50% load to 100% load). Fig. 12 shows the measured circuit efficiencies of the proposed converter and the circuit topology in Fig. 11. The proposed circuit has a better circuit

efficiency because there are more circuit components in Fig. 11. The current stress of power switches in the primary side for both circuit topologies are the same based on the APWM scheme. Because the current doubler rectifier can achieve partially ripple current cancellation at output side, the output ripple current in the proposed converter can expected to be have than the ripple current in Fig. 11. The measured output ripple current of the proposed converter is about 4.5A and the output ripple current of the circuit topology in Fig. 11 is about 6.2A.

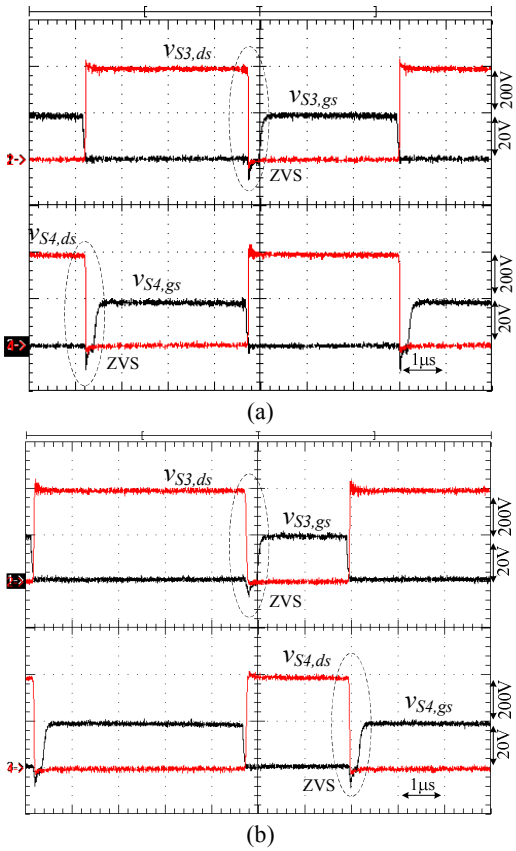


Fig. 6. Measured gate voltages and drain voltages of switches $S_3$ and $S_4$ at (a) 100% load (b) 50% load.

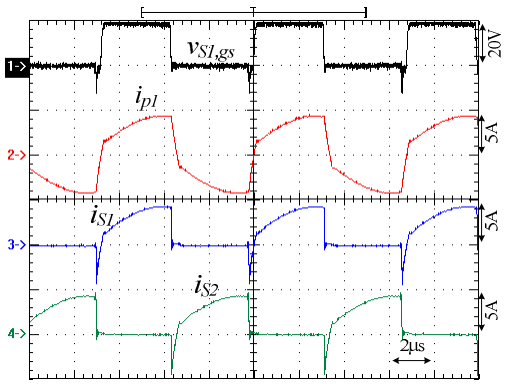


Fig. 7. Measured gate voltages and primary side currents in converter 1 at full load.

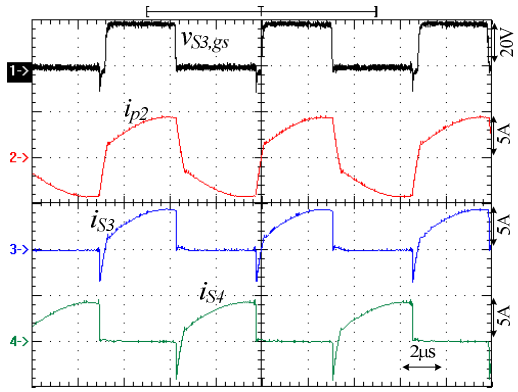


Fig. 8. Measured gate voltages and currents of converter 2 at full load.

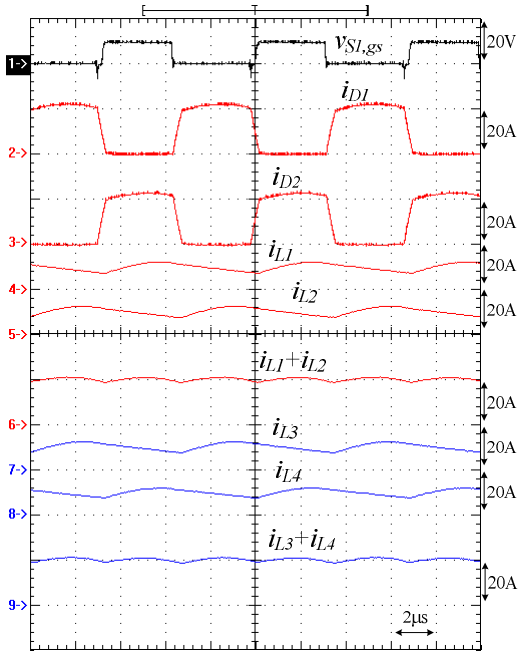


Fig. 9. Measured waveforms of $v_{S1,gs}$, $i_{D1}$, $i_{D2}$, $i_{L1}$, $i_{L2}$, $i_{L1}+i_{L2}$, $i_{L3}$, $i_{L4}$ and $i_{L3}+i_{L4}$ of the proposed converter at full load.

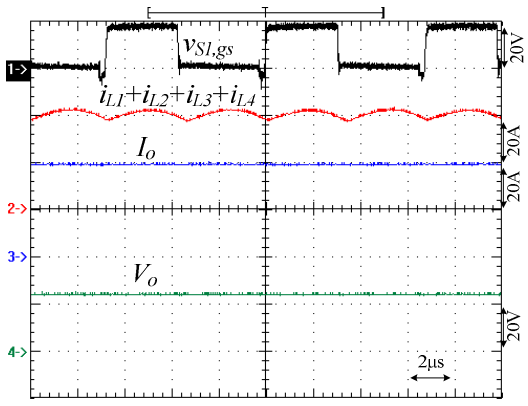


Fig. 10. Measured waveforms of the gate voltage, the resultant inductor current, load current and output voltage at full load.

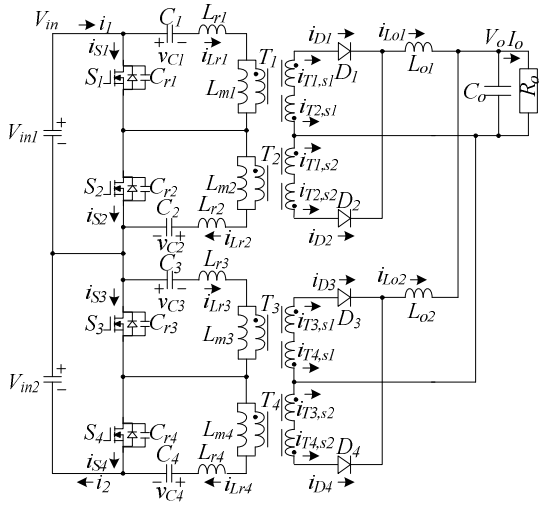


Fig. 11. Circuit topology in [19].

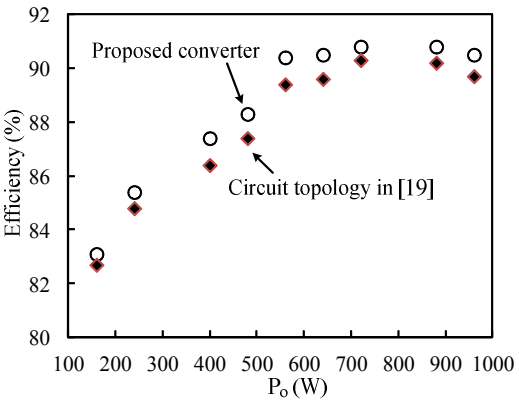


Fig. 12 Measured circuit efficiencies of the proposed converter and the circuit topology in [19] at different load conditions.

## VI. CONCLUSION

This paper presents an interleaved half-bridge converter to achieve 1) zero voltage switching of power switches, 2) the magnetizing flux reset with the asymmetrical PWM scheme, 3) the reduction of voltage stresses of MOSFETs using two series half-bridge converters, and 4) the ripple current reduction with the current doubler rectifier and the interleaved PWM scheme. Two half-bridge converters are connected in series at the primary side to reduce the voltage stresses on active switches and connected in parallel at the output side to reduce the current stresses on the rectifier diodes. Finally, the theoretical analysis and the effectiveness of the proposed converter are verified from the experiments based on a 960W laboratory prototype.

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