JPE 13-1-7

http://dx.doi.org/10.6113/JPE.2013.13.1.59

Multistage Inverters Control Using Surface Hysteresis Comparators

Menshawi K. Menshawi† and Saad Mekhilef*

†*Dept. of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia

Abstract

An alternative technique to control multilevel inverters with vector approximations has been presented. The innovative control method utilizes specially designed two-dimensional hysteresis comparators to simplify the implementation and improve the resultant waveform. The multistage inverter designed with maximum number of levels is operated in such a way to approximate the reference voltage vector by exploiting the large number of multilevel inverter vectors. A three-stage inverter with the main high voltage stage made of three phase, six-switch and singly-fed inverter is considered for application to the proposed design. The proposed control concept is to maintain a higher voltage stage state as long as it can lead to a target vector. High and medium voltage stages controllers are based on surface hysteresis comparators to hold the switching state or to perform the necessary change to achieve its reference voltage with minimal switching losses. The low voltage stage controller is designed to approximate the target reference voltage to the nearest inverter vector using the nearest integer rounding and adjustment comparators. Model simulation and prototype test results show that the proposed control technique clearly outperforms the previous control methods.

Key words: Hybrid, Hysteresis comparators, Multilevel inverters, SVM control, Voltage control

I. INTRODUCTION

Multilevel inverters (MLI) have seen considerable development and research interest compared with its early days when it was first introduced almost 4 decades ago. The class of inverters with output points of several voltage levels with respect to the negative side of its input supply [1], [2].

One of the most common multilevel inverter topologies is the cascaded H-bridge (CHB) topology. CHB as a basic form of the multistage inverter is composed of a number of full-bridge units supplied with equivalent and isolated DC sources (Vs). For each inverter branch, the outputs of the full bridge cells are connected in series to accumulate the branch voltage [5]. The k-cell inverter branch has a maximum, a minimum and steps voltages of kVs, -kVs and Vs, respectively. As a result it has (2k+1) voltage levels. As all of the cells have the same voltage steps, it is expected that the branch voltages, except for the extreme levels, can be achieved with multiple combinations of individual cells switching states. The asymmetrical CHB inverter has been introduced to increase the number of voltage levels with the same number of full bridge cells by supplying the cascaded cells with different DC voltages [4]. It has also been shown that with the cascaded cells voltages related by a ratio of 3 (i.e. Vs, 3Vs. 9Vs...), the number of uniformly spanned voltage levels is maximized since each voltage level has a unique switching state for individual cells which implies the elimination of redundant states [5].

The disadvantage associated with the CHB topology is mainly the need for an isolated DC source by each H-bridge cell which adds to overall complexity, maintenance, and cost. One way to ease this problem is to have the highest voltage stage, also referred to as the main stage, constructed with a topology that uses one DC supply for the three phase branches instead of the three full bridge cells. Constructing multistage inverters with a conventional 6-switch and a 3-level neutral point diode clamped (NPC) main stage has been reported in [6] and [7], respectively.

The main high voltage stage of hybrid multistage inverters withstands the largest portion of the total DC voltage rather than dividing the voltage equally between the switching devices as in basic multilevel inverters. This might be seen as giving up of one of the main features of multilevel inverters which is the ability to construct an inverter with a voltage rating that is a multiple of the switching devices ratings. However, the design of hybrid inverters relies on a fundamental feature of semiconductor switching devices which is a tradeoff between the device switching frequency

Manuscript received Aug. 17, 2011; revised Nov. 19, 2012
Recommended for publication by Associate Editor Se-Kyo Chung.
†CorrespondingAuthor:menshawik@yahoo.com
Tel:+60-03-79675205, University of Malaya
*Dept. of Electrical Engineering, University of Malaya, Malaysia

and the voltage ratings [8], [9]. Therefore, the main stage should be restricted to a low switching frequency, preferably the fundamental frequency, while a low voltage stage can be operated at the desired carrier frequency.

The high voltage stage maintains the low frequency operation, if it is confirmed that the PWM carrier frequency switching between the adjacent voltage levels, can be carried out without involving the high voltage stage. The capacity of changing the voltage between adjacent levels by controlling the low voltage stage by the modulation condition has been addressed and referred to in the literature [10]. The modulation condition imposes a restriction on the DC voltage ratio of the cascaded stages. Maximizing the number of levels by eliminating the state redundancy leads to a failure of the modulation condition, i.e. some redundancy is necessary to satisfy the modulation condition.

Most of the research presented in the literature with ratio-3 based multistage inverter sourcing used low frequency control methods to avoid the undesirable high frequency switching of the high voltage stage. Rather than attempting to produce the local time average of the reference voltage by PWM switching between the nearest higher and lower inverter voltage levels, the reference voltage is approximated to the nearest inverter voltage level [12], [13]. With the presence of a large number of voltage levels, this approximation is justified.

Voltage vector approximation control algorithms presented in [14] follow one of two possible approaches. The first approach has two stages. The first stage is to calculate the nearest inverter vector and the second is to determine the corresponding switching signals for the individual cascaded stages [14], [15]. As the number of levels is usually large, there will be a large number of equivalent switching states sharing the same voltage vector. This makes the second stage rather complicated, particularly if the designer aims to optimize the utilization of the equivalent states. The second approach is based on individual inverter cascaded stage calculations. This approach has been introduced for phase voltage level approximation [16]. It has been recently extended to the vector approximation of multistage inverters designed with a maximum number of levels [17]-[20]. The staged vector approximation has been found to be useful as a basis for the PWM control of inverters with state redundancy elimination without subjecting the high voltage stage to a high switching frequency [21]-[26]. In this paper the voltage vector approximation algorithm is designed according to the second approach.

The algorithm has been designed to hold the higher voltage stage switching state as long as this state can lead to the target vector in order to minimize the switching losses and to ensure the fundamental switching frequency for the high voltage stage. If the present switching state cannot lead to the target vector then the inverter changes it. The new switching state can lead to the target vector and should maintain minimal switching losses. In the work presented in [18], the determination of whether the present state should be maintained or changed and the determination of the next state are all carried out by calculations that depend on geometric description of various locations within the vector space. These calculations involve a lot of algebraic expressions, many trigonometric functions and some lookup tables which resulted in complicated calculations. To simplify the calculations, a 60°- displaced coordinate system is used to represent the inverter and the reference voltage vectors in [21]. In this representation, it has been shown that the comparison needed to determine if a given reference can be realized using a certain state is a very simple integer expression. This led to a considerable simplification and an elimination of the look-up tables, which in turn saves memory space and execution time.

Staged controller structure [18], [20] has been adopted in this paper. However, the control algorithm has been implemented using specially designed 2-D hysteresis comparators rather than algebraic-based equations. This approach aims to simplify the implementation and to overcome some of the bugs associated with the previous implementations. In the following section, the control concept is introduced followed by a brief description of previous implementations and their associated problems. Sections III, IV and V describe the controllers of the three inverter stages. Section VI presents the simulation and experimental results and Section VII concludes the paper.

II. VOLTAGE VECTOR APPROXIMATION CONTROL

The voltage vector control algorithm is explained thoroughly in this section and is suitable for any multistage inverter provided that the voltage steps of the cascaded stages are ratio-3 related. However, the 3-stage inverter shown in Fig. 1 has been used to describe and implement the designed control technique.

A. The Control Algorithm

The 18-levels of the multistage inverter shown in Fig. 1.are highlighted in Fig. 2, in which x, y and z denote the switching states of the high, medium and low voltage stages, respectively.

The voltage levels of one inverter branch output (A, B or C) with respect to an arbitrary reference point (Ref)are also described in Fig. 2. x is a binary number with x=0 and 1 representing the ON state of the lower and the upper switching devices in the main stage sub-inverter. With y (z) = 0, 1 and 2, the medium (low) full bridge cell is producing the negative, 0 and the positive of its DC side voltage, respectively.

The switching states of the inverter stage sare represented by voltage vectors. The voltage vector for a given switching state is obtained by applying Park's transformation equation in the following form:

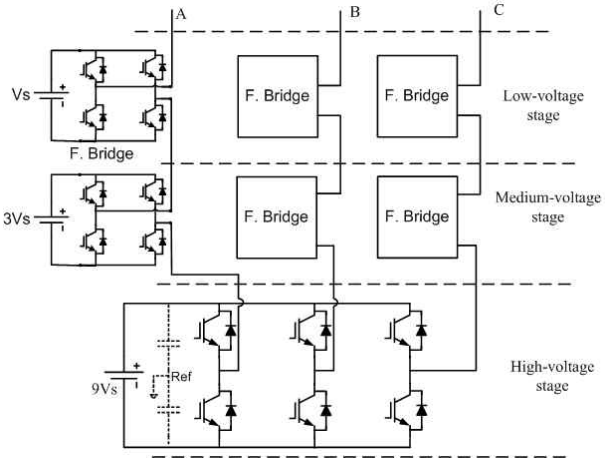

Fig. 1. The three-stage inverter with singly-fed main stage.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = V_S \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} 9x_A + 3y_A + z_A \\ 9x_B + 3y_B + z_B \\ 9x_C + 3y_C + z_C \end{bmatrix} \quad (1)$$

where V_d and V_q are the d- and q- components of the voltage vector and the subscripts (*A, B and C*) denote the phase. For all possible combinations of the switching variables, the resultant voltage vectors compose the inverter voltage vector diagram as given in Fig. 3. In this figure the voltage vector diagram has been drawn with three line thicknesses and colors to show that any inverter voltage vector can be represented as a sum of three vectors: corresponding to the high, medium and low voltage stages.

The controller target is to approximate a reference vector within the inverter voltage vector space to the nearest inverter vector with minimal switching losses. To minimize the switching losses, the controller should produce the nearest target vector with minimal switching giving priority in switching reduction to a higher voltage stage.

The inverter voltage vectors, (except for the outmost layer of Fig. 3), can be obtained by multiple switching combinations of the three stages, despite the absence of state redundancy, as indicated in Fig. 2. The example vector denoted by V1 in Fig. 3 shows that it is possible to represent a given inverter vector as a sum of different high, medium and low voltage vectors. Greater flexibility is added due to the fact that the zero vectors for all of the stages and the non-zero vectors of the normal Vs and 3Vs for the low and medium voltage stages correspond to multiple switching states.

The shaded hexagonal area around the high voltage stage vector shown in Fig. 3, is corresponding to the state x=100 and denoted by "Domain of state x_{ABC}=100." This area is formed by all of the medium and low voltage stages vectors superimposed on the high voltage stage vector corresponding to the state x_{ABC}=100. If and only if a reference vector is

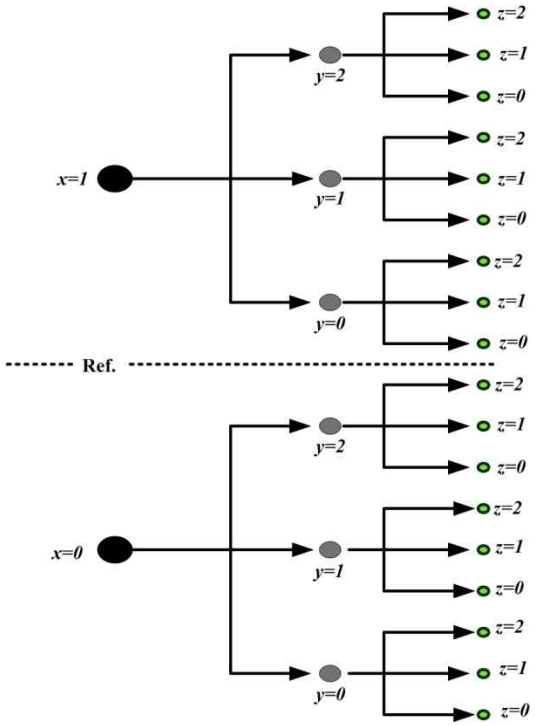

Fig. 2.The 18 voltage levels of the inverter.

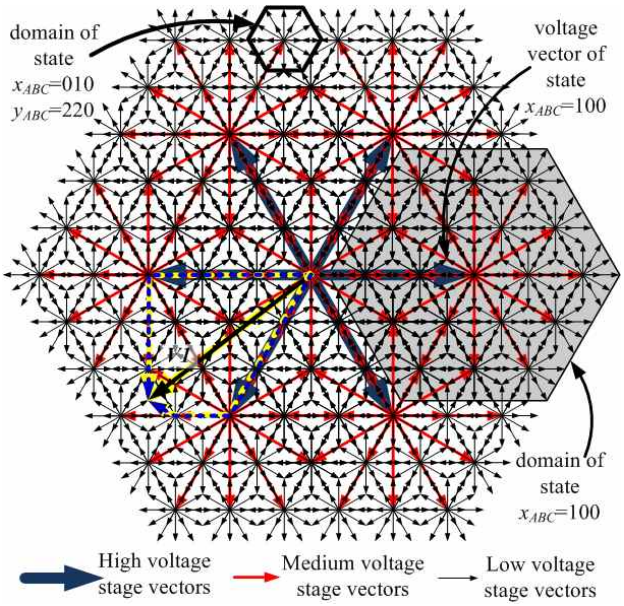

Fig. 3. The inverter vector diagram.

located within the domain of a high voltage state, this vector can be approximated by adding the appropriate medium and low voltage vectors to that high voltage vector.

The next switching state for the three stages consecutively, is determined by the cascaded controller, as shown in Fig. 4. The high voltage stage controller compares the reference vector to the present high voltage stage domain. If the reference vector is located in the present high state domain, then the high voltage stage preserves its switching state for the

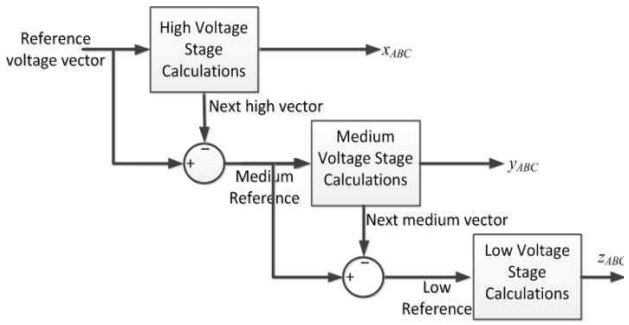

Fig. 4. The controller structure.

next sampling interval. Otherwise, it should be changed to one that has the reference voltage in its domain. The overlap between the high voltage states domains in some regions of the vector space is indicated in Fig. 5. If the reference voltage is located in the domain overlap, there will be more than one option in the next state selection. The state obtained with minimum switching action, is selected in order to reduce switching losses.

The high voltage stage controller produces the next high voltage state, as the present state or as a new state; the corresponding voltage vector is then subtracted from the reference voltage vector. The resultant vector is denoted in Fig. 4 by the medium reference and represents the balance of the reference vector that needs to be supplemented by the medium and low voltage stages. To control the medium voltage stage, the state domain has been defined in a way that is similar to the high voltage stage domain, as indicated in Fig. 3. The medium voltage stage control concept is similar to the concept of the high voltage stage control, i.e. the switching state is maintained if the reference vector is located in its domain, else the nearest state that has the reference voltage in its domain is selected.

Once the medium voltage stage controller produces the next medium voltage state, the corresponding vector is then subtracted from the medium reference and the result, denoted in Fig. 4 by the low reference, represents the part of the reference vector that needs to be approximated, or realized, by the low voltage stage.

B. Geometric-Based Calculations

The voltage vector approximation described in [18], has been implemented by representing the voltage vectors with their orthogonal (d-q) components. The geometry of the voltage vector space has been represented by linear equations that must use floating-point coefficients.

The various regions resulting from domains overlapping have been subjected to a series of comparisons to determine the reference vector location in terms of various domains after specifying the reference sector. For low voltage stage control an interpolating polynomial has been composed to approximate the points around each low stage voltage vector

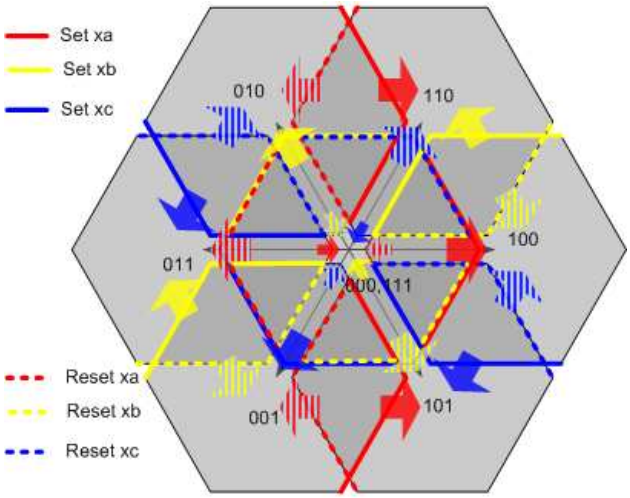

Fig. 5. The function of the 2-dimensional hysteresis comparators to control the high voltage stage.

to the nearest vector. This implementation, despite achieving the design goals in terms of controller function suffers from some drawbacks that can be summarized as :

1. Large memory space, due to the long routines and the use of lookup tables.
2. Costly floating point controller or slow processing with a fixed point controller, due to the floating point coefficients and the frequent use of trigonometric functions.
3. Difficulty in extending the design for over modulation region.

C. 60°-Displaced Coordinates Control

The representation of the normalized reference voltage and the inverter vectors in the 60°-displaced coordinates system *G-H*, has significantly simplified the control procedure as shown for a three-level inverter in Fig. 6. The voltage vectors of the three inverter stages have simple integer coordinates in the *G-H* system. In addition, the relationship between the switching variables and the *G-H* coordinated is a simple integer expression. As for any stage, the inverter vector *G-H* coordinates are given by:

$$\begin{bmatrix} V_G \\ V_H \end{bmatrix} = V_{DC} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} \sigma_A \\ \sigma_B \\ \sigma_C \end{bmatrix} \quad (2)$$

Where, V_{DC} is the stage DC voltage and σ_{ABC} is the stage switching variable, i.e. *x, y* and *z* for the high medium and low voltage stages, respectively. This simplifies the voltage vector approximation procedure to mostly integer calculations [20]. Due to the simple comparison expressions, the comparisons to determine the location of the reference vector in terms of various domains have been abandoned and the valid next

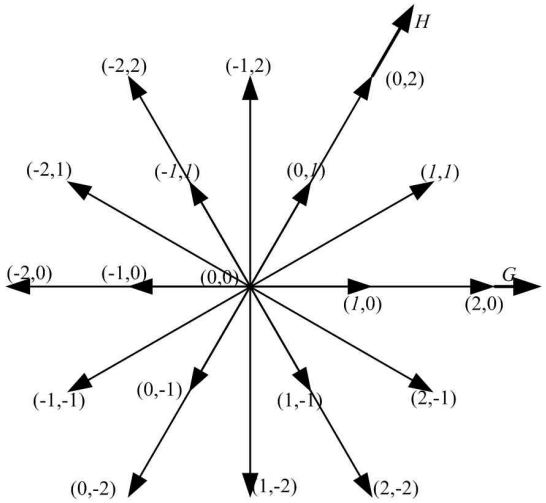

Fig. 6. The GH coordinate system and the normalized coordinates of a three level inverter.

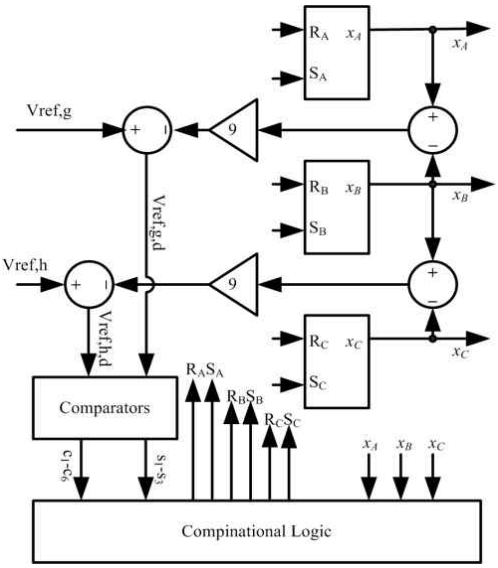

Fig. 7. The high voltage stage logic controller.

states have been determined by repeating the comparison of the reference vector coordinates with all of the vectors domains. The low voltage stage has been controlled by rounding the normalized low reference *G-H* coordinates and reversing the relationship expressed in (2) to determine z_{ABC}. The memory and the execution time have been considerably reduced with this implementation but some errors are generated due to the fact that *G-H* rounding does not always lead to the best vector approximation.

D. The New Control Hypothesis

The alternative control algorithm presented in this paper, is described for the hybrid three stage inverter shown in Fig. 1 and is based on the cascaded controller structure shown in Fig. 4. However, the control technique has been modified to create a simpler implementation and a more robust control.

The new control method described in this section can be explained for high and medium voltage stages as the sub-inverter holds its switching state for as long as it can lead to a reference approximation. This function can be viewed as a hysteresis comparator that deals with inputs represented as vectors in two-dimensional space. The characteristics of the various stages comparators are determined by the stage domain and the form of the adjacent states domains overlap.

III. Main Voltage Stage Controller

In this new control technique, the three binary digits x_{ABC} representing the main (high) voltage switching state, are held by three RS flip-flops, as indicated in Fig. 7. The vector corresponding to the present high state is always subtracted from the reference vector. If the difference ($V_{ref,g,d}$, $V_{ref,h,d}$) is located within the hexagonal hysteresis band, or the state domain, then the switching state is preserved by keeping the RS signals inactive. When the difference vector exceeds the hysteresis region, it will be detected by one of the comparators designed to determine the excess segment, as defined in Fig. 8. The comparators signals trigger the Set or Reset signals according to the relationship between the binary expressions of the present and the new state, indicated in Fig. 5. The triggering signals have been composed as a set of combinational logic expressions that have the following form:

$$RS_{ABC} = F(x_{ABC}, c_{1-6}, s_{1-3}) \tag{3}$$

where c_{1-6} and s_{1-3} are the comparators used to determine the domain borders crossing, as indicated in Fig. 8.

IV. Control Of The Medium Voltage Stage

Two flip-flops hold the switching state of each medium voltage stage full bridge cell. Each flip-flop controls one of the full bridge arms. The flip-flops outputs are denoted by y_{A1},y_{A0} for phase A, y_{B1},y_{B0} for phase B, and y_{C1},y_{C0} for phase C. The definition of the code used to represent the three switching states is explained in Table I. The advantage of this coding is that 2-bit values can be directly used to drive the switching devices without further decoding. In addition, this coding shows that the full bridge characteristic has two zero-producing switching states. Therefore it provides a simple method to balance the devices currents.

TABLE I
The 2-bit Coding Used to Represent the Medium Voltage State in the Proposed Controller

Base-3 State (y)	Bridge output voltage	y_1	y_0
0	−3Vs	0	1
1	0	0/1	0/1 (=y_1)
2	3Vs	1	0

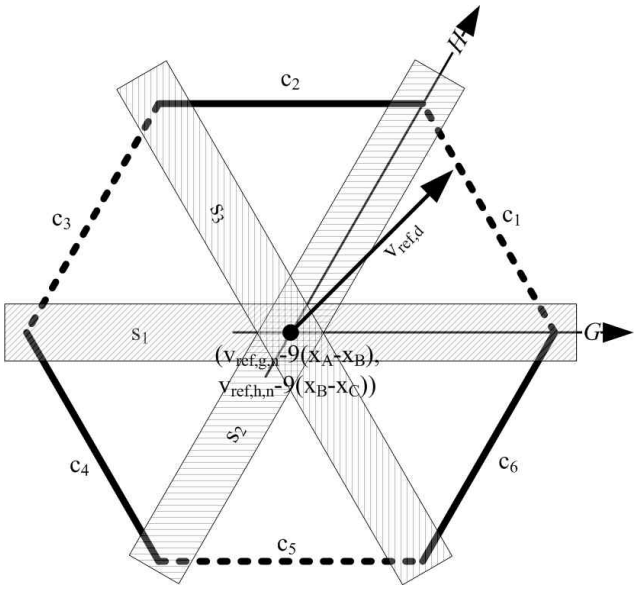

Fig. 8. The comparators to determine the high voltage state transition.

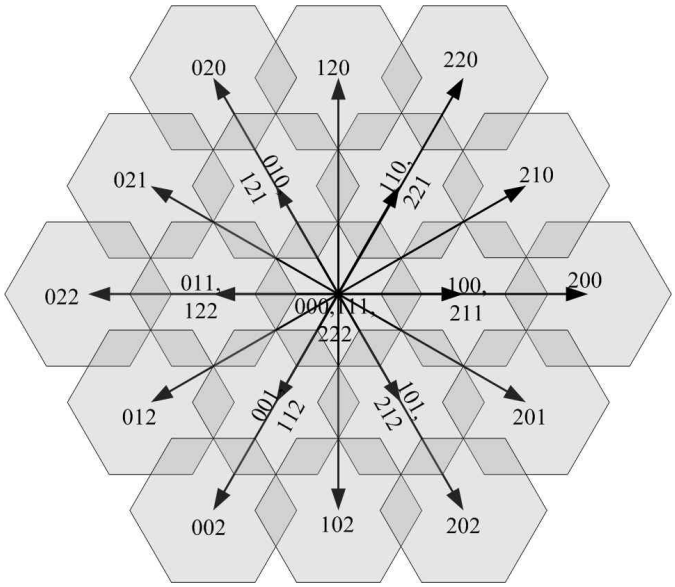

Fig. 9. Medium voltage domains within one high state domain.

The controller of the medium voltage stage design is based on the distribution of the medium stage domains in a high state domain, as shown in Fig. 9. This distribution resulted in domain overlapping and the border of one domain with an overlapping one is always formed by two halves of the hexagon's adjacent sides. Therefore, the six detectors to indicate the exceeding reference have been characterized, as shown in Fig. 10. In this figure, the action of the medium stage controller has been indicated as an increment or decrement in one of three differences defined as follows:

$$\begin{aligned} \Delta y_A &= \lfloor (y_A - y_B) \quad (y_A - y_C) \rfloor \\ \Delta y_B &= \lceil (y_B - y_A) \quad (y_B - y_C) \rceil \\ \Delta y_C &= \lfloor (y_C - y_A) \quad (y_C - y_B) \rceil \end{aligned} \tag{4}$$

The implementation of the increment or decrement command indicated in Fig. 10 by the medium voltage stage controller is explained in Table II by examples. The controller takes one of three actions according to their priority. First, changing the corresponding switching variable in the desired direction. Second, changing the other two switching variable in the opposite direction. Third, if both changes are not possible, then the present switching state is maintained. In other words, the increment or decrement of the state is subjected to saturation as the switching variable y[0, 2]. If the desired change cannot be realized due to this limit, it implies that the reference is beyond the medium vector space and the medium stage is preserved. The core of the medium stage controller is implemented using a 2-bit saturable up/down counter with a special counting sequence.

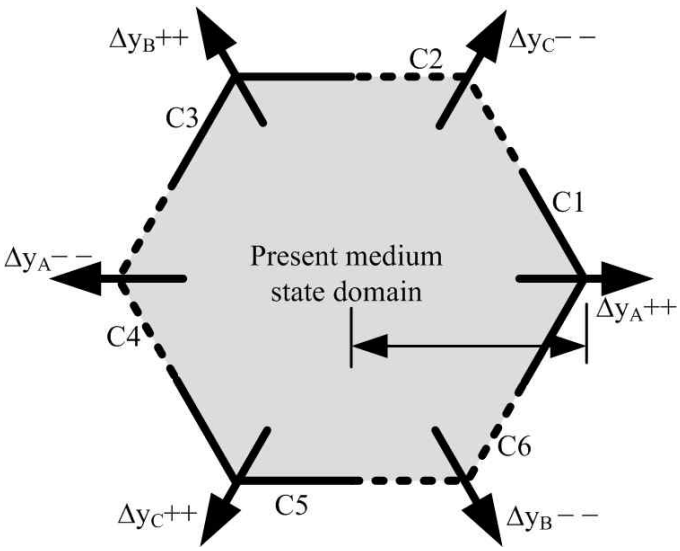

Fig. 10. Medium voltage stage domain excess comparators and control actions.

TABLE II

THE CONTROLLER ACTION TO CHANGE THE MEDIUM STAGE DUE TO EXCEEDING THE PRESENTS DOMAIN.

Desired Change	Priority	Action	Example	
			Initial state	Next state
Increment Δy_A++	1	Increase y_A	120	121
	2	Decrease y_B ,y_C	212	201
		No change	210	210
Decrement Δy_B−−	1	Decrease y_B	120	110
	2	Increase y_A ,y_C	001	102
		No change	102	102

V. CONTROL OF THE LOW VOLTAGE STAGE

The low voltage stage controller approximates the low voltage reference vector, indicated in Fig. 4, to the nearest inverter vector. The low reference is represented in the G-H coordinates. The method presented in [20] uses the relationship between the G-H representation of the reference and the switching state to approximate the reference vector in the following two steps:

1. The rounding of reference coordinates: the normalized reference coordinates have been rounded to the nearest integers, and the integer coordinates have been taken as the coordinates of the nearest target vector.
2. The target vector switching states have been determined using the following inverse form of equation (2):

$$\begin{bmatrix} z_A' \\ z_B' \\ z_C' \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{bmatrix}\begin{bmatrix} vg_{ref,L} \\ vh_{ref,L} \end{bmatrix} \quad (5)$$

The specific solution(s) are obtained by imposing the three-level switching variables limits z[0, 2].

The above steps create an error in the inverter's output signal if the reference vector is not located in the mutual area between the parallelogram and the hexagon. The error occurs when leading the approximation of the parallelogram area around each vector to its center point. However, the best approximation for each reference vector is given by a 90° rotated hexagon around each vector, as indicated in Fig. 11. Therefore, the G-H coordinates of the target vector have to be corrected before determining the switching states according to step 2. The correction procedure is explained by Fig. 12. In this figure, the low stage reference coordinates are denoted by (g_{ref}) and (h_{ref}) and their nearest integer rounding are G_r and H_r respectively. Over the four shaded triangular regions shaded Fig. 12, the G-H coordinates of the best approximation or nearest inverter vector (G_b, H_b) have to be calculated after considering the following conditions representing the operation of the five comparators:

$$C_1 : g_{ref} > G_r - H_r + h_{ref} \quad (6)$$

$$C_2 : g_{ref} > 1 + G_r + 2H_r - 2h_{ref} \quad (7)$$

$$C_3 : g_{ref} > \frac{1}{2} + G_r + \frac{H_r}{2} - \frac{h_{ref}}{2} \quad (8)$$

$$C_4 : g_{ref} < G_r + 2H_r - 1 - 2h_{ref} \quad (9)$$

$$C_5 : g_{ref} < G_r + \frac{H_r}{2} - \frac{1}{2} - \frac{h_{ref}}{2} \quad (10)$$

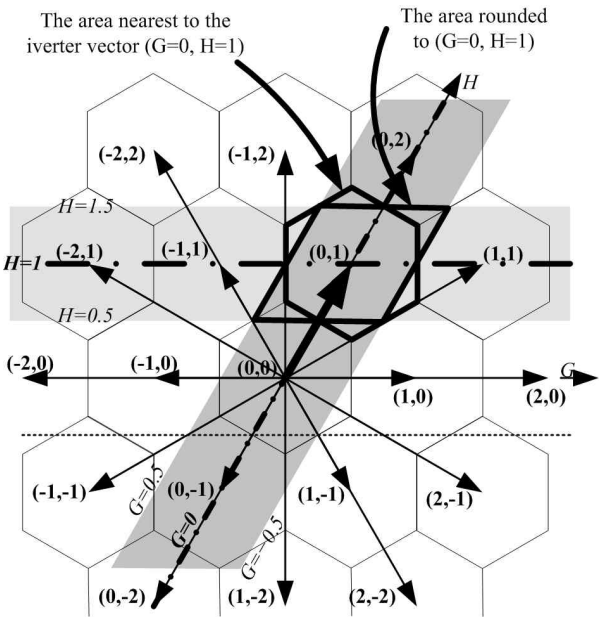

Fig. 11. The GH coordinates rounding approximation of the reference vector verses the best reference vector approximation.

Modifying the rounded coordinates (G_r, H_r) achieves the best vector approximation. The correction process is described according to following equations:

$$G_b = G_r + (C_1.AND.C_3) - (\overline{C_1}.AND.C_5) \quad (11)$$

$$H_b = H_r + (\overline{C_1}.AND.C_2) - (C_1.AND.C_4) \quad (12)$$

In (11) and (12), the logic expression in the brackets results in a numerical value of 0 or 1 which modifies the values of G_b and H_b, according to Fig. 12.

VI. RESULTS

A simulation model and an experimental prototype have been constructed, tested and compared to verify the proposed control method and its advantages over previous methods. In this implementation a step voltage (Vs) of 12V is considered to supply the low and medium voltage stages by using 12V lead-acid batteries. One unit is used to supply each low voltage stage bridge and three series-connected units are used for the medium voltage stage. A regulated DC supply is used to supply 108V for the high voltage stage. A passive three-phase Y-connected RL load is connected to the output side.

The MATLAB-SIMULINK® environment has been used to carry out the simulation process, while the real-time algorithm driving the experimental prototype has been implemented by using an eZdspF28335 controller board which is based on a TMS320F28335 DSP 32-bit fixed-point processor. The processing frequency is 150 MIPS.

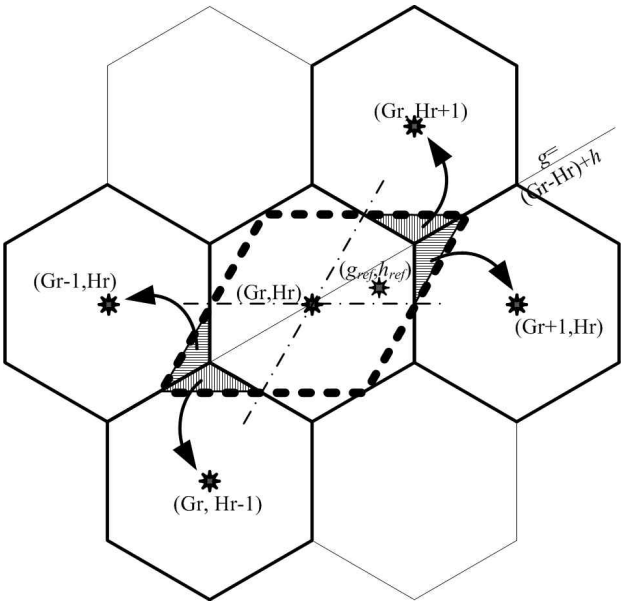

Fig. 12. The correction of G-H rounding parallelogram to the best approximation hexagon.

A. The Control Concept

The simulated result of different inverter stages output voltage waveforms are shown in Fig. 13, 14 and 15. The measured line voltage waveforms at different stages are shown in Fig. 16, 17 and 18. The load phase voltage with two reference voltage amplitude values are shown in Fig. 19. The results analysis further shows that the inverter maintains a harmonic distortion below 4% for a reference amplitude of 60% or higher. In Fig. 13, the simulated voltage waveforms are compared to the voltages obtained using the method presented in [20] which applies the GH-based control and uses mathematical calculations to determine the switching signals. It can be seen that the distortion which occurred in the previous method due to the difference between the nearest inverter vector and the GH coordinates rounding has been removed and less distorted waveforms are obtained.

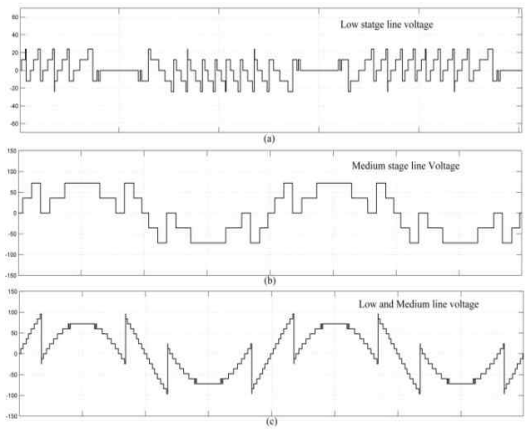

Fig. 13. Simulated: (a) Low stage voltage, (b) Medium stage voltage, (c) Low and medium stages line voltage.

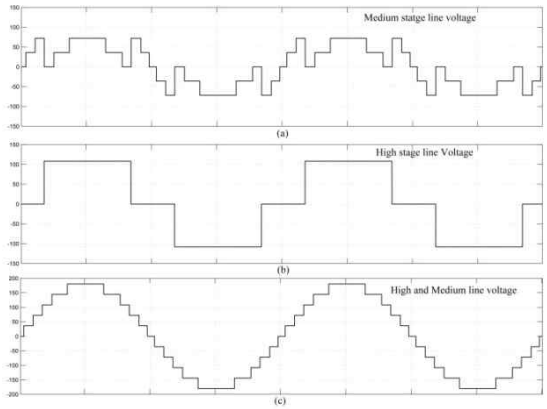

Fig. 14. Simulated: (a) Medium stage voltage, (b) High stage voltage, (c) Medium and high stages line voltage.

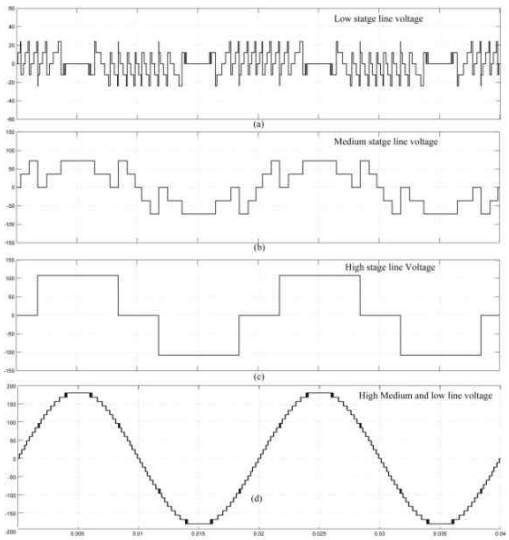

Fig. 15. Simulated: (a) Low stage voltage, (b) Medium stage voltage, (c) High stages voltage, (d) Three stages line voltage.

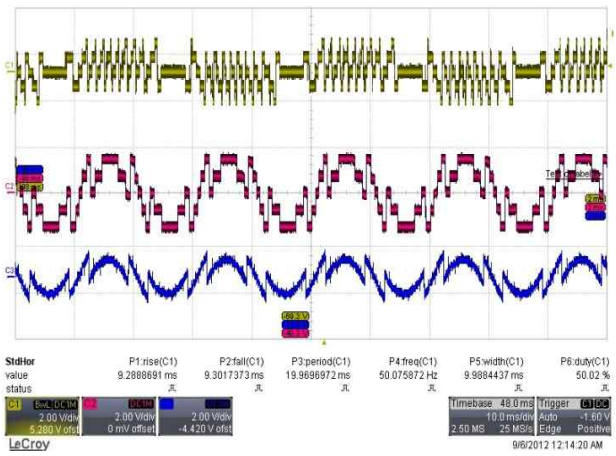

Fig. 16. Experimental: from top, low stage voltage, medium stage voltage, and low & medium stages line voltage.

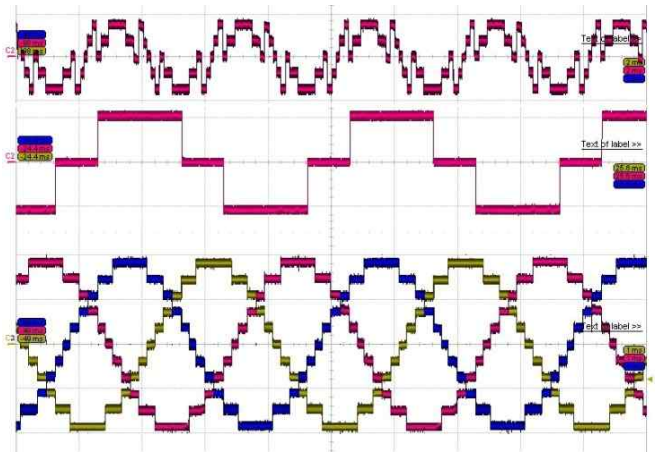

Fig. 17. Experimental: from top, medium stage voltage, high stage voltage, and high and medium stages 3 phase LL voltages.

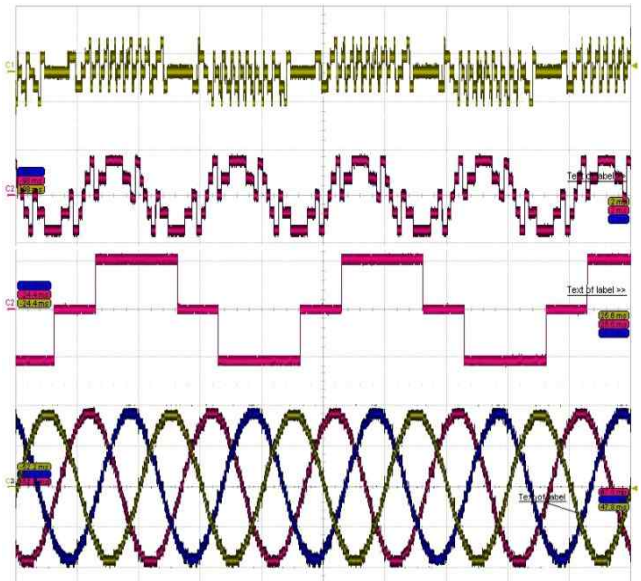

Fig. 18. Experimental: from top, low stage voltage ,medium stage voltage, high stage voltage, three stages 3 phase LL voltages.

In Fig. 20, the total harmonic distortion of the load phase voltages are compared for the two control methods. It can be observed that the proposed method provides a1-5% reduction in the harmonic distortion using the same sampling rate and with similar operating conditions.

B. The switching frequency

Fig. 21 shows the high voltage switching states and the corresponding triggering signals for the three flip-flops. This figure verifies that the high voltage stage is operating at the fundamental frequency. It also shows that the combinational logic is operating according to the described design.

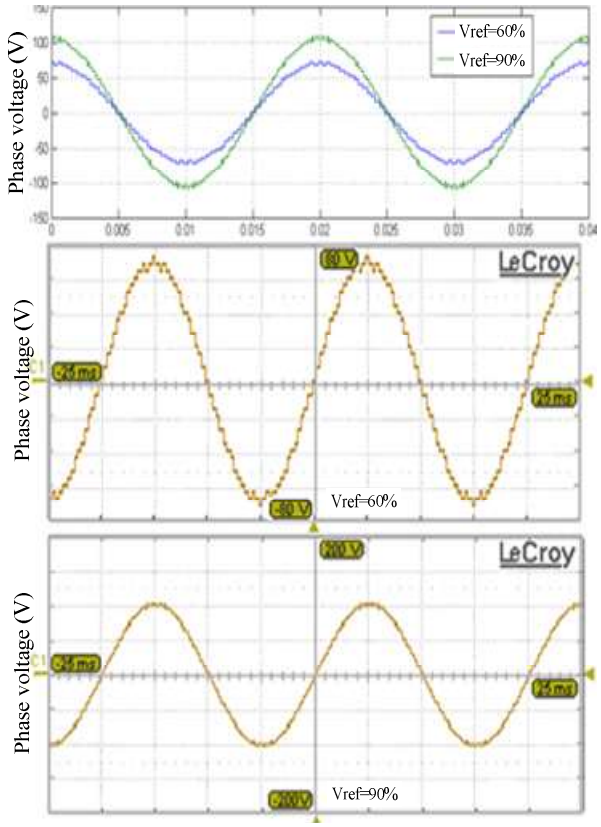

Fig. 19. Load phase voltage from the top simulated waveforms with reference voltages of 90% and 60%, measured waveform with 60% reference voltage and 90% reference voltage.

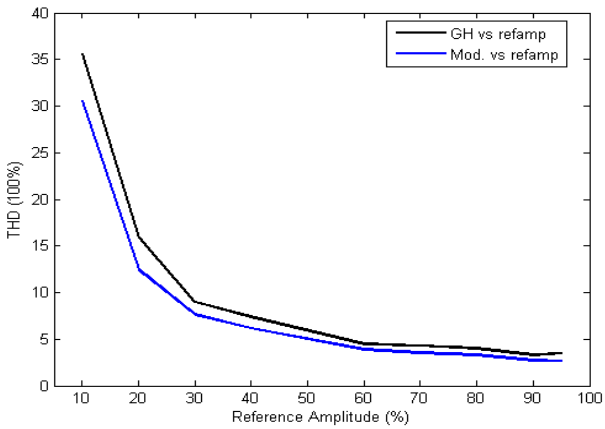

Fig. 20. Measured total harmonic distortion (%) against the reference amplitude for the two control methods.

VII. CONCLUSION

This paper has presented the concept of an alternative voltage vector approximation control technique and has shown its effectiveness. The proposed control method is suitable for state redundancy free multistage inverters designed with a maximized number of levels.

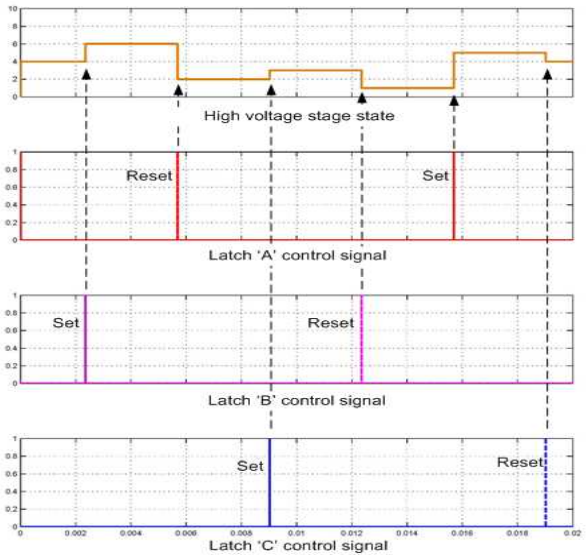

Fig. 21. High voltage stage switching state over one output cycle and the corresponding flip-flops driving signals.

The control strategy has been designed and applied to each individual stage starting with high voltage stage going through the medium stage and finally ending with the low voltage stage. The individual stage controllers have been implemented using state-of-art logic expressions. The switching states are saved in the most basic flip-flops while the control function is implemented with novel comparators and combinational logic.

The presented control technique has distinctive advantages such as simplicity and execution speed, as well as the ability to contain the exact inverter characteristics which lead to harmonics distortion reduction and inherent balanced current distribution. The results have verified the effectiveness of the proposed control method.

ACKNOWLEDGMENT

This work was supported by the HIR-MOHE Project. The grant was funded under the Project reference number, (UM.C/HIR/MOHE/ENG/ D000017- 16001).

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Menshawi K. Menshawi received his B.S. from the University of Benghazi (formally known as the University of Garyounis), Benghazi, Libya, in 1990 and his M.S. in Engineering from the University Technology Malaysia (UTM), Skudai, Malaysia, in 1995. He is currently working on his Ph.D. in Power Electronics in the Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia. Since 1996, has been employed as a full time Lecturer at the Multimedia University, Cyberjaya, Malaysia and the University of Benghazi, Benghazi, Libya.

Saad Mekhilef (M'01, SM'12) received his B.S. in Electrical Engineering from the University of Setif, Setif, Algeria, in 1995, and his M.S. in Engineering Science and Ph.D. from the University of Malaya, Kuala Lumpur, Malaysia, in 1998 and 2003, respectively. He is currently a Professor and the Head of the Department of Electrical Engineering, University of Malaya. He is the author and coauthor of more than 150 publications in international journals and proceedings. He is actively involved in industrial consultancy for major corporations in the power electronics field. His current research interests include power conversion techniques, control of power converters, renewable energy, and energy efficiency.