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Transformerless Three-Level DC-DC Buck Converter with a High Step-Down Conversion Ratio

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Abstract

For high power high step-down dc-dc conversion applications, conventional three-level dc-dc converters are subject to extreme duty cycles or increased volume and cost due to the use of transformers. In this paper, a transformerless three-level dc-dc buck converter with a high step-down conversion ratio is proposed. The converter comprises two asymmetrical half bridges, which are of the neutral point clamped structures. Therefore, the output pulse voltage of the converter can be obtained in terms of the voltage difference between the two half bridges. In order to realize harmonious switching of the converter, a modulation strategy with capacitor voltages self balance is presented. According to the deduced output dc voltage function, transformerless operation without extreme duty cycles can be implemented. Experimental results from a 1kW prototype verify the validity of the proposed converter. It is suitable for ship electric power distribution systems.

Key words: DC-DC buck converter, High step-down conversion, Non-extreme duty cycles, Three-level

I. INTRODUCTION

With the development of power electronics techniques, there has been a growing interest in multilevel converters for high power and high voltage applications [1]-[6]. Basically, there are three types of multilevel inverters for dc-ac applications: diode-clamped inverters, flying-capacitor inverters, and cascaded H-bridge inverters [7]-[9]. In 1981, the neutral point clamped (NPC) three-level inverter was proposed by A. Nabae [10]. During the following years, this concept for a multilevel conversion technique has been applied to dc-dc applications. J. R. Pinheiro proposed a three-level ZVS (zero-voltage switching) PWM converter with the NPC structure in 1992 [11]. Then a new concept in high voltage dc-dc conversion was established.

Later, the basic family of three-level dc-dc converters was discussed in [12]. From the conventional half bridge converter, the half bridge three-level converter was derived with the so-called three-level switch cells. Then, six nonisolated three-level converters based on the buck, boost, buck-boost, Cuk, SEPIC, and Zeta topologies were obtained, as well as five isolated three-level converters based on the forward, flyback, push-pull, half bridge, and full bridge topologies.

As for three-level step-down converters, the non-isolated three-level dc-dc buck converter is the basic topology to implement the conversion from a high voltage input to a low voltage output. Unfortunately, this basic topology may also be subject to extreme duty cycles when a high step-down conversion is required [13]. Therefore, the output rectifier diode in the basic three-level buck converter must sustain a short pulse width current with a high amplitude, which leads to severe reverse recovery and high electromagnetic interference (EMI) problems [14], [15]. Moreover, extreme duty cycles are not desirable, because no space is left for the controller to compensate changes in load or line.

Another solution to achieve a high step-down voltage gain is to increase the turns ratio of the transformer. Such an isolated three-level dc-dc converter can deal with the input high voltage and avoid the extreme duty cycles due to the presence of a transformer. Although the circulating current can be minimized effectively, the transformer design is critical to the success of the converter performance [16]. However, several applications require high step-down non-isolated dc-dc converters, for example, the buck type PFC (power factor correction) [17], the buck converter used

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in ship electric power distribution systems [16], and so on. A transformerless dc-dc converter without extreme duty cycles is necessary to decrease the volume and to increase efficiency.

In this paper, a transformerless three-level dc-dc buck converter with a high step-down conversion ratio is proposed for ship electric power distribution systems. This converter can convert a high DC bus voltage to a low DC voltage for important DC loads of high power. In Section II, the circuit of the converter is presented and the operation principles are described in detail. Then a modulation strategy which can satisfy the operation of the converter is proposed with the capacitor voltages self balance, and the function of the output dc voltage V_o is deduced. Moreover, the principle of transformerless operation without extreme duty cycles is also clarified when the step-down conversion ratio is rather high. In Section III, a 1 kW hardware prototype for the resistive load has been designed and tested to verify the validity of the converter operation and performance.

II. Operational Principles of the Proposed Converter

A. Topology and Operation of the Converter

Fig. 1 shows the proposed transformerless three-level dc-dc buck converter with a high step-down conversion ratio. V_{in} is the input dc voltage. The input filtering capacitors C_1 and C_2 are series connected and serve as a capacitive voltage divider to split the input dc voltage V_{in} into two equal voltages V_{C1} and V_{C2}. Then there are three voltage levels: zero, $V_{in}/2$ and V_{in}. The converter comprises the left half bridge (LHB) "a" and the right half bridge (RHB) "b". The LHB "a" consists of the power switches Q_1 and Q_2, and the diodes D_1 and D_2, whose blocking voltages are all clamped at $V_{in}/2$ via the clamped diodes D_{c1} and D_{c2}. The RHB "b" consists of the power switches Q_3 and Q_4, and the diodes D_3 and D_4, whose blocking voltages are also clamped at $V_{in}/2$ via the clamped diodes D_{c3} and D_{c4}. Finally, the output dc voltage V_o is obtained by the filters (L_f and C_f) between the output ports "a" and "b" of the converter for supplying power to the load R, as shown in Fig. 1.

Both the LHB and the RHB can operate, and the switching state concept is introduced in this paper, namely S_x="0" or "1" denotes that Q_x is off or on (x=1~4). As for the LHB, the three-level output voltage V_{ag} is V_{in} when the switching state is S_1S_2=11. If the switching state is S_1S_2=01, V_{ag} is $V_{in}/2$, which is the voltage across C_2, and the voltage stress of Q_1 is $V_{in}/2$ (the voltage across C_1). V_{ag} becomes zero when the switching state is S_1S_2=00. Meanwhile, D_1 and D_2 are freewheeling, and Q_1 and Q_2 are both clamped by the voltages ($V_{in}/2$) across C_1 and C_2, respectively.

As for the RHB, the three-level output voltage V_{bg} is zero when the switching state is S_3S_4=11. When the switching state is S_3S_4=10, V_{bg} is $V_{in}/2$ (the voltage across C_2), and the blocking voltage of Q_4 is the voltage across C_2. V_{bg} is V_{in} when the switching state is S_3S_4=00, and D_3 and D_4 are freewheeling. At the same time, the blocking voltages of Q_3 and Q_4 are across C_1 and C_2, respectively. As a result, the output pulse voltage (V_{ab}) between the output ports "a" and "b" of the proposed converter can be obtained as follows:

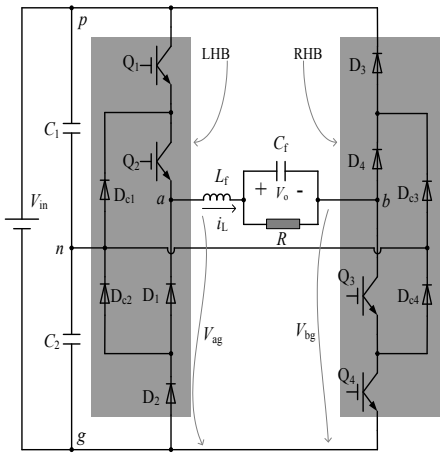


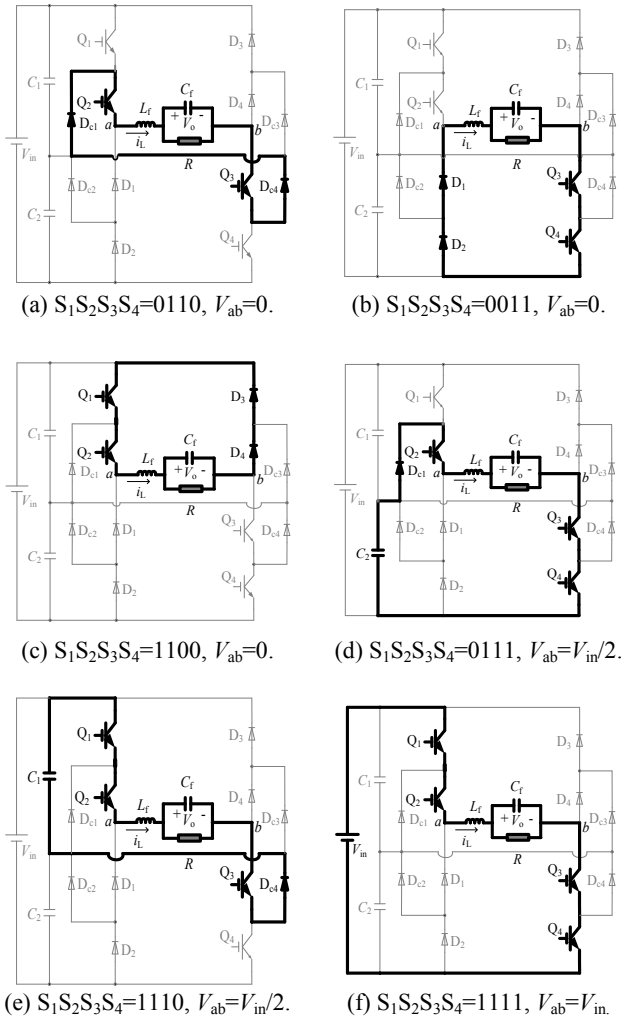
Fig. 1. Circuit diagram of the proposed converter.

$$V_{ab} = V_{ag} - V_{bg} \tag{1}$$

According to (1), the available pulse voltage V_{ab} can be generated in the case of harmonious switching of the four power switches Q_1~Q_4, namely the switching state "$S_1S_2S_3S_4$." Assuming that the inductor current i_L is continuous, there are six operation modes of the proposed converter, as shown in Fig. 2. When the switching state is $S_1S_2S_3S_4$=0110, i_L flows through: Q_2, the filter and the load (L_f, C_f and R), Q_3, and the clamped diodes D_{c4} and D_{c1}, as shown in Fig. 2(a). Then the pulse voltage V_{ab} is zero. When i_L flows through the filter and load, the power switches Q_3 and Q_4, and diodes D_2 and D_1, as shown in Fig. 2(b), V_{ab} is also zero. Under similar condition to Fig. 2(b), as shown in Fig. 2(c), i_L flows through the filter and load, diodes D_4 and D_1, and the power switches Q_1 and Q_2. Consequently, V_{ab} is zero all the same. The operation modes in Figs. 2(a)~(c) are all in freewheeling states due to the continuous inductor current i_L. Namely, the converter has three redundant states for V_{ab}=0.

When the switching state is $S_1S_2S_3S_4$=0111, as shown in Fig. 2(d), the inductor current i_L flows through the filter and the load, the power switches Q_3 and Q_4, the filtering bottom capacitor C_2, the clamped diode D_{c1} and the power switch Q_2. Then V_{ab}=$V_{in}/2$ can be obtained due to the voltage across the bottom divided capacitor C_2. As a result, C_2 is discharged to supply the energy for the load R.

In addition, V_{ab}=$V_{in}/2$ can be generated when the switching state is $S_1S_2S_3S_4$=1110, as shown in Fig. 2(e). Then, the inductor current i_L flows through the filter and the load, the power switch Q_3, the clamped diode D_{c1}, the filtering upper capacitor C_1, and the power switches Q_1 and Q_2. Therefore, the upper divided capacitor C_1 is also discharged, taking the



(a) $S_1S_2S_3S_4$=0110, V_{ab}=0. (b) $S_1S_2S_3S_4$=0011, V_{ab}=0.

(c) $S_1S_2S_3S_4$=1100, V_{ab}=0. (d) $S_1S_2S_3S_4$=0111, V_{ab}=V_{in}/2.

(e) $S_1S_2S_3S_4$=1110, V_{ab}=V_{in}/2. (f) $S_1S_2S_3S_4$=1111, V_{ab}=V_{in}.

Fig. 2. Topological operation modes of the proposed converter.

power supply for the load R. Namely, there is the another redundant switching state for V_{ab}=V_{in}/2.

The last operation mode, as shown in Fig. 2(f), can be realized when the switching state is $S_1S_2S_3S_4$=1111. Then, the inductor current i_L flows through the filter and the load, the RHB power switches Q_3 and Q_4, the input dc power supply V_{in}, and the LHB power switches Q_1 and Q_2. Hence the pulse voltage V_{ab} becomes V_{in}.

B. Modulation Strategy with Capacitor Voltages Self Balance

In order to carry out harmonious switching of the converter's power switches and to achieve a high voltage gain, the key modulation strategy is proposed in Fig. 3, based on the principle of the proposed converter. The modulation indices of the left and right half bridges are m_a and m_b, respectively, as shown in Fig. 3(a). Both carrier waves (carrier1 and carrier2) are π phase-shifted. In every carrier period (T), the modulation law is designed as follows:

$$\begin{cases} m_b > V_{carrier1}, S_1 = 0 \\ m_a > V_{carrier2}, S_2 = 1 \\ m_a > V_{carrier1}, S_3 = 1 \\ m_b > V_{carrier2}, S_4 = 0 \end{cases} \quad (2)$$

where $V_{carrier1}$ and $V_{carrier2}$ are the instantaneous values of carrier1 and carrier2, respectively.

By virtue of (2), the gate signals of the four power switches S_1~S_4 (as well as the switching states) are shown in Figs. 3(b)~(e) and (h). Then, the output three-level voltages are generated by each half bridge, as shown in Figs. 3(f) and (g). Taking advantage of (1), the pulse voltage V_{ab} can be shown in Fig. 3(h). There are five switching states ($S_1S_2S_3S_4$) in the first half period (0~T/2) due to redundant switching states. In order these switching states are: 0110-1110-1100-1110-0110 (as shown in Fig. 3(h)). Then, the two voltage pulses of V_{ab} (V_{in}/2) can be obtained between the output ports "a" and "b" just when the switching state is "1110," as shown in Fig. 3(h). This results in the discharging of the upper divided capacitor C_1 for the load, as shown in Fig. 3(j). Similarly, in the second half period (T/2~T), the corresponding five switching states are in order: 0110-0111-0011-0111-0110. Then, the other two voltage pulses of V_{ab} (V_{in}/2) are obtained due to the switching state "0111," as shown in Fig. 3(h). As a result, the load is supplied by the bottom divided capacitor C_2, and C_2 is discharged, as shown in Fig. 3(k).

It is worth noting that there is only one switching change between the adjacent switching states, as depicted in Fig. 3(h). Consequently, the requirement of minimal switching losses can be met freely. According to the analysis of the topological operation modes, when V_{ab}=V_{in}/2, both C_1 and C_2 are charged and discharged in turn in every carrier period, as shown in Figs. 3(j) and (k). The modulation waves m_a and m_b and the average inductor current I_L can all be considered constant in every carrier period. In addition, the carriers are symmetrical, so the discharging/charging time of C_1 and C_2 can be equal, namely t_{1_3}=t_{2_4}, as shown in Figs. 3(c) and (d). Therefore, the voltages (V_{C1} and V_{C2}) across C_1 and C_2 can be self balanced in each carrier period. Furthermore, the equivalent frequency of V_{ab} is double the switching frequency, as shown in Figs. 3(a) and (h).

Assuming that the inductor current i_L is continuous, the energy W_{st} is stored by L_f when V_{ab} is V_{in}/2. This leads to i_L increasing linearly, as shown in Fig. 3(i). The energy W_{tr} is transferred when V_{ab} is 0, and it results in i_L decreasing linearly, as shown in Fig. 3(i). In every carrier period, W_{st} and W_{tr} can be described as follows:

$$\begin{cases} W_{st} = (V_{in}/2 - V_o) \times I_L \times 2 \times (t_{on1} - t_{off3}) \\ W_{tr} = V_o \times I_L \times [T - 2 \times (t_{on1} - t_{off3})] \\ W_{st} = W_{tr} \end{cases} \quad (3)$$

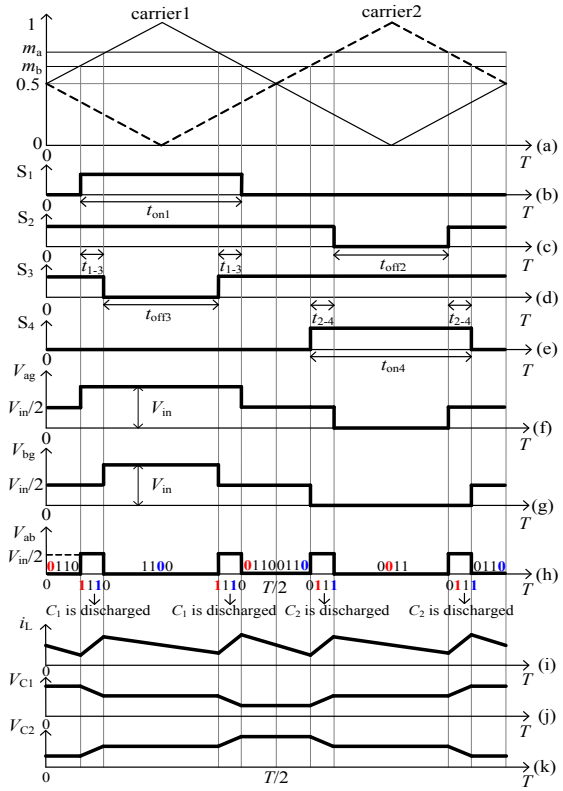


Fig. 3. Modulation strategy with capacitor voltages self balance.

where V_o is the output dc voltage after the L_f C_f filter, t_{on1} is the gate-on time of the power switch Q_1, and t_{off3} is the gate-off time of the power switch Q_3, as shown in Fig. 3. From Figs. 3(a)~(e), the corresponding duty cycles d_1~d_4 of the four power switches Q_1~Q_4 are described as:

$$\begin{cases} d_1 = d_4 = \dfrac{t_{on1}}{T} = 1 - m_b \\ d_3 = d_2 = \dfrac{T - t_{off3}}{T} = m_a \end{cases} \tag{4}$$

By combining (3) and (4), V_o can be written as:

$$V_o = V_{in} \times (m_a - m_b) \tag{5}$$

Namely, $V_o = V_{in} \times (d_1 + d_2 - 1)$ can be obtained and the limited conditions are $0 \le m_b < m_a \le 1$ and $m_a + m_b > 1$.

C. Transformerless Operation without Extreme Duty Cycles

For conventional three-level dc-dc buck converters without transformers, a high step-down conversion may always be achieved by means of extreme duty cycles. For example, when the voltage gain is higher, ***10*** (V_{in}/V_o), the conventional duty cycle may be ***0.1***, which is far from **0.5**. Fortunately, the duty cycles of the proposed transformerless scheme may be ***0.6*** and ***0.5*** by setting m_a=0.6 and m_b=0.5, by virtue of (4) and (5).

In fact, the essence of transformerless operation without extreme duty cycles is that the output pulse voltage V_{ab} is obtained from the three-level voltage difference between V_{ag} and V_{bg}, by means of Figs. 3(f)~(h). The short pulse width is up to the switching time intervals t_{1_3} and t_{2_4}, as shown in Figs. 3(d) and (e), which can be described as:

$$\begin{cases} t_{1\_3} = \dfrac{t_{on1} - t_{off3}}{2} \\ t_{2\_4} = \dfrac{t_{on4} - t_{off2}}{2} \end{cases} \tag{6}$$

and t_{1_3}=t_{2_4} can be confirmed due to the symmetrical geometry relationships in Fig. 3. According to (4)~(6), an identical voltage gain has infinite solution sets for m_a and m_b. As a result, with a higher step-down conversion ratio, optimum duty cycles can be chosen for the transformerless operation of the proposed converter, instead of the extreme ones. The simple selection method for m_a and m_b is to first set m_b as a constant, for example, 0.55 in this paper, according to the tradeoff between the duty cycles (d_1 and d_4) which are near 0.5, and the fluctuating amplitude of the inductor current. Then m_a can be obtained by means of the output (m_a-m_b) of the current PI controller.

D. Filter Design of the Converter

The filter of the proposed converter is important in terms of its operation performance, and it includes the filtering inductor L_f, and the filtering capacitor C_f. Therefore, the minimum values of L_f and C_f can be obtained according to the required maximum inductor current ripple ΔI_{L_max} and the output voltage ripple ΔV_{o_max}, respectively. According to (3) and Fig. 3, when V_{ab} is zero the energy stored in L_f is transferred, which leads to the filtering inductor current falling. As a result, the longer the falling time, the larger the inductor current ripple becomes.

In this paper, the longer falling time t_f is t_{off2} or t_{off3}, as shown in Figs.3 (c) and (d). Then t_f can be obtained as:

$$t_f = (1 - d_2) \cdot T \tag{7}$$

where T is the carrier period. During t_f, the voltage of L_f is written as:

$$u_L = 0 - V_o = -(d_1 + d_2 - 1) \cdot V_{in} \tag{8}$$

In addition, the inductor current ripple ΔI_L can be described as:

$$\Delta I_L = \frac{-u_L}{L_f} \cdot t_f \tag{9}$$

By substituting (7) and (8) into (9), the inductor current ripple ΔI_L can be written as:

$$\Delta I_L = \frac{(d_1 + d_2 - 1) \cdot (1 - d_2) \cdot T \cdot V_{in}}{L_f} \tag{10}$$

When d_1 is set as 0.5, d_2 is calculated as 0.75, and ΔI_{L_max} can be obtained as:

$$\Delta I_{\text{L\_max}} = \frac{V_{\text{in}} \cdot T}{16 L_{\text{f}}} \tag{11}$$

Therefore, the minimum value of L_{f} is limited by means of the required maximum inductor current ripple $\Delta I_{\text{L\_max}}$:

$$L_{\text{f\_min}} = \frac{V_{\text{in}} \cdot T}{16 \Delta I_{\text{L\_max}}} \tag{12}$$

In addition, the output voltage ripple ΔV_{o} can be described as:

$$\Delta V_{\text{o}} = \frac{1}{C_{\text{f}}} \times \frac{\Delta I_{\text{L}}}{2} \times \frac{T}{8} = \frac{\Delta I_{\text{L}} \cdot T}{16 C_{\text{f}}} \tag{13}$$

Hence the minimum value of C_{f} is described according to the inductor current ripple ΔI_{L} and the required output voltage ripple $\Delta V_{\text{o\_max}}$:

$$C_{\text{f\_min}} = \frac{\Delta I_{\text{L}} \cdot T}{16 \Delta V_{\text{o\_max}}} \tag{14}$$

As a result, the filter design of the converter can be completed theoretically by means of (12) and (14).

III. Experimental Results

The proposed converter with the voltage and current double-loop control scheme, in which PI controllers are adopted has been experimentally verified. The 1kW hardware prototype has been set up in the lab, as shown in Fig. 4. The experimental parameters and components are listed in Tab. 1.

Fig. 5 shows the pulse voltage V_{ab} (the amplitude of the pulse voltage is half the input dc voltage), the inductor current i_{L}, and the output dc voltage V_{o}, which is a constant 68V output, and a small ripple is achieved within ±2%. Fig. 6 shows the waveforms of voltages across the power switches Q_1 and Q_2, in which the blocking voltages are also the ones across the divided capacitors C_1 and C_2. Therefore, the voltages of C_1 and C_2 are self balanced, and both of the duty cycles are around 0.45 and 0.686, instead of 0.136 (68/500). Both of these values are closer to 0.5. Such non-extreme duty cycles are necessary for the converter when the switching frequency is increased to minimize the filter. The output three-level voltages of the half bridges V_{ag}, and V_{bg} are shown in Fig. 7. They are in agreement with the theoretical analysis in Figs. 3(f) and (g).

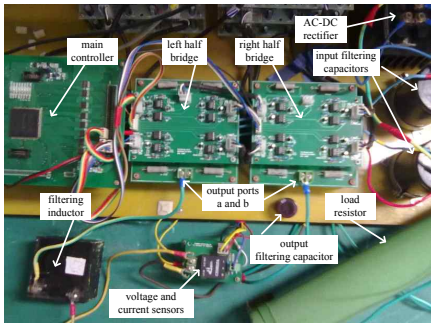


Fig. 4. 1kW hardware prototype.

TABLE I
EXPERIMENTAL PARAMETERS AND COMPONENTS

parameters and components	values (units)
rated power P_{n}	1 kW
input dc voltage V_{in}	500~640 V
reference voltage V_{ref}	68 V
input filtering capacitors C_1=C_2	2200 μF
output filtering capacitor C_{f}	160 μF
inductor L_{f}	317 μH
switching frequency f_{c}	10 kHz and 11.36kHz
load resistor R_{L}	3.8~50 Ω
power switches Q_1~Q_4	FGA30N60 (600V, 30A)
diodes D_1~D_4 and D_{c1}~D_{c4}	MUR3060 (600V, 30A)
K_{pv} of voltage PI controller	10.2
K_{iv} of voltage PI controller	1012
K_{pc} of current PI controller	0.021
K_{ic} of current PI controller	11.23

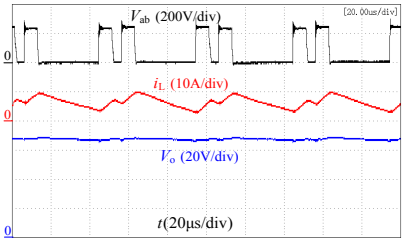


Fig. 5. Experimental waveforms of V_{ab} (upper), i_{L} (middle), and V_{o} (bottom), when V_{in}=500V and f_{c}=10kHz.

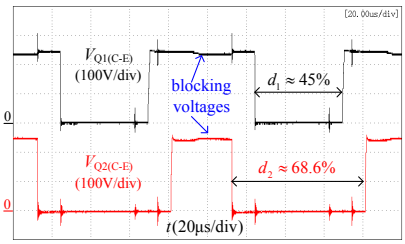


Fig. 6. Experimental waveforms of voltages across Q_1 (upper) and Q_2 (bottom), when V_{in}=500V and f_{c}=10kHz.

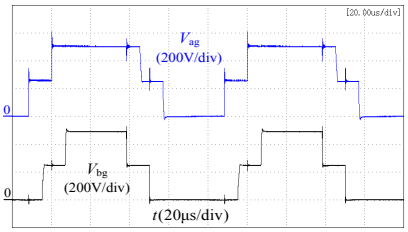


Fig. 7. Experimental waveforms of the output three-level voltages of V_{ag} (upper), and V_{bg} (bottom), when V_{in}=500V and f_{c}=10kHz.

Fig. 8 shows the pulse voltage V_{ab} (the amplitude of the pulse voltage is still half the input dc voltage), the inductor current i_{L}, and the output dc voltage V_{o} when V_{in} is changed to 640V. V_{o} is still controlled at a constant 68V output for the wide-input voltage range from 500V to 640V, and a small ripple is still achieved within ±2%.

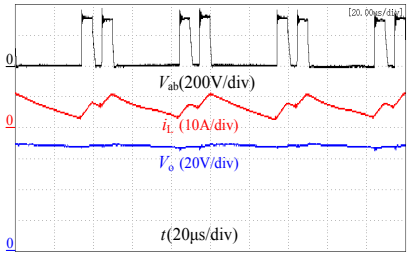


Fig. 8. Experimental waveforms of V_{ab} (upper), i_L (middle), and V_o (bottom), when V_{in}=640V and f_c=10kHz.

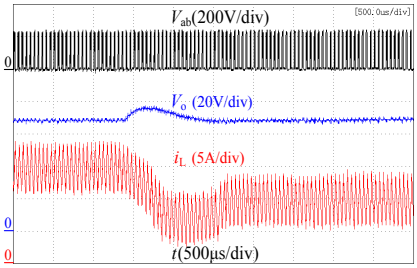


Fig. 9. Experimental waveforms of V_{ab} (upper), V_o (middle), and i_L (bottom), at the step load change from 4.6 Ω to 7 Ω, when V_{in}=500V and f_c=10kHz.

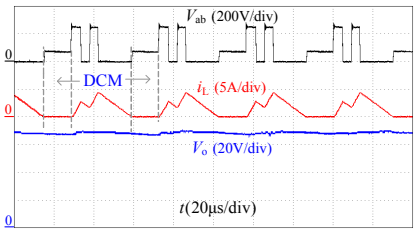


Fig. 10. DCM experimental waveforms of V_{ab} (upper), i_L (middle), and V_o (bottom), when V_{in}=500V and f_c=11.36kHz.

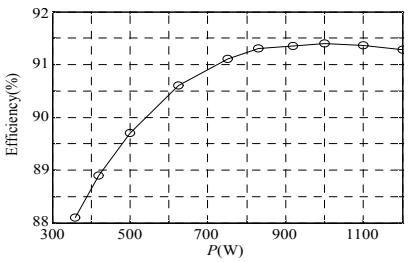


Fig. 11. Efficiency of the prototype versus output power, V_{in}=500V, and V_o=68V.

The output voltages and current under step load changes are shown in Fig. 9. When the load resistor is 4.6 Ω, the output dc voltage V_o is around 68V, and the inductor current i_L fluctuates from 11A to 19A. At the moment of the step load change (from 4.6 Ω to 7 Ω), V_o goes through the transient response, and it is still controlled at around 68V after about 1ms, due to the voltage controller. At the same time, the inductor current i_L goes down accordingly, and then it fluctuates from 6A to 14A in the steady state of the conversion system. The transient response time can be reduced further by the improved controller, if the overshoot of the output dc voltage V_o and the input capacitor voltages transient balance can be considered as well.

In order to verify the usability of the proposed converter for a light load, the discontinuous conduction mode (DCM) experimental waveforms with another increased switching frequency f_c=11.36kHz are shown in Fig. 10. The light load resistor is 45 Ω. Then the energy stored in the inductor is not enough to supply the load. At this point i_L becomes zero, namely it is in DCM. During DCM, the load is supplied by C_f merely, and V_{ab} is the voltage V_o across C_f, as shown in Fig. 10. However, it is shown that V_o can still be controlled at around the reference voltage 68V.

When the high input dc voltage V_{in} is 500V, and the low output dc voltage V_o is controlled at 68V, the efficiency of the experimental prototype is measured with the output power as illustrated in Fig. 11. The maximum efficiency is approximately 91.4% under a full load. Although a lower blocking voltages across the power switches and diodes can reduce the switching losses, the soft-switching mode will improve the efficiency of the proposed converter more than the present hard-switching mode.

IV. Conclusions

A transformerless three-level dc-dc buck converter with a high step-down conversion ratio is proposed. Such a converter can operate over a wide input voltage range for high voltage applications with fewer low-voltage-rated power components. It can also avoid extreme duty cycles without a transformer. The voltages across the two series capacitors are self balanced with the proposed modulation strategy, the blocking voltages of the IGBTs are half the input dc voltage, and the equivalent frequency of the output pulse voltage is double the switching frequency. From the experimental results, it can be seen that such a dc-dc converter displays good performance and hence is suitable for high power converters operating from a high-input dc voltage to a low-output dc voltage. It would be especially useful for ship electric power distribution systems.

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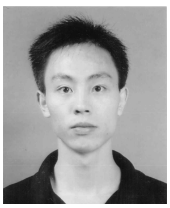

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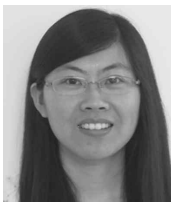

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