JPE 13-2-8

http://dx.doi.org/10.6113/JPE.2013.13.2.243

Neutral-Point Voltage Balancing Method for Three-Level Inverter Systems with a Time-Offset Estimation Scheme

Ui-Min Choi* and Kyo-Beum Lee†

*†Dept. of Electrical and Computer Eng., Ajou University, Suwon, Korea

Abstract

This paper presents a neutral-point voltage balancing method for three-level inverter systems using a time-offset estimation scheme. The neutral-point voltage is balanced by adding a time-offset to the turn-on time of the switches. If an inaccurate time-offset is added, the neutral-point deviation still remains. An accurate time-offset is obtained through the proposed time-offset estimation scheme. This method is implemented without additional hardware, complex calculations, or analysis. The effectiveness of the proposed method is verified by experiments.

Key words: Multilevel, Neutral-point voltage balancing, NPC inverter

I. INTRODUCTION

Multilevel inverters have been widely applied in high-power applications. Among multilevel inverters, the NPC inverter has the most widely used topology because of its advantages. The NPC inverter improves the output voltage and current waveforms and can reduce the size of the filters. In addition, the voltage stress across the switch is reduced to half that of a conventional two-level inverter. Fig. 1 shows a simplified diagram of an NPC inverter system. It is composed of twelve IGBTs and six diodes. The DC-link capacitor is split into two sources to generate different voltage levels. To maximize the performance of the NPC inverter, the voltages of the two capacitors connected in series must have the same values. If these values are different, this may lead to premature failure of the switching devices, and the THD of the output current increases because the low-order harmonics become dominant; and second- and fourth-order harmonics appear in the output voltage [1]-[7].

DC-link voltage deviation can occur owing to the following causes [8]: unbalanced DC capacitors due to manufacturing tolerances, inconsistency in the switching device characteristics, and unbalanced three-phase operation. Since directly solving these problems is difficult, many strategies have been introduced to balance the neutral-point voltage. SVM strategies have been introduced in many papers [9], [10]. In [9], the space vector diagram is divided into 12 sectors and four alternative switching sequences are defined for each of the 12 sectors. Then, the proper switching sequence is chosen based on an analysis of the predicted voltage unbalance. In [10], the independent phase duty ratios are calculated through complex calculations. Using these, the control signals of the 12 switches are generated. These methods are complex to use and can increase the switching frequency and output THD.

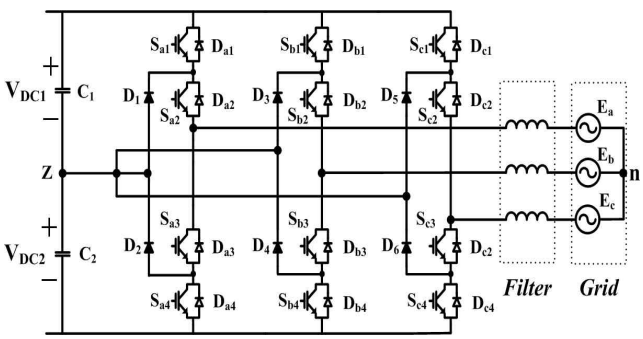

Fig. 1. Simplified diagram of an NPC inverter system.

Manuscript received Jul. 31, 2012; revised Feb. 1, 2013
Recommended for publication by Associate Editor Yong-Sug Suh.
†Corresponding Author: kyl@ajou.ac.kr
Tel: +82-31-219-2376, Fax: +82-31-212-9531, Ajou University
*Dept. of Electrical and Computer Eng., Ajou University, Korea

TABLE I

SWITCHING STATES OF SMALL VOLTAGE VECTORS

Type	Switching state
N-type	[ONN], [OON], [NON], [NOO], [NNO], [ONO]
P-type	[POO], [PPO], [OPO], [OPP], [OOP], [POP]

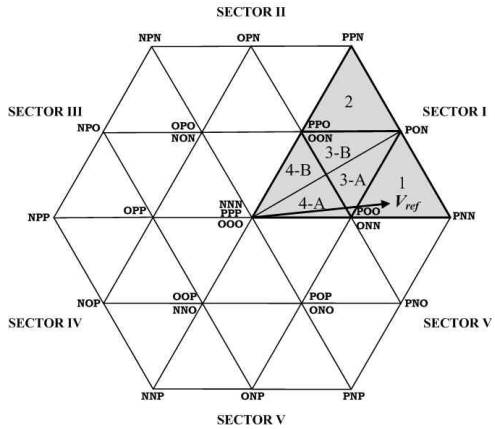

Fig. 2. Space vector diagram of three-level inverter.

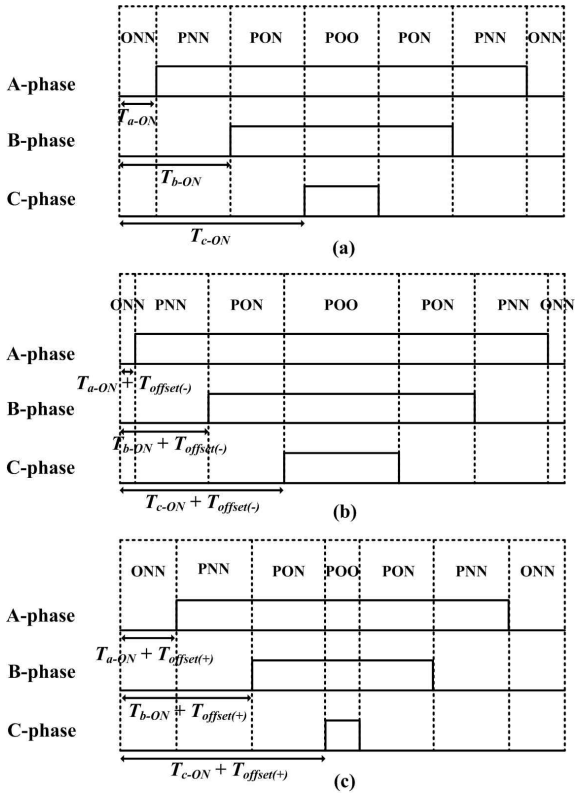

Fig. 3. Change in dwell time of small voltage vector: (a) normal operation; (b) when the negative time-offset $T_{offset(-)}$ is added; (c) when the positive time-offset $T_{offset(+)}$ is added.

By analyzing small-signal models for the neutral-point voltage developed using closed-form expressions, a compensator for neutral-point voltage balancing has been designed [11]. However, this paper does not contain analyses of the compensator gains. A PI compensator based on the continuous model has also been proposed in [12]. However, these methods require accurate system modeling. The performance of compensators based on modeling can differ according to conditions such as loads. Several alternative topologies were presented in [13], [14]. However, they are not cost-effective because they require additional hardware. Other approaches were proposed in [15]-[17]. However, their use is limited. Some of the methods can only be used in low modulation index [15], [16]. The method proposed in [17] can be applied when SHE-PWM is used.

This paper proposes a simple method to balance neutral-point voltage. The neutral-point voltage is balanced by adding an accurate time-offset at the gate-on time. The accurate time-offset can be obtained through the proposed time-offset estimation scheme.

II. INFLUENCE OF TIME-OFFSET ON THE NEUTRAL-POINT VOLTAGE

The small voltage vectors of an NPC inverter affect the neutral-point voltage. The N-type small switching state decreases the neutral-point voltage, and the P-type small switching state increases the neutral-point voltage when the inverter is in normal operation (inverting mode). Hence the dwell time of a small voltage vector should be divided equally. Conversely, if the dwell times of the P-type and N-type small voltage vectors are adjusted when the neutral-point voltage is unbalanced, the neutral-point voltage can be balanced.

Table I lists the switching states of the small voltage.

A. Change in Dwell Time of the Small Voltage Vector

The dwell times of the P-type and N-type small voltage vectors can be adjusted by adding a time-offset to the turn-on time of the switch. If the reference voltage falls into region 1 of sector I, as shown in Fig. 2, the dwell times of the P-type and N-type small voltage vectors are equally distributed in normal SVM, as shown in Fig. 3(a).

If the negative time-offset $T_{offset(-)}$ is added to the three phase turn-on times of switches (T_a, T_b, T_c), the dwell time of the P-type small voltage vector increases while that of the N-type small voltage vector decreases, as shown in Fig. 3(b). If the positive time-offset $T_{offset(+)}$ is added, as shown in Fig. 3(c), to the turn-on times of the switches, the dwell time of the P-type small voltage vector decreases and that of the N-type small voltage vector increases.

B. Change of the Neutral-Point Voltage by the Time-offset

As in the above analysis, the neutral-point voltage can be balanced by adding a time-offset T_{offset} to the turn-on times of the switches. If V_{DC1} is greater than V_{DC2}, the negative

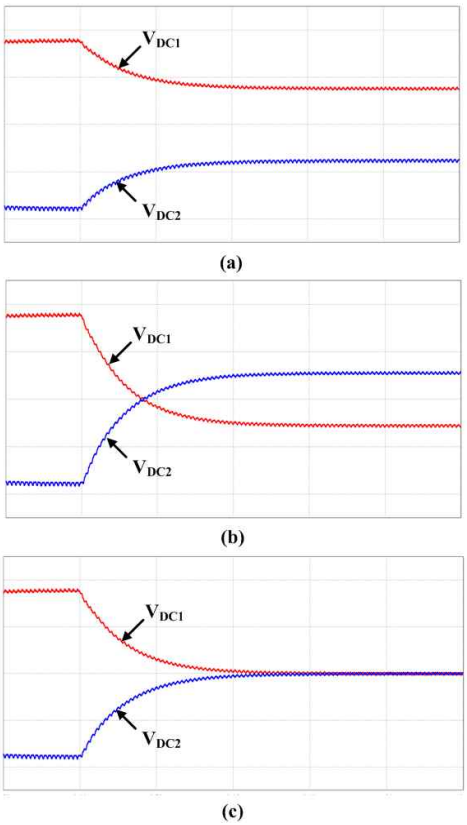

Fig. 4. Change of the neutral-point voltage (a) $T_{offset} < T_{correct}$; (b) $T_{offset} > T_{correct}$; and (c) $T_{offset} = T_{correct}$.

time-offset $T_{offset(-)}$ should be added to balance the neutral-point voltage. Conversely, if V_{DC1} is less than V_{DC2}, the positive time-offset $T_{offset(+)}$ should be added. However, if an incorrect time-offset is added, the neutral-point voltage still remains.

Fig. 4(a) shows the change in the neutral-point voltage deviation when a smaller time-offset T_{offset} than the correct time-offset $T_{correct}$ is added. The neutral-point voltage deviation becomes smaller than before the time-offset T_{offset} is added, but it still remains. If a time-offset T_{offset} greater than the correct time-offset $T_{correct}$ is added, V_{DC2} becomes greater than V_{DC1}, and the neutral-point voltage deviation still remains, as shown in Fig. 4(b). The neutral point is balanced when the added time-offset T_{offset} is equal to $T_{correct}$, as shown in Fig. 4(c). The neutral-point voltage can be balanced when the correct time-offset is added. However, it is difficult to find the precise time-offset $T_{correct}$ because it changes depending on the magnitude of the output phase current, the DC-link capacitor, the neutral-point voltage deviation, etc. It is also difficult to mathematically analyze the change in the neutral-point voltage by the time-offset T_{offset}.

III. Proposed Scheme to Balance the Neutral-Point Voltage

Fig. 5 illustrates a flowchart of the proposed neutral-point balancing scheme. In this paper, the difference between the two half-capacitor voltages (V_{DC1} - V_{DC2}) is defined as V_d, and the limit range of the normal condition is defined as $|V_{normal}|$, where V_{DC1} is the upper capacitor voltage, and V_{DC2} is the lower capacitor voltage. If $|V_d|$ is lower than $|V_{normal}|$, it can be assumed that the neutral-point voltage is balanced. If T_{offset} has a positive value, T_{offset} is expressed by $T_{offset(+)}$. Conversely, if it has a negative value, T_{offset} is defined by $T_{offset(-)}$. The modified turn-on times of the switches are defined as (1). According to V_d, the time-offset T_{offset} is changed to balance the neutral-point voltage, as expressed in (2).

$$T'_{x(x=a,\ b,\ c)} = T_{x(x=a,\ b,\ c)} + T_{offset} \tag{1}$$

$$T_{offset} = T_{offset\_old} \pm \Delta T_{offset} \tag{2}$$

where T_{offset} is the current value, T_{offset_old} is the previous value, and ΔT_{offset} is the changing value.

A. Changing the Magnitude of ΔT_{offset}

If the voltage difference $|V_d|$ is greater than $|V_{d\_max}|$, the time-offset T_{offset} is set by $|T_{offset\_max}|$. The maximum magnitude of the time-offset $|T_{offset\_max}|$ is set to not exceed the modulation index 1 and is calculated as:

$$m_a = \frac{\sqrt{3}}{V_{DC}}(V_{ref} + V_{\max}) = 1 \tag{3}$$

$$V_{\max} = (\frac{V_{DC}}{\sqrt{3}} - V_{ref}) \tag{4}$$

$$|T_{offset\_\max}| = (\frac{2V_{\max}}{V_{DC}} \times \frac{T_{sw}}{2T_{clock}} \times T_{clock}) = (\frac{V_{\max}}{V_{DC}} \times T_{sw}) \tag{5}$$

Substituting (4) into (5) yields:

$$|T_{offset\_\max}| = ((\frac{1}{\sqrt{3}} - \frac{V_{ref}}{V_{DC}}) \times T_{sw}) \tag{6}$$

If $|V_d|$ is in the range of $|V_{d\_min}|<|V_d|<|V_{d\_max}|$, ΔT_{offset} is set by αT_{clock}.

If $|V_d|$ is in the range of $|V_{d\_normal}|<|V_d|<|V_{d\_min}|$, ΔT_{offset} is set by βT_{clock}.

Lastly, if $|V_d|<|V_{normal}|$, ΔT_{offset} is set by 0 and $T_{offset} = T_{off\_old}$.

where the value of α can be (10~30), β can be (1~3) and T_{clock} is the clock of a digital signal processor.

α is the constant value for leading the time-offset to near the desired value and β is the other constant value to correct a slight error between the time-offset and the correct value. If β is big, more time to converge the time-offset to the desired value is required because β is applied in the small region. On the other hand, if α is small, a longer time is needed to move the time-offset close to the correct value. Therefore, α and β are

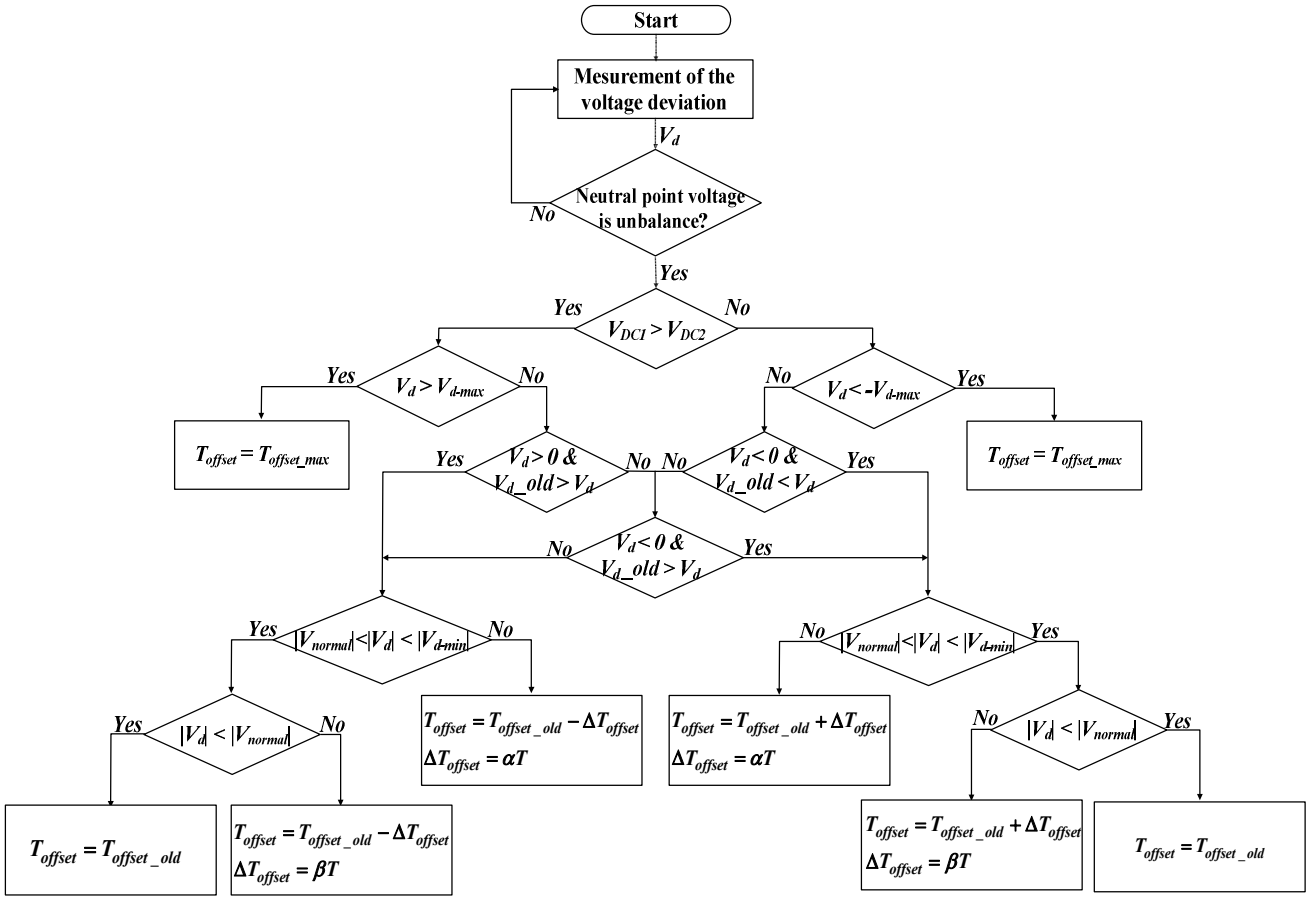

Fig. 5. Block diagram of proposed scheme.

determined as above.

B. Time-offset Estimation Scheme

The proposed time-offset estimation scheme is explained by dividing into two cases and considering five situations for each case.

■ $V_{DC1} > V_{DC2}$

In this case, a negative time-offset $T_{offset(-)}$ should be added to the turn-on times of the switches.

1) $|V_d| > |V_{d\text{-}max}|$: $T_{offset(-)}$ is set by the negative $T_{offset\_max(-)}$.

$$T_{offset(-)} = T_{offset\_max(-)}$$

2) $V_d > 0$ & $V_{d\_old} > V_d$: ΔT_{offset} should be subtracted from $T_{offset\_old(-)}$ because the voltage deviation still remains. $T_{offset(-)}$ is defined as:

$$T_{offset(-)} = T_{offset\_old(-)} - \Delta T_{offset}$$

3) $V_d < 0$ & $V_{d\_old} > V_d$: this situation occurs when the added time-offset $T_{offset\_old(-)}$ has a larger magnitude of the negative value than $T_{correct(-)}$. Therefore, ΔT_{offset} should be added to reduce the magnitude of the negative value. $T_{offset(-)}$ is defined as:

$$T_{offset(-)} = T_{offset\_old(-)} + \Delta T_{offset}$$

4) $V_d > 0$ & $V_{d\text{-}old} < V_d$: in this situation, ΔT_{offset} should be subtracted because the added time-offset $T_{offset\_old(-)}$ has a smaller magnitude of the negative value than $T_{correct(-)}$. The redefined $T_{offset(-)}$ is:

$$T_{offset(-)} = T_{offset\_old(-)} - \Delta T_{offset}$$

5) $|V_d| < |V_{normal}|$: in this situation it is considered that the neutral-point voltage is balanced. Hence, ΔT_{offset} is set by 0 and $T_{offset(-)}$ is equal to $T_{offset\_old(-)}$.

$$T_{offset(-)} = T_{offset\_old(-)}$$

■ $V_{DC1} < V_{DC2}$

In this case, a positive time-offset $T_{offset(+)}$ should be added to the turn-on times of the switches.

1) $|V_d| > |V_{d\text{-}max}|$: $T_{offset(+)}$ is set by a positive $T_{offset\_max(+)}$.

$$T_{offset(+)} = T_{offset\_max(+)}$$

2) $V_d < 0$ & $V_{d\text{-}old} < V_d$: ΔT_{offset} should be added to $T_{offset\_old(+)}$

because the voltage deviation still remains. $T_{offset(+)}$ is defined as:

$$T_{offset(+)} = T_{offset\_old(+)} + \Delta T_{offset}$$

3) $V_d > 0$ & $V_{d\_old} < V_d$: this situation occurs when the added time-offset $T_{offset(+)}$ has a larger magnitude of the positive value than $T_{correct(+)}$. Therefore, ΔT_{offset} should be subtracted to reduce the magnitude of the positive value. $T_{offset(+)}$ is defined as:

$$T_{offset(+)} = T_{offset\_old(+)} - \Delta T_{offset}$$

4) $V_d < 0$ & $V_{d\_old} > V_d$: in this situation, ΔT_{offset} should be added to $T_{offset\_old(+)}$ because $T_{offset\_old(+)}$ has a smaller magnitude of the positive value than $T_{correct(+)}$. $T_{offset(+)}$ is defined as:

$$T_{offset(+)} = T_{offset\_old(+)} + \Delta T_{offset}$$

5) $|V_d| < |V_{normal}|$: in this situation it is considered that the neutral-point voltage is balanced. Hence, ΔT_{offset} is set by 0 and $T_{offset(+)}$ is equal to $T_{offset\_old(+)}$.

$$T_{offset(+)} = T_{offset\_old(+)}$$

If the control period is short, it is difficult to check the change of the neutral-point voltage by the added time-offset T_{offset} during a period. Therefore, the time-offset T_{offset} is changed frequently. Conversely, if the control period is long, a lot of time is needed to balance the neutral-point voltage because the amount of the voltage change is large during a period. Hence the control period of the neutral-point voltage balancing scheme has to be considered.

IV. Experimental Results

Experiments have been carried out to confirm the validity of the proposed neutral-point voltage balancing scheme. The experimental setup is implemented using a 10 kW, NPC inverter system. Table II lists the parameters applied to the experiments.

Fig. 6 shows a photograph of the experimental power circuit. The digital controller is based on a (TMS320C28346) digital signal processor.

Fig. 7 shows the experimental results of the proposed scheme, according to the control period. Fig. 7(a) shows the two capacitor voltages and the estimated time-offset when the control period is proper. Table II lists the control period of the proposed scheme. The upper and lower capacitor voltages converged to half the value of the DC-link voltage at 80 V, and the time-offset converged to $-600T_{clock}$ in about 1.8 s after the proposed scheme is applied. If the control period of the

TABLE II

Parameters of the Experiments

Parameter	Value	Parameter	Value
DC-link voltage	160 V	Control period of proposed scheme	$5 \times T_{control}$ ($V_d > V_{d\_min}$)
Switching frequency	15 kHz		$20 \times T_{control}$ ($V_d < V_{d\_min}$)
Control period ($T_{control}$)	66.7 μs	V_{d_max}	10 V
T_{clock}	3.33 ns	V_{d_min}	3 V
Current	6 A	V_{normal}	1 V
Frequency of current	60 Hz	T_{offset_max}	$1150T_{clock}$
Load	10 Ω	ΔT_{offset}	$\alpha = 30$
	3 mH		$\beta = 1$

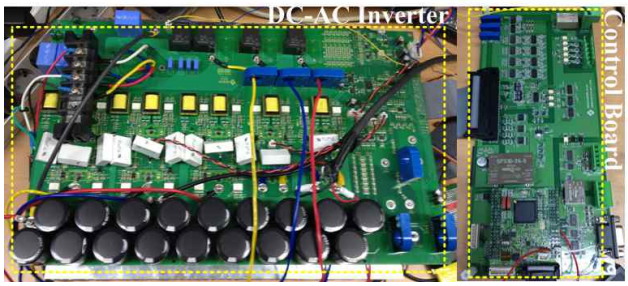

Fig. 6. Experimental setup of 10 kW, NPC inverter systems.

proposed scheme is too short, the upper and lower capacitor voltages oscillate in the steady state, and more time is needed than in the former case until the time-offset and two capacitor voltages converge to constant values, as shown in Fig. 7(b). In this case, the control period of the proposed scheme is $T_{control}$. Fig. 7(c) shows the upper and lower capacitor voltages and the time-offset when the control period of the proposed scheme is long. The control period of the proposed scheme is $25 \times T_{control}$. The two capacitor voltages and the time-offset converged to constant values about 2.5 s after the proposed algorithm is applied. More time is needed than that required for the first case.

Fig. 8 compares the output phase current before and after the proposed method is applied. When the neutral-point is unbalanced, the output phase current is distorted owing to the

low-order harmonic components, predominantly the second- and fourth-order harmonics. After the proposed algorithm is applied, the phase current distortion is eliminated, and the neutral-point voltage is balanced.

The FFT of the out phase current is illustrated in Fig. 9. The 2nd and 4th order harmonics are formed due to the neutral-point voltage deviation, as shown in Fig. 9 (a). After the proposed method is applied, these harmonics are eliminated as shown in Fig. 9 (b).

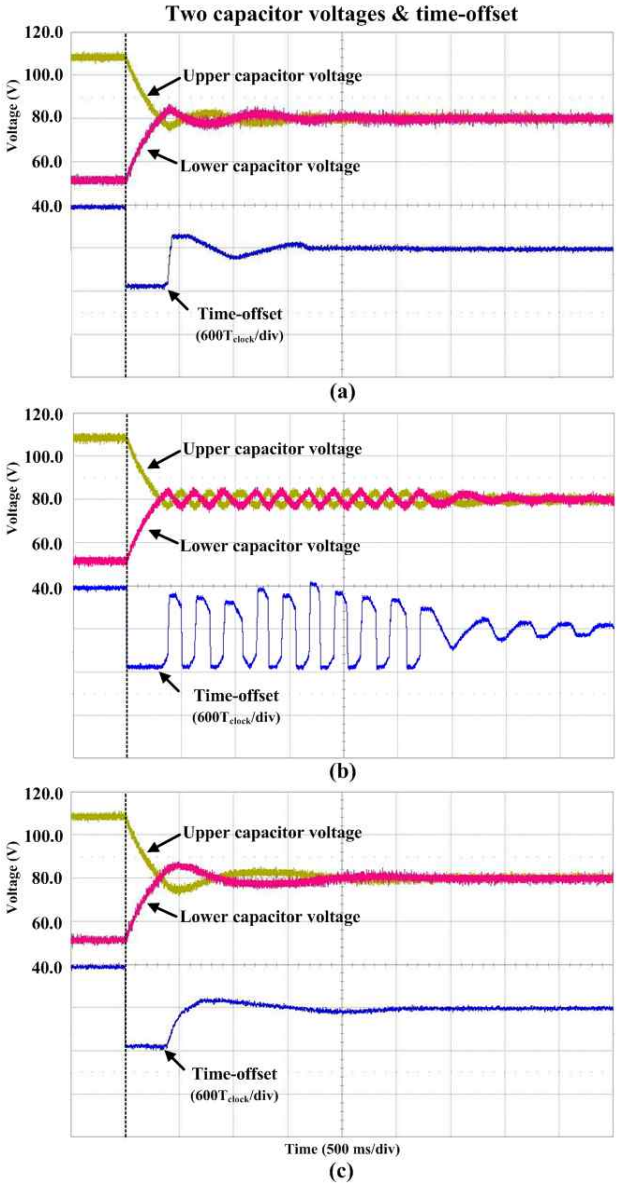

Fig. 7. Experimental results of the proposed algorithm when the period is (a) precise, (b) short, and (c) long.

V. CONCLUSIONS

This paper has presented a neutral-point voltage balancing scheme. The proposed method is implemented by adding a time-offset to the turn-on times of switches. An accurate time-offset is obtained through the proposed time-offset estimation scheme without complex calculations, modeling, or additional hardware. Furthermore, the proposed method does not affect the system performance. The experimental results confirm the feasibility and effectiveness of the proposed neutral-point voltage balancing method.

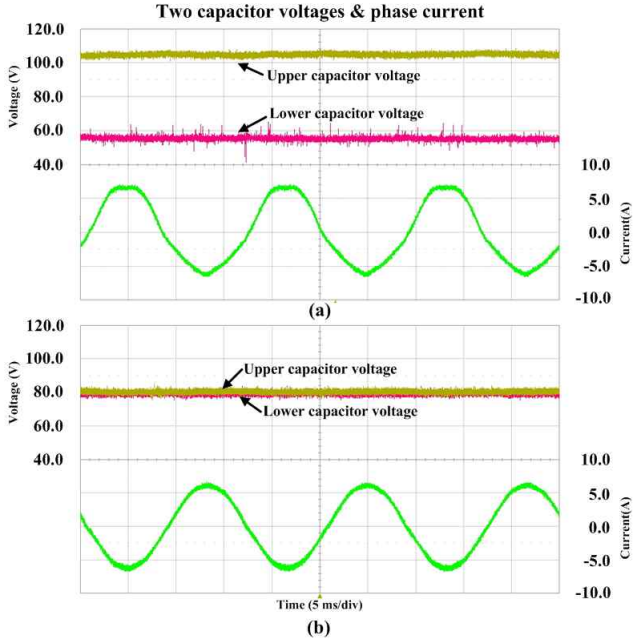

Fig. 8. Comparison of the output phase current (a) when the neutral-point voltage is unbalanced (b) after the proposed algorithm is applied.

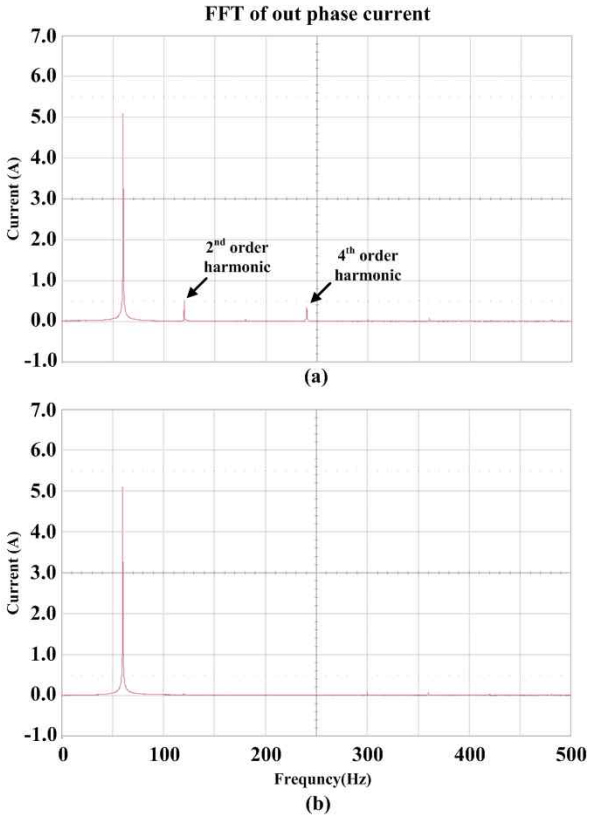

Fig. 9. FFT analysis of output phase current (a) when the neutral-point voltage is unbalanced (b) after the proposed algorithm is applied.

ACKNOWLEDGMENT

This work was supported by a National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (no. 20120002247).

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Ui-Min Choi was born in Icheon, Korea, in 1986. He received his B.S and M.S. in Electrical and Computer Engineering from Ajou University, Suwon, Korea, in 2011 and 2013, respectively. He is currently working toward his PhD. at Aalborg University, Aalborg, Denmark. His current research interests include power conversion, renewable power generation, multilevel inverters and reliability.

Kyo-Beum Lee was born in Seoul, Korea, in 1972. He received his B.S. and M.S. in Electrical and Electronic Engineering from Ajou University, Suwon, Korea, in 1997 and 1999, respectively. He received his Ph.D. in Electrical Engineering from Korea University, Seoul, Korea, in 2003. From 2003 to 2006, he was with the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From 2006 to 2007, he was with the Division of Electronics and Information Engineering, Chonbuk National University, Jeonju, Korea. In 2007 he joined the Department of Electrical and Computer Engineering, Ajou University, Suwon, Korea. He is an Associated Editor of the IEEE Transactions on Power Electronics, the IEEE Transactions on Industrial Electronics, and the Journal of Power Electronics. His current research interests include electric machine drives and renewable power generation.