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Implementation of a Non-Linear Adaptive Filter Based Sag Detection Method for Dynamic Voltage Restorers under Unbalanced Fault Conditions

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Abstract

The most common power quality problems in distribution systems are related to unbalanced voltage sags. Voltage sags must be detected quickly and corrected in a minimum amount of time. One of the most widely used methods for sag detection is based on the d-q transformation. This method has the disadvantage of missing the detection of unbalanced faults, because this method uses a voltage sag level signal obtained from the average of 3 phases for sag detection. In this paper, an adaptive filter sag detection method is proposed for Dynamic Voltage Restorers (DVR) under unbalanced fault conditions. The proposed DVR controller is able to detect balanced, unbalanced and single phase voltage sags. A novel reference voltage generation method is also presented. To validate the proposed control methods, a 3-phase DSP controlling a DVR prototype with a power rating of 1.5-kVA has been developed. Finally, experimental results are presented to verify the performance of the proposed control methods.

Key words: Dynamic Voltage Restorer, Power Quality, Reference Voltage Generation, Sag Detection

I. INTRODUCTION

Power quality is crucial for the companies operating in a highly competitive business environment because of its effects on profitability, which is definitely a driving force in industry. This increasing interest on the improvement of efficiency and the elimination of variations in industry has resulted in more complex instruments. These instruments tend to be more sensitive to voltage disturbances such as voltage sags, voltage swells, outages, harmonics, interruptions and phase shifts. Voltage sags are considered to be the most severe power quality problem since sensitive loads are very susceptible to temporary changes in voltage.

A DVR is a power quality device, which can protect these plants against the bulk of these disturbances, i.e. voltage sags and swells related to remote system faults. A DVR compensates for these voltage excursions provided that the supply grid does not get disconnected entirely through breaker trips [1]-[3].

The main considerations for the control system of a DVR include: The sag detection method and reference voltage generation method for transient/steady state control of the injected voltage. Voltage sags must be detected quickly and corrected with a minimum of false operations. One of the most widely used methods for sag detection is based on a d-q transformation. Thus the three phase set of voltages are transformed into the d-q domain [4], [5]. The monitoring of $\sqrt{V_d^2 + V_q^2}$ or V_d in a vector controller is the simplest type of sag detection. This will return the state of the supply at any instant in time and hence detect whether or not a sag has occurred [6]. To separate the positive and negative sequence components, low pass filters (LPFs) are used after the d-q transformation in the literature. For effective removal, the cut-off frequency of the low pass filter must be reduced, but this method has the side effect of reducing the controller response time [7]. However, this method has the disadvantage of missing the detection of single phase-to-ground faults

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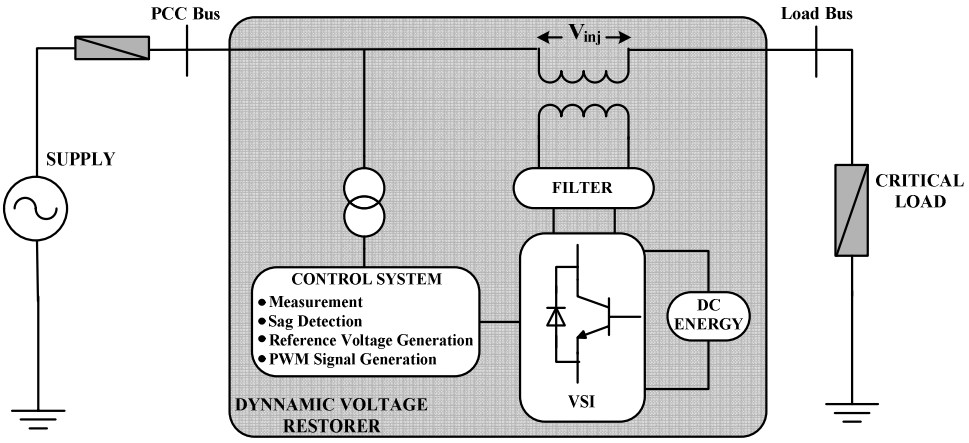

Fig. 1. Single line diagram of the proposed DVR system.

when the permissible voltage sag limit is selected to be 10%. This is due to the fact that this method compares a reference obtained from the average of three phases to the voltage sag limit. In [8], various applications for a nonlinear adaptive notch filter which operates based on the concept of an enhanced phase locked loop (PLL) are presented. This filter can be used for sinusoidal waveform peak detection, harmonic identification/detection, detection/extraction of the individual components of a signal, and amplitude (phase) demodulation for flicker estimation.

In this paper, the signal analysis method in [8] is developed for a sag detection algorithm. By using this approach, the detection time can be further improved with respect to the conventional methods using a LPF. This adaptive filter method is also used for reference voltage generation in this paper. The mitigation device and control algorithms presented in this study differ from the previously discussed approaches in the following ways:

(i) An algorithm for unbalanced voltage sag detection is presented. A passive filter with a low cut-off frequency is not used in the sag detection. When a single phase fault occurs in the system, it is difficult to compensate the faulty voltage using d-q transformation method. This is because the fault analysis is achieved by using the average of three phases and the depth of the voltage sag is not calculated correctly which can cause the sag detection unit to operate incorrectly. The proposed method can detect single phase voltage sags correctly. The extraction and tracking of disturbances are quick and accurate

(ii) A novel reference voltage generation method is presented which is used in the voltage compensation of a DVR. Most of the methods in the literature have drawbacks in terms of generating compensation signals experimentally when the supply voltage contains distortions. With this approach, "distortions in the supply line are perfectly filtered" and a pure sinusoidal reference voltage is obtained.

(iii) Each phase is controlled independently. Thus minimum voltage injection is obtained during faults.

In the following sections, the basic DVR principle will be given. Next, the PLL method is presented. In section IV, the conventional and proposed sag detection methods will be compared. The proposed voltage compensation strategy will be described in Section V. The Digital Signal Processor (DSP) controlling the experimental DVR hardware and the flowcharts of control methods used in DSP will be described in section VI. Finally, experimental results using a low voltage 1.5-kVA DVR prototype will be shown to verify and prove the functionality of the presented control methods in both single phase unbalanced and three phase balanced voltage sag conditions.

II. CONFIGURATION OF THE PROPOSED DVR

The DVR is composed of a control unit, DC energy storage, H-bridge voltage source inverters (VSI), a harmonic filter and an injection transformer, as shown in Fig. 1. A regulated DC supply with a constant output is employed as the energy storage of the inverter. Three single-phase H-bridge Pulse Width Modulation (PWM) inverters consisting of IGBT switches are used in the VSI circuit. The use of the single-phase H-bridge PWM inverters in the DVR power circuit makes the injection of positive, negative and zero sequence voltages possible. As a result, this topology will be able to control each phase independently. Inverter side filtering is preferred in this study. Using this filtering scheme, the high order harmonic currents are prevented from penetrating into the series transformer. Thus it reduces the voltage stress on the transformer. The VSI rating is relatively low in voltage and high in current due to the use of injection transformers. The designed sag generator system consists of variable voltage sources, thyristors pairs, thyristors drivers, protection devices and time relays. The sag generator creates balanced or unbalanced faults at a desired time and magnitude.

In the control unit, sag detection and voltage compensation methods are processed. This paper proposes simple and

effective control algorithms for both sag detection and voltage compensation. The proposed algorithms are based on the nonlinear adaptive filter presented in [8] and this filter can be used as a PLL. The PLL is the heart of the sag detection and reference signal generation. The presented PLL algorithm also has the ability to detect the peak of the signal and to extract the harmonics.

III. NONLINEAR ADAPTIVE FILTER AND PHASE LOCKED LOOP

The phase locked loop is comprised of a phase detector, a loop filter and a voltage controlled oscillator. In Fig.2, a block diagram of the PLL is given. The PLL tracks a specific component of the input signal and simultaneously extracts its amplitude and phase. The error signal represents the deviation of the input signal from the output signal.

The following discrete equations shown in (1), (2), (3) and (4) are used for the adaptive filter:

$$e(t_k) = u(t_k) - y(t_k) \tag{1}$$

$$A(t_{k+1}) = A(t_k) + T_s * K * e(t_k) * \sin(\theta(t_k) - \pi/2) \tag{2}$$

$$y(t_{k+1}) = A(t_{k+1}) * \sin((\theta(t_k) - \pi/2) \tag{3}$$

$$\theta(t_{k+1}) = \theta(t_k) + T_s \left\{ K_p * K_v * e(t_k) * \sin(\theta(t_k)) + w_0 \right\} \tag{4}$$

u(t) is the input signal to the PLL that will be tracked while *y(t)* is the output. *A(t)* is the amplitude and *θ(t)* is the phase angle of the tracked signal. *e(t)* is used to represent the error signal which represents the difference between the input signal and the output signal. w_0 determines the frequency of the output signal and is defined as $2\pi f$. The generated output signal *y(t)* is both in phase and amplitude with the input signal *u(t)*. In other words, *y(t)* is the same as *u(t)*. The initial conditions are chosen as $\theta(0) = 0$, $A(0) = 0$ and $y(0) = 0$.

IV. SAG DETECTION METHOD

The proposed sag detection method is compared with the conventional method using the d-q transformation to show its superiority. In the conventional method [4-5], the phase-to-neutral voltages V_a, V_b and V_c are transformed to the d-q plane as given in Eq. (5). With the use of Eq. (6), the sag level (SL_{conv}) is obtained.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{5}$$

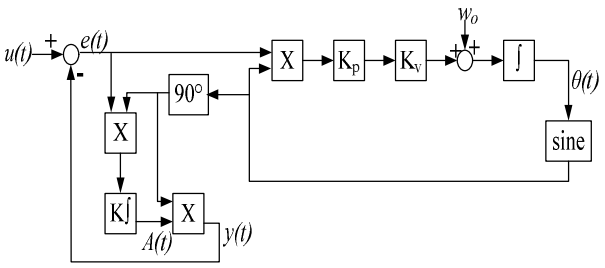

Fig. 2. Block diagram of the PLL

$$SL_{conv} = \left| 1 - \sqrt{V_d{}^2 + V_q{}^2} \right| \tag{6}$$

In Fig. 3(a), a block diagram of the d-q transformation based sag detection method is shown. After the three phase sets of voltages are transformed into d and q components, the square root of the sum of squares of these components is obtained. The obtained value is subtracted from 1 (the reference value) and then the absolute value of the resulting variable is filtered out with a 50 Hz low pass filter. The filtered output is subjected to a hysteresis comparator and the output of this comparator generates the sag detection signal. This signal is high when a sag occurs, otherwise it is low. The D-q sag detection method is able to detect a three phase balanced voltage sag with an acceptable performance. However, the most important disadvantage of this method is that it uses three phase voltage measurements for the detection. This method is unable to detect voltage sags lower than a definite level. As an example, a single phase to ground fault resulting in a 15% voltage sag can not be determined by this method because is uses the average of the three phase voltages and perceives the single phase voltage sag as an average value of 5% if the voltage sag detection limit is selected to be 10%. Another restriction of this method is the use of a low pass filter tuned at 50 Hz. This filter reduces the response speed of the detection scheme. To overcome the disadvantages of the d-q sag detection method, the PLL explained in the previous section is used in this study. With the proposed method, the controller is able to detect balanced, unbalanced and single phase voltage sags without errors. In this method, three PLLs are used to track each of the three phases. The signal *A(t)*, depicted in Fig. 2, gives the amplitude of the tracked signal *u*(t). For example, if the amplitude of the measured phase B voltage is 220 V_{rms}, the *A(t)* signal is obtained as a continuous 1 pu. If the amplitude falls to 187 V_{rms}, the amplitude of the *A(t)* signal falls to 0.85 pu. Figure 3(b) presents the voltage sag detection method using the PLL. By subtracting the *A(t)* signal from the ideal voltage level (1 pu), the voltage sag level (SL_{prop}) can be detected. The comparison of this value with the limit value of 10% (0.1 pu) points to a voltage sag.

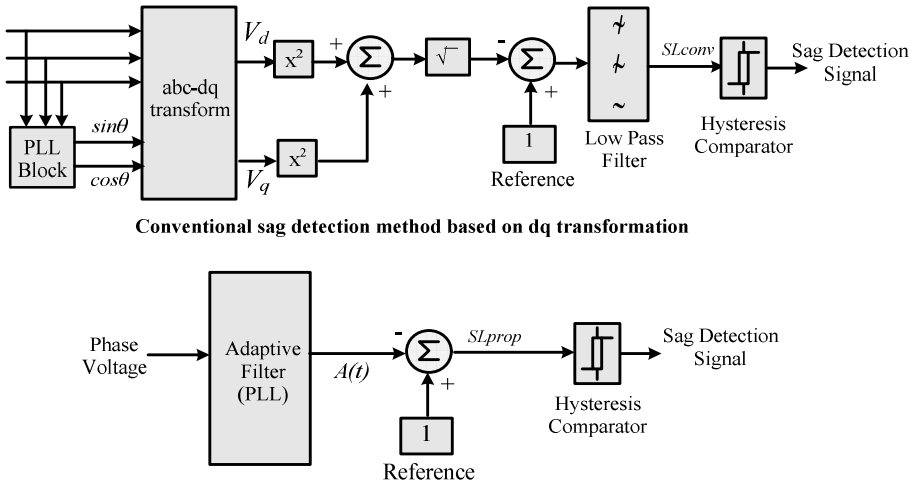

Fig. 3. Block diagram of (a) Conventional and (b) Proposed sag detection methods.

$$SL_{prop} = \left|1 - A(t)\right| \tag{7}$$

Fig. 4 shows the voltage sag level signals of the conventional and proposed methods in the case of a 15% voltage sag occurring on Phase B. The single phase voltage sag occurs between 0.2 and 0.3 ms. As shown in Figure 4, the conventional method can not detect the sag. However, the proposed method can detect the sag level with an exact certainty.

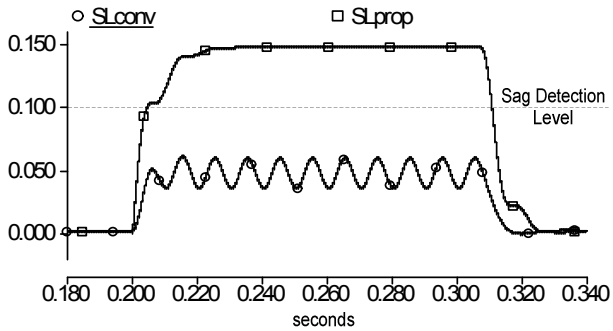

Fig. 4. Determined voltage sag levels by using conventional and proposed sag detection methods.

V. VOLTAGE COMPENSATION METHOD

The proposed method was verified by experimental results. Most of the methods in the literature have drawbacks when generating compensation signals when the supply voltage is unbalanced or contains distortions. This paper proposes a simple control algorithm for the DVR. With this method, the experimental control system of the DVR is not affected by system distortions. This method directly calculates compensation voltages without a time delay and compensates for faulted voltages dynamically in the time domain.

A. Reference Voltage Generation

For reference voltage generation, another property of the PLL is used. The output *y(t)* shown in Fig. 5 is an extracted signal from the input *u(t)* having the amplitude *A(t)* and phase *θ(t)* of the input *u(t)*. With this approach, the "distortions in the supply line are perfectly filtered" and a pure sinusoidal reference voltage is obtained.

$$V_{ref1} = u(t) - y(t) \tag{8}$$

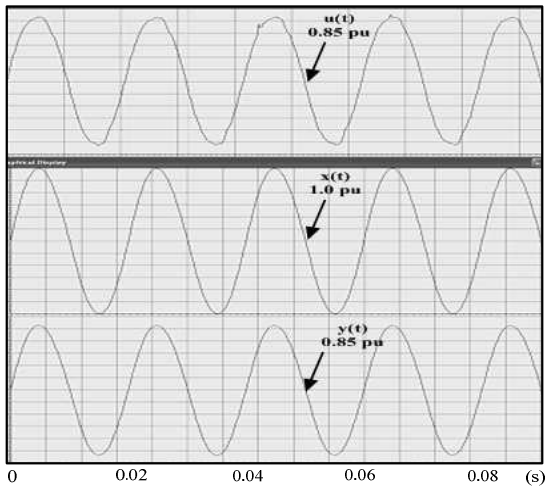

Fig. 5. Measured supply voltage u(t), reference signal x(t) and extracted y(t).

In the proposed method, a reference sinusoidal signal *x(t)* having a magnitude of 1 pu and a phase angle of *θ(t)* is used. A reference voltage signal is generated (11) from the difference between *y(t)* and *x(t)*.

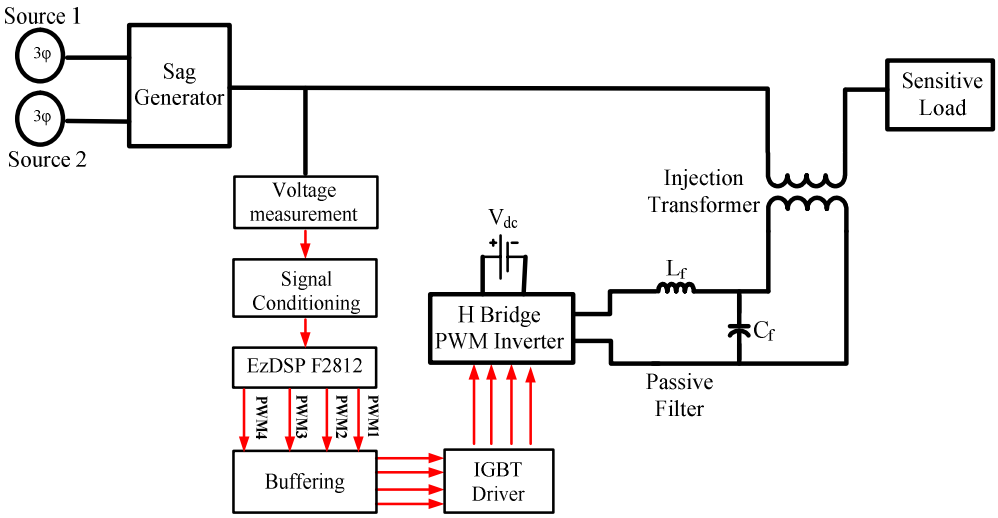

Fig. 6. The block diagram of experimental prototype of DVR.

$$x(t) = 1.\sin(\theta(t)) \quad (9)$$

$$y(t) = A(t).\sin(\theta(t)) \quad (10)$$

$$V_{refpure} = x(t) - y(t) \quad (11)$$

If (8) is used for the reference voltage generation, this reference voltage will contain distortions and negatively effect the control signals during the experimental study. The voltage compensation signal $V_{refpure}$ is compared with a fixed frequency carrier wave to generate the firing pulses as PWM signals. In this way, a voltage with the same phase as the supply side generated by the DVR voltage source inverter is injected to the load side.

B. Minimum Energy Injection and Stand-by Operation

When a single phase fault occurs, it is not necessary to operate all of the inverters. However, in conventional methods all of the H-bridges are operated at the same time resulting in increased losses. In this paper, by using an independent sag detection element for each phase, each H-bridge inverter is controlled independently. With this method, minimum energy is injected and the switching losses are reduced when single phase or double phase faults occur. Most of the time the DVR is in standby mode and conduction losses will account for the bulk of the converter losses during operation [1]. In most of the DVR studies, the injection transformer operates like a secondary shorted current transformer using bypass switches in this mode. In this study, an alternative solution is presented for the standby operation of the DVR. During the standby operation of the DVR, the two lower IGBTs in each phase remain turned on while the two upper IGBTs remain turned off. To obtain a short circuit across the secondary (inverter side) windings of the series transformer through L_F, the use of bypass switches is thus eliminated [10]. When a voltage sag is detected, the DVR reacts as quickly as possible and injects the missing voltage into the grid.

VI. Implementation of DSP Based DVR Prototype

The main objective of this section is to present a description of both the DSP controlled experimental hardware of the DVR and an implementation of the proposed control methods.

A. Experimental Setup

A block diagram of the experimental prototype of the proposed 3 phase 3 wire DVR system is given in Fig. 6. A 1.5-kVA, 400-V, 3-phase DVR prototype is designed and implemented in the laboratory. The experimental prototype consists of the components shown in Table I.

B. Flowcharts of the Control Methods Used in the DSP

The flowcharts for the proposed control algorithms and comprehensive information are given in this section. A TMS320F2812 ezDSP board is used in the experimental study. This board has a built in Analog to Digital Converter (ADC) module and PWM modules to control the DVR. All of the control codes are written in C language using Code Composer Studio.

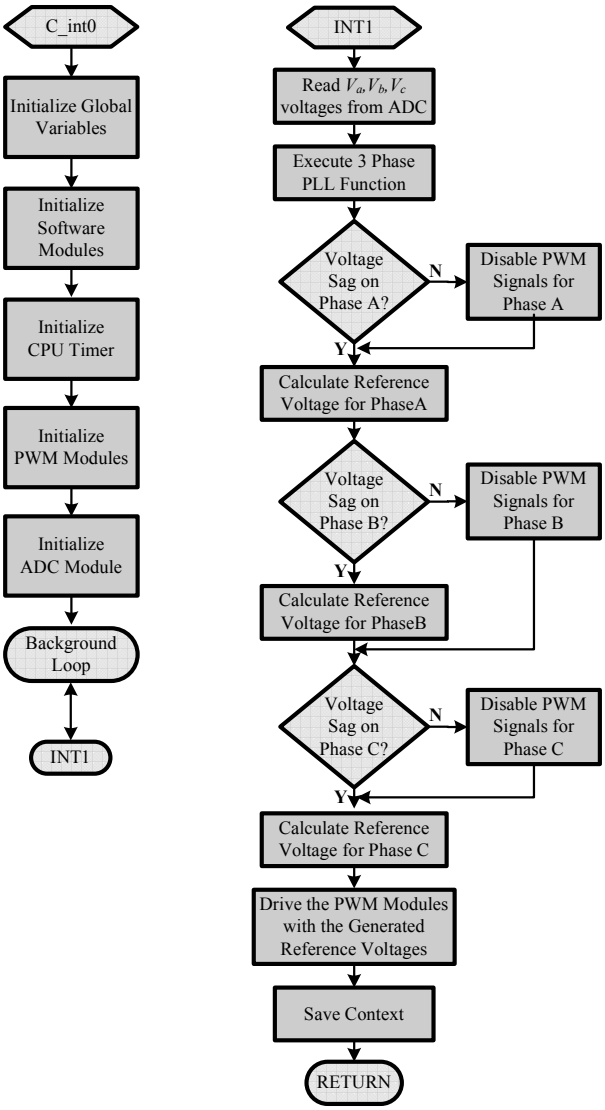

Fig. 7. The general flowchart for the control of the proposed experimental system.

The processor timer of a F2812 Digital Signal Processor (DSP) is used to generate the timing interrupts to determine the sampling time. The control algorithm starts with a "*main*" function and then waits for the timer interrupt. Fig. 7 shows a general flowchart of the proposed experimental system. The processor starts with C_int0 interrupt and runs the "main" function given on the left hand side of Fig. 7. Initially, the global variables that will be used throughout the entire control algorithm are defined and initialized in the main function. Then, software modules that let the programmer develop algorithms by the use of the object oriented approach are initialized. Then, the processor timer and the CPU timer are adjusted to determine the sampling interval. The sampling time is selected to be 20 μs. The PWM modules are then set to give the required outputs. The carrier wave frequency of the PWM modules is set to 10 kHz. In the last step, to obtain the voltage measurements, the ADC module is initialized. After the completion of all the required initialization work, the processor sits in an endless loop and waits for the processor timer interrupt, INT1.

TABLE I

LIST OF COMPONENTS FOR EXPERIMENTAL SETUP

Component	Features
Voltage measurement and signal conditioning cards	LEM LV 25-400 voltage transducers, LM324 and other passive circuit elements are used.
TMS320F2812 ezDSP	A fixed step DSP with 20 μs sampling time. Includes sag detection and voltage compensation algorithms written in C language. The PWM switching frequency is set to 10 kHz.
IGBT driver card	Semikron SKHI 22-2 IGBT drivers
H-bridge inverter	**S**emikron SKM75GB123D IGBTs
DC energy storage system	Regulated DC voltage at 150 V
LC passive filter	L=5 mH, C=18 μF
Series injection transformer	2 kVA, 110-110 V_{rms}
Load	Pure Resistive, 98 Ω
Two incoming 3 phase feeders	400 V, 50 Hz, negligible impedance
Sag generator system	Thyristors pairs, thyristors drivers, protection devices and time relays

The CPU timer calls the interrupt service routine INT1, shown on the right hand side of the Fig.7, periodically every 20 μs. In this routine, the ADC module is driven to read the three phase sets of voltages and convert them into pu equivalents. Then these converted voltages are subjected to the three phase PLL function. Using the values obtained from the PLL function, each phase is controlled by the sag detection function. If a voltage sag is detected, the reference signal for that phase is calculated, otherwise the PWM module for that phase is disabled during that sampling interval. Finally, the calculated reference signals for the faulted phases are compared with the PWM carrier wave, and the PWM gate pulse signals for the related phases are generated.

Fig. 8(a) shows a flowchart of the used PLL function. The PLL function uses the measured phase-to-ground voltages as parameters. Then the error signals for each phase are determined. The values of the sine and cosine are calculated and then the amplitudes for the phases are determined. The product of amplitude *AA* and *sinwt* gives y_a which is a filtered copy of phase A generated by the PLL. Likewise, y_b and y_c are calculated and then the phase angles are determined. Each phase angle is restored to zero after a period of 2π.

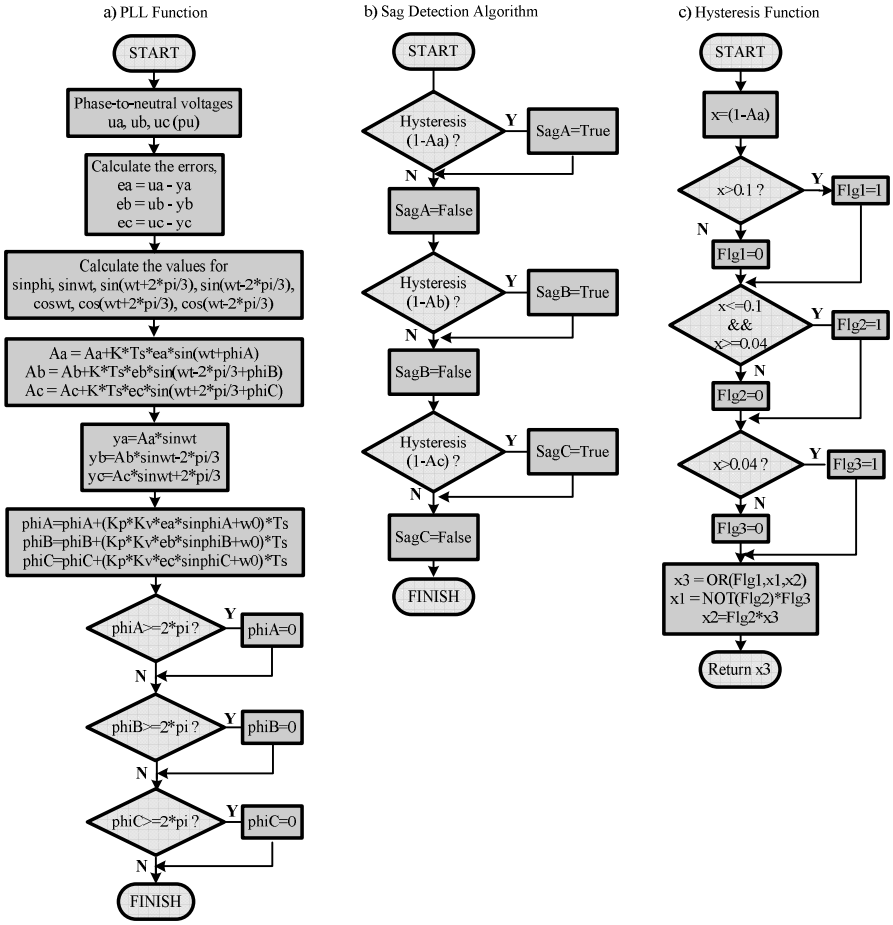

Fig. 8. Flowcharts for (a) PLL function (b) Sag detection algorithm (c) Hysteresis functions for phase A.

Fig. 8(b) shows the flowcharts for the sag detection function. As previously stated, the sag detection function is based on the PLL variables. Each of the phase amplitudes *AA*, *AB* and *AC* obtained from the PLL is subjected to the hysteresis function and the sag is determined by the result coming from the hysteresis function. The hysteresis function shown in Fig.8c has the duty of stabilizing the sag signals because harmonics and measurement noises affect the stability of the sag detection. The sag signal is set when the input signal to the hysteresis function exceeds the 0.1 limit and it is reset when the signal falls below 0.04. The variables x and x_3 shown in Fig.8 c represent the sag level signal and sag detection signal, respectively.

The control algorithm periodically reads the supply voltage and determines the voltage sag for each phase independently. If it detects a sag in a phase, it drives the H-bridge inverter of that phase only. In the following section, the experimental results are discussed.

e_a, e_b, e_c: the error signals determined for phases A, B and C, respectively.

u_a, u_b, u_c: the measured phase-to-ground voltages in pu.

y_a, y_b, y_c: the filtered copies of phases A, B and C.

A_a, A_b, A_c: the calculated amplitudes for phases A, B and C.

phiA, phiB, phiC: the calculated phase angles for phases A, B and C.

VII. Implementation Experimental Results

In this section, the experimental results for two different voltage sags are presented. For Case A, the system is tested to validate the operation of the sag detection algorithm for single phase faults. For Case B, the DVR is tested to show the voltage sag compensation capability of the proposed system. For all of the experiments, the data previously given in Table 1 are used and the measurements are taken using a HIOKI 3196 Power Quality Analyzer.

A. 15% Single Phase Unbalanced Voltage Sag

In this case, the sag detection strategy is tested during a 15% single phase voltage sag. Fig. 9 shows the voltage and current waveforms at the start of a single phase 15% voltage sag. The voltage waveforms of Ch1, Ch2 and Ch3 indicate the phase A supply voltage, the phase A load voltage and the injected voltage at the load side, respectively. The current waveforms of Ch1, Ch2 and Ch3 indicate the phase A, phase

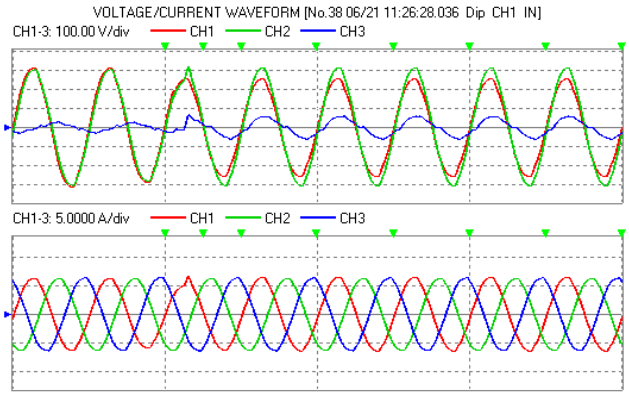

Fig. 9. Voltage/Current waveforms for starting of a single phase 15% sag.

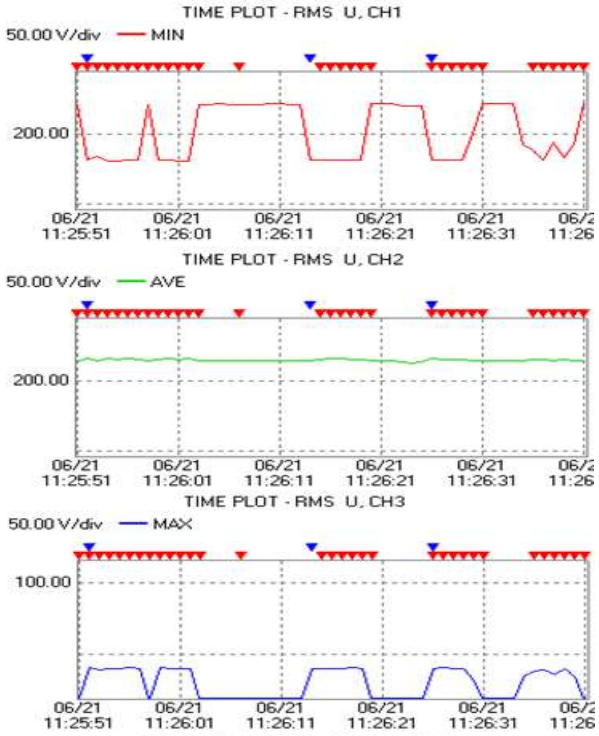

Fig. 10. RMS voltage trends for various single phase 15% sags.

B and phase C load currents, respectively. The load voltage waveform is identical to the load current waveforms because the load is purely resistive. As shown in Fig.9, when the sag occurs, only the related H-bridge inverter of the DVR starts to operate. The current waveforms also show that the sag occurs only on phase A and phase A load current so its voltage is not affected by the sag. The sag can clearly be seen in the waveform of the supply voltage. However, the load current (and voltage) remains within its specifications and the sag does not have an influence on the load voltage. Fig. 10 shows the rms results of the supply voltage for a 15% voltage sag occurring at different time instants. Ch1, Ch2 and Ch3 indicate the rms values of the phase A supply voltage, the phase A load voltage and the injected voltage at the load side, respectively. From these results it can be seen that the DVR responds rapidly to sags occurring at different times and that

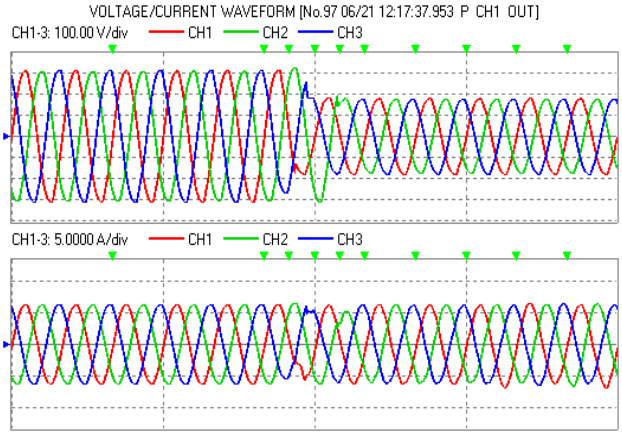

Fig. 11. Voltage/Current waveforms for starting of a three phase 40% voltage sag.

it keeps the load voltages almost constant.

B. 40% Three Phase Balanced Voltage Sag

During this case, a balanced fault takes place thus leading to a three-phase voltage sag. The supply voltage drops to 60% of its nominal value during the fault. Fig.11 shows the waveform results measured by the power quality analyzer. The voltage waveforms of Ch1, Ch2 and Ch3 indicate phase A, phase B and phase C of the supply voltages, respectively. Similarly, the current waveforms of Ch1, Ch2 and Ch3 indicate phase A, phase B and phase C of the load currents, respectively.

From Fig.11 it can be seen that with the use of the proposed voltage compensation method, the load current and the load voltage are not affected by the voltage sag. The load voltage is only affected at the starting and ending times of the sag due to the instantaneous reduction of the voltage reference and the delay originating from the sag detection time. During normal operating conditions, the supply voltage THD is 2.15% and the load voltage THD is 1.69%. However, the THD values of the supply voltage and the load voltage are measured as 2.17% and 3.01% during the voltage compensation, respectively. The load voltage THD value is kept below the voltage distortion limits stated in [11].

VIII. CONCLUSIONS

This paper presents an effective voltage sag detection method for unbalanced faults originated from the supply side. It uses the possible approaches for minimum energy injection and components reduction for the DVR. With the proposed sag detection method, the disadvantages of the conventional methods are eliminated and single phase faults are correctly measured in minimum time. The unbalanced voltage sags are compensated with minimum energy injection due to the

individual control of the H bridge inverters for each phase. In addition, a novel reference voltage generation method is presented which is used in the voltage compensation of the DVR. Most of the methods in the literature have drawbacks in generating compensation signals experimentally when the supply voltage contains distortions. With the proposed method, the experimental control system of the DVR is not affected by system distortions. The performance of the DSP based DVR has been tested experimentally. The results have shown the superior features of the DVR for sag detection and voltage compensation while meeting the requirements of IEEE 519 Std. The proposed sag detection and/or reference signal generation methods can be employed as a controller system for other Custom Power Devices such as a Static Transfer Switch and/or a Unified Power Quality Conditioner.

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