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The Effect of Transformer Leakage Inductance on the Steady State Performance of Push-pull based Converter with Continuous Current

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Abstract

As a result of the advantages such as high efficiency, continuous current and high stability margin, push-pull converter with continuous current (PPCWCC) is competitive for battery discharge regulator (BDR) which plays an important role in power conditioning unit (PCU).Leakage inductance yields current spike in low-ripple current of PPCWCCs. The operating modes are added due to leakage inductance. Therefore the steady state performance is affected, which is embodied in the spike of low-ripple current. PPCWCCs which are suitable for BDR can be separated into three types by current spike characteristics. Three representative topologies IIs1, IIcb2 and Is3 are analyzed in order to investigate the factors on the magnitude and duration of spike. Equivalent current sampling method (ECSM) which eliminates the sampling time delay and achieves excellent dynamic performance is adopted to prevent the spike disturbance on current sampling. However, ECSM reduces the sampling accuracy and telemetry accuracy due to neglecting the spike. In this paper, ECSM used in PPCWCCs is summarized. The current sampling error is analyzed in quality and quantity, which provides the foundation for offsetting and enhancing the telemetry accuracy. Finally, current sampling error rate of three topologies is compared by experiment results, which verify the theoretical analysis.

Key words: Current sampling error, Current spike, Equivalent current sampling, Leakage inductance, Push-pull converter

I. INTRODUCTION

Satellite power supply system which is an important element of satellite is a system that generates, stores, transforms and distributes electricity. As the core of Satellite power supply system, primary electrical power system powers the equipments in satellite and protects power supply system. A joint-power-supply consists of solar array and lithium-ion battery is adopted due to the merits of high reliability, long serving life and light weight [1]-[9]. Power conditioning unit (PCU) which is mainly composed of battery discharge regulator (BDR), battery charge regulator (BCR) and solar array regulator (SAR) is a typical primary electrical power system. The architecture of PCU is shown as Fig.1. Compared with the multisource power generation system in [10] and [11], the charge current of the PCU shown in Fig.1 can be controlled precisely, which is beneficial to prolong the battery life.

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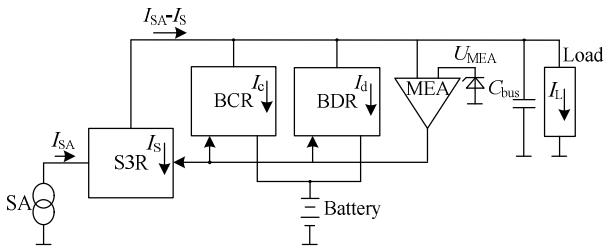


Fig. 1. Diagram of PCU.

When satellites can't get enough energy from solar array in shadow region or sunshine region, BDR regulates the power that flows from battery to load. PPCWCC is widely adopted as BDR on account of high efficiency, continuous current and convenience to parallel.

Input and output current of PPCWCC are both above zero at any time. If the turn ratio of transformer and coupled inductor are designed properly, input or output current of PPCWCC will be low-ripple which means the average current during switch-on state is equal to that during switch-off state. PCU is a three-domain control system, which is controlled by the bus current of BCR, BDR and S3R

to regulate the bus voltage. It's more convenient to sample if the bus current is low-ripple [12]. Therefore, PPCWCC whose output current is low-ripple is suitable for BDR.

At present, Weinberg converter which is belong to PPCWCCs has been already adopted as BDR in several PCUs with different models [13]-[16]. Although output current of Weinberg converter is low-ripple, the spike exists in output current. Reference [17] and [18] analyze the current spike of Weinberg converter briefly. However, the current spike hasn't been analyzed in detail, such as the magnitude and average value of current spike. The impact of current spike is also not mentioned. Actually, for PPCWCCs which are suitable for BDR, current spike always exists in output current, which is induced by leakage inductance. The current sampling accuracy and telemetry accuracy are impacted by current spike. Thus it's essential to pay attention on current spike of PPCWCC.

A series of PPCWCCs are proposed in [19], [20]. This paper focuses on PPCWCCs whose output current is low-ripple. They are classified into three types based on different characteristics of current spike. Three topologies which represent three spike characteristics are analyzed in quality and quantity to investigate the main factors that influence the magnitude and duration of current spike. The error that is introduced by equivalent current sampling method (ECSM) is also analyzed and compared.

This paper is organized as follows. Section II proposes the concept of PPCWCC and divides them into three types. Section III analyzes the current spike of topology IIs1, IIcb2 and Is3 in quality and quantity. Section IV summarizes the factors on current spike. To overcome the disturbance of current spike, section V introduces ECSM, while section VI analyzes the problem induced by ECSM. Finally the experimental results and conclusions are given in section VII and VIII.

II. CLASSIFICATION OF SPIKE CHARACTERISTICS

As is shown in Fig. 2, four kinds of push-pull cells which are the core of PPCWCC are named as I, II, III and IV.

Compared with traditional push-pull cell, push-pull cell I, shown as Fig. 2(a), connects the centre tap of secondary winding with positive terminal of power supply, which boosts voltage with continuous input and output current. For push-pull cell I, MOSFET is connected with the primary winding. When Q_1 is switched on, the potential of transformer which is negative in homonymous-ends makes the diode D_1 switch on; When Q_2 is switched on, the potential of transformer which is positive in homonymous-ends makes the diode D_2 switch on.

Traditional push-pull cell is equivalent as a pair of forward cells in parallel. For push-pull cell I, current only flows through two of the four transformer windings when Q_1 or Q_2 is switched on. In order to reduce transformer volume, push-pull cell II is derived by connecting the anode of D_1 and D_2 with the drain of Q_1 and Q_2, which is shown in Fig. 3. Meanwhile, current flows through both of the transformer windings when Q_1 or Q_2 is switched on.

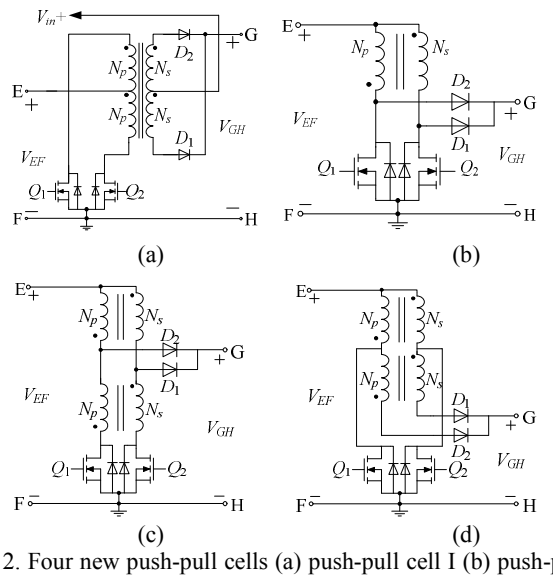


Fig. 2. Four new push-pull cells (a) push-pull cell I (b) push-pull cell II (c) push-pull cell III (d) push-pull cell IV.

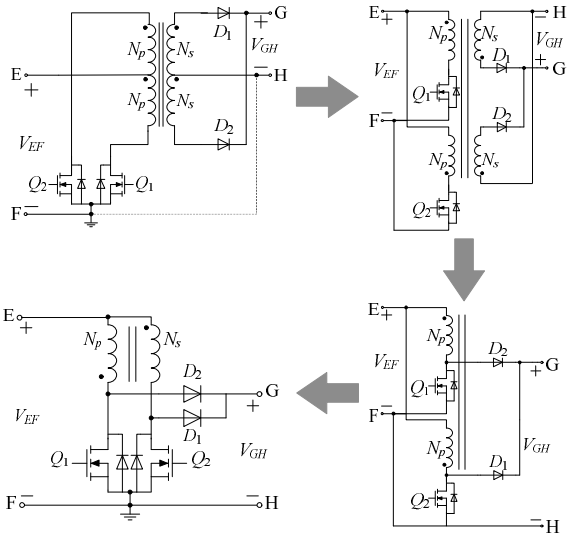


Fig. 3. Derivation of II type push-pull cell.

Push-pull cell III and IV, shown as Fig. 2(c) and Fig.2(d), are derived from push-pull cell II by substituting the four-winding transformer for two-winding transformer to achieve different voltage gain[21]. Unlike push-pull cell I, MOSFETs are connected with primary and secondary windings seperately for push-pull cell II, III, IV. It should be pointed out that the primary and secondary windings are not fixed and the winding which is connected with the switched-on MOSFET is the primary winding.

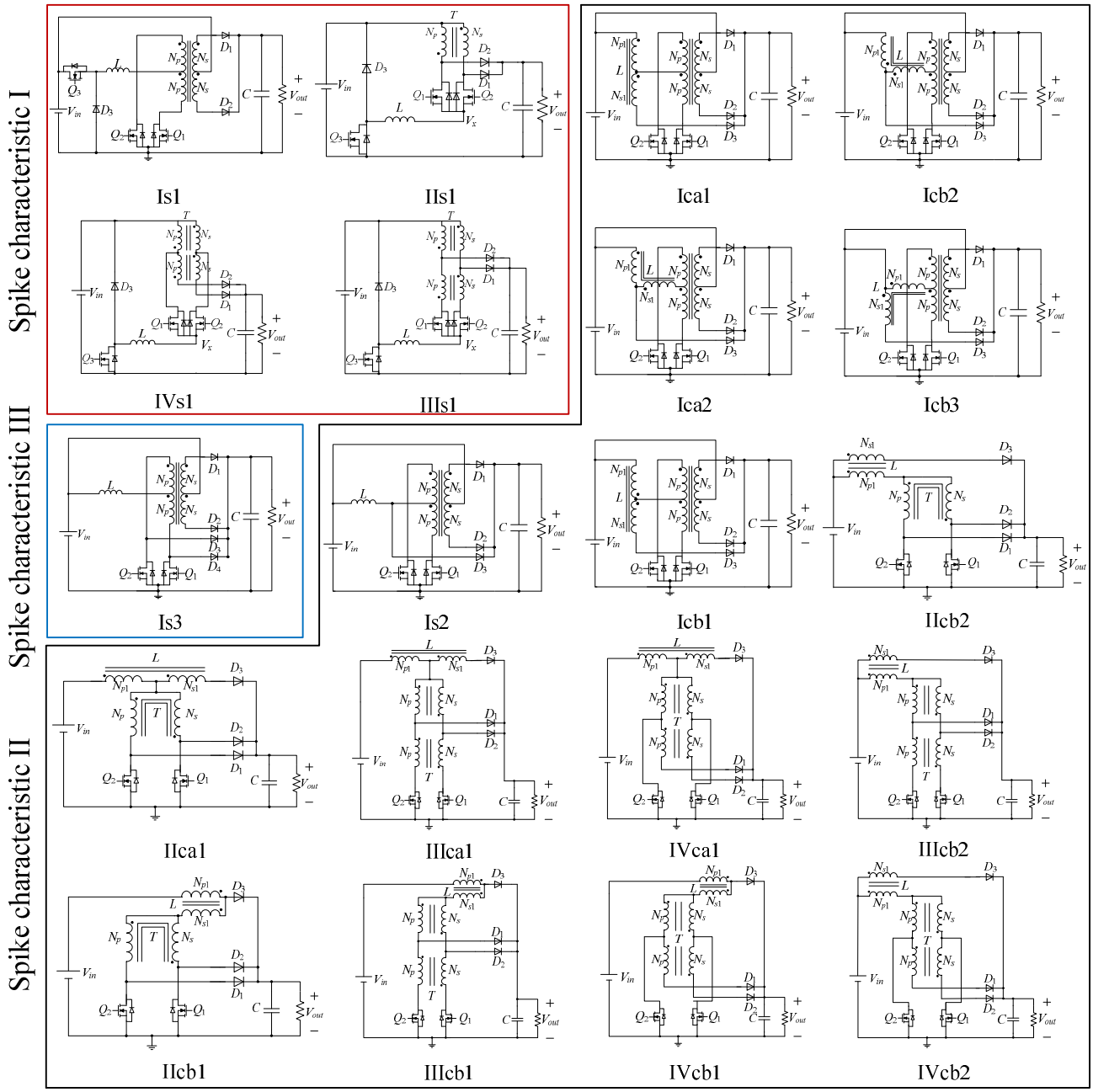


Fig.4. Push-pull based converter with continuous current.

Fig. 4 shows twenty PPCWCCs for BDR which are generated from four kinds of push-pull cells. These topologies are named as the following rules: The first bit means the push-pull cell, four kinds of push-pull cells are named as I, II, III, IV respectively. The second bit expresses the inductor structure, single inductor is named as ‘s’ while coupled inductor is named as ‘c’. The third bit means rank for the topology with single inductor or the connecting way of inductor for the topology with coupled inductor, positive connection is named as ‘a’ while negative connection is named as ‘b’. The fourth bit expresses rank for the topology with coupled inductor. These topologies can be divided into three types according to different spike characteristics:

Spike characteristic I: negative spike exists in low-ripple current. Topologies with this spike characteristic includes Is1, IIs1, IIIs1 and IVs1.

Spike characteristic II: positive spike exists in low-ripple current. Topologies with this spike characteristic includes Ica1, IIca1, IIIca1, IVca1, IIcb1, IIIcb1, IVcb1, Icb3, IIcb2, IIIcb2, IVcb2, Is2, Ica2, Icb1 and Icb2.

Spike characteristic III: both of negative and positive spikes exist in low-ripple current simultaneously. Topology with this spike characteristic includes Is3.

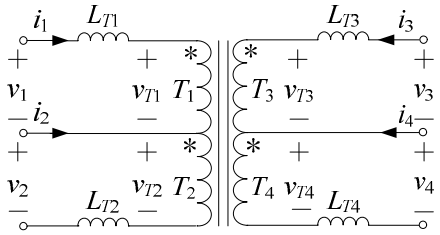


Fig. 5. Positive direction of voltage and current for transformer.

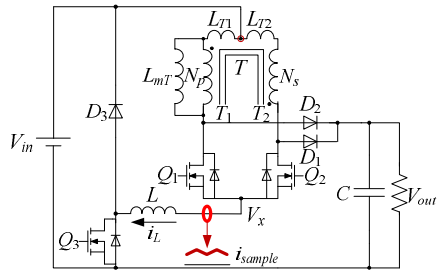


Fig. 6. Topology IIs1 with magnetizing inductance and leakage inductance.

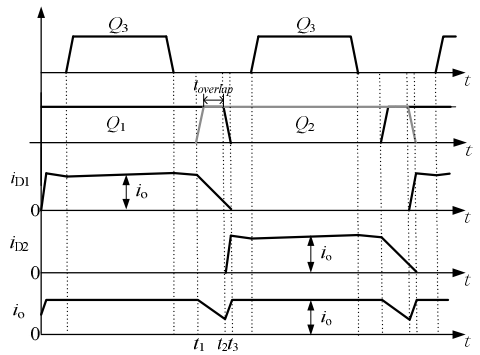


Fig. 7. Current waveform of topology IIs1.

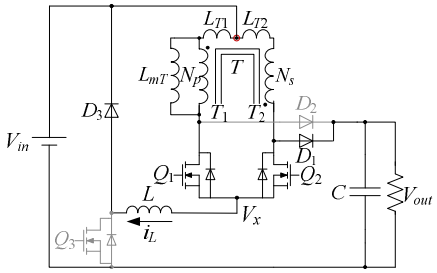
III. Analysis of Current Spike for Three Topologies

Topology IIs1, IIcb2 and Is3 which are on behalf of three spike characteristics are chosen to analyze. The positive direction of voltage and current for transformer, shown as Fig.5, are defined as follows: the electric potential of homonymous-ends and the current flowing into homonymous-ends is positive. Due to the single turn ratio, L_{T1}=L_{T2}=L_{T3}=L_{T4}=L_T, v_{T1}=v_{T2}=v_{T3}=v_{T4}=v_T are satisfied. If the magnetic resistance can be neglected

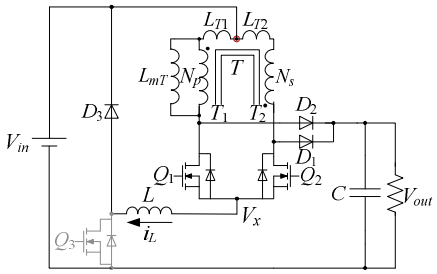
$$N_1 i_1 + N_2 i_2 + N_3 i_3 + N_4 i_4 = 0 \tag{1}$$

A. Topology IIs1

Topology IIs1, shown in Fig.6, is a current fed push-pull based converter. In order to keep the current of inductor flowing regularly, the duty cycle of Q_1 and Q_2 should be a bit higher than 0.5 and the phase difference is 180 degrees. When Q_1 and Q_2 are switched on simultaneously, the output current will reduce dramatically to induce a negative spike. From the current waveform of topology IIs1 in Fig.7, the negative spike transition is separated into two stages (t_1~t_2 stage and t_2~t_3 stage) to analyze.



(a)



(b)

Fig. 8. Equivalent circuit of topology IIs1 during (a) t_1~t_2 stage (b) t_2~t_3 stage.

According to Eq.(1), the primary current and secondary current satisfy

$$i_{Q2} + i_{D1} = i_{Q1} + i_{D2} \tag{2}$$

The current of inductor L is equal to the sum of the current that is flowing through Q_1 and Q_2.

$$i_{Q1} + i_{Q2} = i_L \tag{3}$$

The equivalent circuit during t_1~t_2 stage is shown in Fig.8 (a). Current flows through Q_1 and Q_2 simultaneously, therefore the current flowing through D_1 starts to reduce from t_1 to t_2.

Fig. 8 (b) shows the equivalent circuit during t_2~t_3 stage. Current flows through Q_1, Q_2, D_1 and D_2 simultaneously. At t_3, i_{D1} reduces to zero and i_{D2} reach the steady state.

Considering magnetizing inductance and leakage inductance, the winding voltage of transformer is expressed as

$$\begin{cases} v_1 = v_{LT1} + v_{T1} = v_{out} - v_{in} \\ v_2 = v_{T2} - v_{LT2} = v_{in} - v_{out} \end{cases} \tag{4}$$

Equation (4) is simplified as

$$-0.5L_T \frac{di_{Q1}}{dt} - 0.5L_T \frac{di_{Q2}}{dt} - 0.5L_T \frac{di_{D1}}{dt} = v_{out} - v_{in} \tag{5}$$

During t_1~t_2 stage, the current flowing through D_2 is zero. By differentiating Eq.(2) and (3)

$$\frac{di_{D1}}{dt} = 2\frac{di_{Q1}}{dt} = -2\frac{di_{Q2}}{dt} \tag{6}$$

Substituting Eq.(6) into Eq.(5) yields

$$L_T \frac{di_{D1}}{dt} = -2(v_{out} - v_{in}) \tag{7}$$

The variation of i_{D1} is i_o during t_1~t_3 stage, so the duration

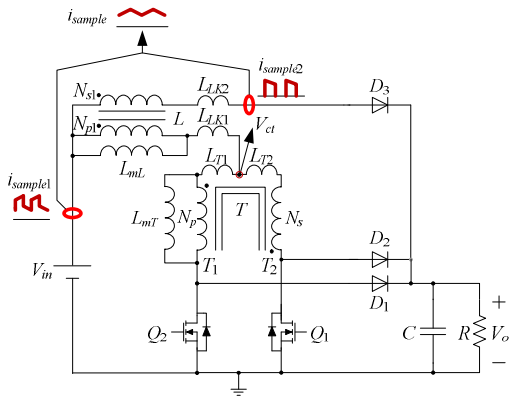


Fig. 9. Topology IIcb2 with magnetizing inductance and leakage inductance.

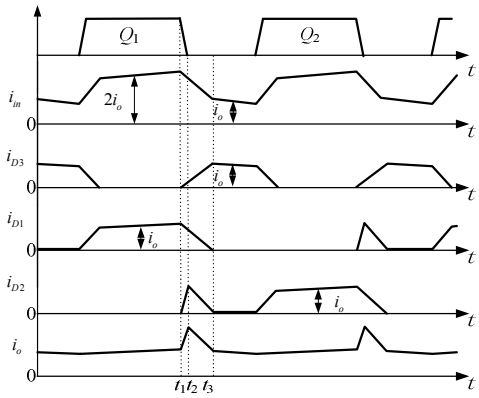


Fig. 10. Current waveform of topology IIcb2.

of negative spike is

$$t_{n-spike} = t_3 - t_1 = \frac{L_T i_o}{2(v_{out} - v_{in})} = t_{off-on} + t_{on-off} + t_{overlap} \quad (8)$$

The output current reduces to the minimum at t_2. Thus the negative spike is

$$i_{n-spike} = i_{D1} + i_{D2} = i_{D1}(t_2) = i_o - 2\frac{v_{out} - v_{in}}{L_T}(t_2 - t_1) \quad (9)$$

In Eq.(9), t_2-t_1 is added by the rise time of MOSFET $t_{\text{off-on}}$ and overlap conduction time t_{overlap}.

Using Eq.(8) in Eq.(9) yields

$$\begin{aligned} i_{n-spike} &= i_{D1} + i_{D2} = i_{D1}(t_2) \\ &= i_o - 2\frac{v_{out} - v_{in}}{L_T}\left(\frac{L_T i_o}{2(v_{out} - v_{in})} - t_{on-off}\right) \end{aligned} \quad (10)$$

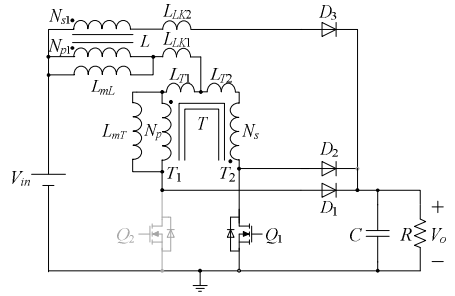
B. Topology IIcb2

Considering the magnetizing inductance and leakage inductance, topology IIcb2 is shown in Fig.9. The magnetizing inductance and leakage inductance of coupled inductor is given in Eq.(11).

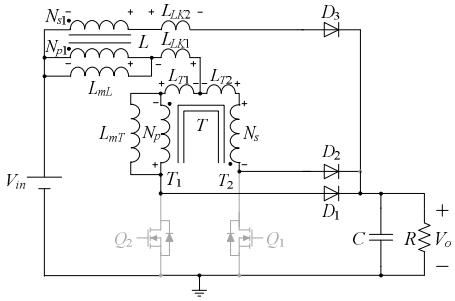
$$\begin{cases} L_{LK1} = \dfrac{N_1 \Phi_{11}(1-k_1)}{i_1} = L_1(1-k_1) \\ L_{LK2} = \dfrac{N_2 \Phi_{22}(1-k_2)}{i_2} = L_2(1-k_2) \end{cases} \quad (11)$$

L_1 and L_2 are the self inductance of primary and secondary winding respectively. The closer the coupling coefficient $\sqrt{k_1 \cdot k_2}$ is to single, the smaller the leakage of coupled inductor L_{LK} will be. Suppose that the turn ratio of coupled inductor and transformer is N_1=N_{p1}/N_{s1} and N_2=N_p/N_s separately, N_2=2N_1=1 should be satisfied to realize low-ripple output current.

Fig.10 shows the current waveform of topology IIcb2. The positive spike exists during the transition that MOSFET is switched off. The positive spike transition is separated into two stages (t_1~t_2 stage and t_2~t_3 stage) to analyze.



(a)



(b)

Fig. 11. Equivalent circuit of topology IIcb2 during (a) t_1~t_2 stage (b) t_2~t_3 stage.

Based on Eq.(1)

$$i_{Q2} + i_{D1} = i_{Q1} + i_{D2} \quad (12)$$

For topology IIcb2, the sum of input current and diode current i_{D3} is twice of output current, therefore

$$2i_{D3} + i_{D1} + i_{D2} + i_{Q1} + i_{Q2} = 2i_o \quad (13)$$

The equivalent circuit during t_1~t_2 stage is shown in Fig.11(a). As Q_1 is switched off, the current flowing through Q_1 and D_1 reduce from i_o and the current flowing through D_3 and D_2 rise from 0. At t_2, the output current is at its maximum.

Fig.11(b) shows the equivalent circuit of t_2~t_3 stage. During this stage, i_{D3}, i_{D1} and i_{D2} reach stable states at t_3. Meanwhile, D_1 and D_2 are already switched off and the current of diode D_3 is i_o.

The leakage inductance voltage of transformer is

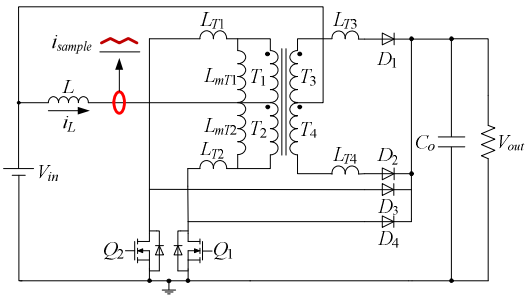


Fig. 12. Topology Is3 with magnetizing inductance and leakage inductance.

$$v_{LT1} = v_{LT2} = v_{LT} = -L_T \frac{di_{D1}}{dt} \tag{14}$$

The turn ratio of coupled inductor is 0.5, therefore the secondary leakage inductance is quadruple of the primary leakage inductance, that is L_{LK2}=4L_{LK1}=4L_{LK}. The leakage inductance voltage of coupled inductor is

$$v_{LK2} = 2v_{LK1} = 2v_{LK} = -2L_{LK1} \frac{d(i_{D1} + i_{D2})}{dt} \tag{15}$$

Equation (16) is derived by compiling the voltage loop equation.

$$v_{in} + v_{N_{p1}} + v_{LK1} + v_{LT1} + v_{N_p} = v_{out} \tag{16}$$

Substitute Eq.(14) and (15) to (16) yields

$$-4L_{LK} \frac{di_{D1}}{dt} - 4L_{LK} \frac{di_{D2}}{dt} - 2L_T \frac{di_{D1}}{dt} = v_{out} - v_{in} \tag{17}$$

During t_2~t_3 stage, the current of Q_1 and Q_2 is equal to zero. According to Eq.(12) and (13)

$$\frac{di_{D1}}{dt} = \frac{di_{D2}}{dt} = -\frac{di_{D3}}{dt} \tag{18}$$

Comparing Eq.(18) and Eq.(17) yields

$$(8L_{LK} + 2L_T) \frac{di_{D3}}{dt} = v_{out} - v_{in} \tag{19}$$

During t_1~t_3 stage, the variation of i_{D3} is i_o, so the duration of positive spike is

$$t_{p-spike} = t_3 - t_1 = \frac{i_o(8L_{LK} + 2L_T)}{v_{out} - v_{in}} \tag{20}$$

The positive spike is

$$\begin{aligned} i_{p-spike} &= i_{D1} + i_{D2} + i_{D3} = 2i_o - i_{D3}(t_2) \\ &= 2i_o - \frac{v_{out} - v_{in}}{8L_{LK} + 2L_T}(t_2 - t_1) \end{aligned} \tag{21}$$

In Eq.(21), t_2-t_1 is equal to the fall time of MOSFET $t_{\text{on-off}}$.

C. Topology Is3

Fig.12 shows topology Is3 with magnetizing inductance and leakage inductance. When the turn ratio of transformer is single, the output current is low-ripple. The positive spike exists during switch-off transition while the negative spike exists during switch-on transition, which is shown in Fig. 13.

According to Eq.(1)

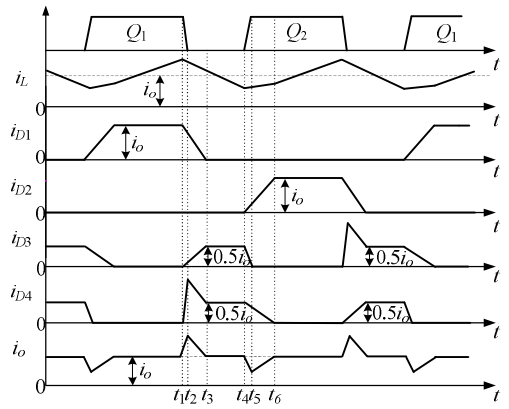


Fig. 13. Current waveform of topology Is3.

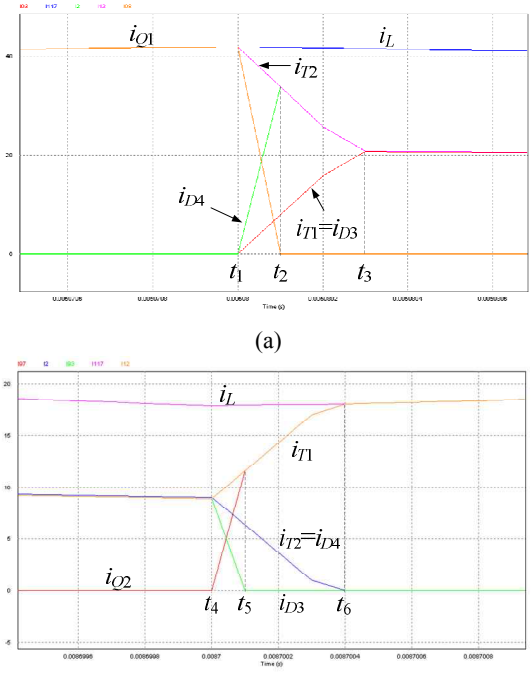


Fig. 14. Current waveform of topology Is3 during (a) switch-off transition (b) switch-on transition.

$$-i_{D1} + i_{D2} - i_{D3} + i_{D4} + i_{Q1} - i_{Q2} = 0 \tag{22}$$

$$i_{D3} + i_{Q2} + i_{D4} + i_{Q1} = i_L \tag{23}$$

The current waveform during switch-off transition is shown in Fig.14(a). The positive spike which exists during this transition is separated into two stages (t_1~t_2 stage and t_2~t_3 stage) to analyze.

Equivalent circuit during t_1~t_2 stage is shown in Fig.15(a). For the reason that the right side potential of inductor is higher than the left one, the anode potential of D_3 and D_4 is higher than that of D_1 and D_2. Therefore the inductor current flows through T_1 and T_2 windings rather than T_3 and T_4 windings. As Q_1 switched off, the current flowing through T_2 starts to fall while the current flowing through T_1 starts to rise from 0. Both of them reach steady state when they are 0.5i_L. At this moment, the current flowing through Q_1 has already

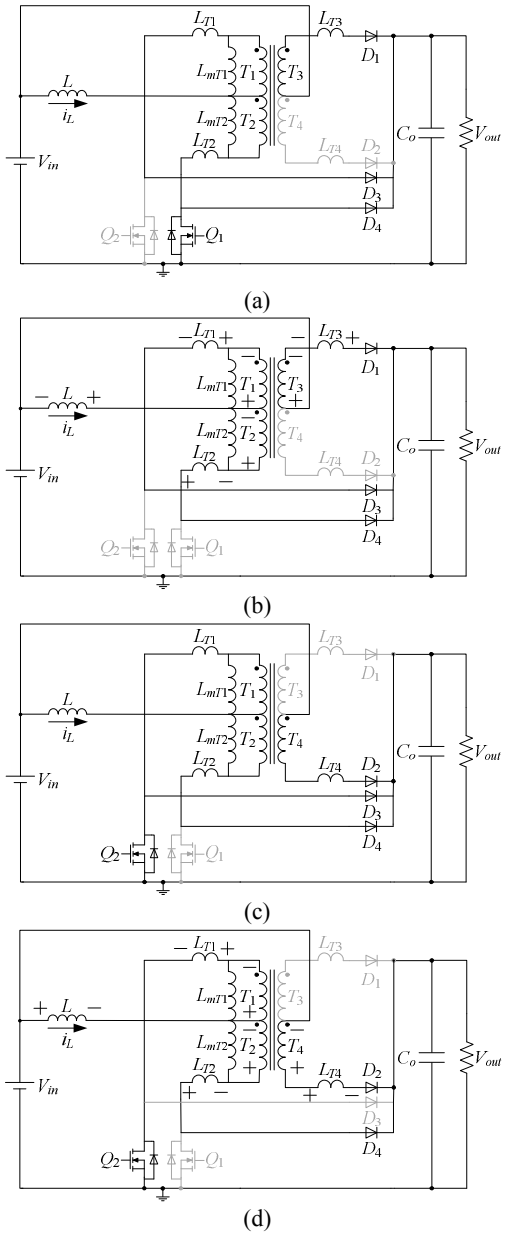


Fig.15 Equivalent circuit of topology Is3 during (a) t_1~t_2 stage (b) t_2~t_3 stage (c) t_4~t_5 stage (d) t_5~t_6 stage.

fallen to 0 and i_{T2}=i_{D4} is satisfied. Compared with the time that i_{T1} and i_{T2} reach steady state, the fall time of Q_1 is much shorter. At t_2, Q_1 has already turned off but i_{T1} and i_{T2} haven't reach steady state. Thus i_{D4}>i_{D3} is satisfied and output current is the maximum at this moment.

During t_2~t_3 stage, i_{D3} is rising. In contrast, i_{D4} and i_{D1} are falling. All of them don't reach steady state until t_3. At this moment, D_1 is switched off and both of i_{D3} and i_{D4} are equal to 0.5i_o. Equivalent circuit of this stage is shown in Fig.15(b).

Considering magnetizing inductance and leakage inductance, the winding voltage of transformer is given as

$$\begin{cases} v_1 = -v_{LT1} - v_{T1} = v_{out} - v_{L+} \\ v_2 = -v_{LT2} - v_{T2} = v_{L+} - v_{out} \\ v_3 = v_{LT3} - v_{T3} = v_{out} - v_{in} \end{cases} \quad (24)$$

Equation (24) is simplified as

$$-2L_T \frac{di_{D1}}{dt} + L_T \frac{di_{D3}}{dt} - L_T \frac{di_{D4}}{dt} = 2(v_{out} - v_{in}) \quad (25)$$

During this stage, i_{Q1}=i_{Q2}=i_{D2}=0. Equation (26) is simplified from Eq.(22) and Eq.(23)

$$\frac{di_{D1}}{dt} = 2\frac{di_{D4}}{dt} = -2\frac{di_{D3}}{dt} \quad (26)$$

From Eq.(25) and Eq.(26)

$$6L_T \frac{di_{D3}}{dt} = 2(v_{out} - v_{in}) \quad (27)$$

During t_1~t_3 stage, the variation of i_{D3} is 0.5i_o, so the duration of positive spike is

$$t_{p-spike} = t_3 - t_1 = \frac{3L_T i_o}{2(v_{out} - v_{in})} \quad (28)$$

The positive spike is at its maximum at t_2.

$$i_{p-spike} = i_{D1} + i_{D3} + i_{D4} = 2i_o - 2\frac{v_{out} - v_{in}}{3L_T}(t_2 - t_1) \quad (29)$$

In Eq.(29), t_2-t_1 is equal to the fall time of MOSFET $t_{\text{on-off}}$.

The current waveform during switch-on transition is shown in Fig.14(b). The negative spike during this transition is separated into two stages (t_4~t_5 stage and t_5~t_6 stage) to analyze.

Equivalent circuit during t_4~t_5 stage is shown in Fig.15(c). As Q_2 is switched on, the current flowing through T_1 starts to rise from 0.5i_L to i_L while the current flowing through T_2 starts to fall from 0.5i_L to 0, the absolute value of di_{T1}/dt and di_{T2}/dt are equal. Since the slope of i_{Q2} is higher than that of i_{T1} and i_{D3}=i_{T1}-i_{Q2} is satisfied, the absolute value of di_{D3}/dt is higher than that of di_{T1}/dt. Meanwhile, the slope of i_{T2} is equal to that of i_{D4}, so |di_{D3}/dt|>|di_{D4}/dt| is satisfied. That's why i_{D3} falls faster than i_{D4}. At t_5, i_{D3} has already fallen to 0 and output current is at its minimum.

During t_5~t_6 stage, i_{D2} is rising. In contrast, i_{D4} is falling. All of them won't reach steady state until t_6. At this moment, D_4 is switched off and i_{D2} is equal to i_o. Equivalent circuit of this stage is shown in Fig.15(d).

The winding voltage of transformer is

$$\begin{cases} v_1 = -v_{LT1} - v_{T1} = 0 - v_{L-} \\ v_2 = -v_{LT2} - v_{T2} = v_{L-} - v_{out} \\ v_4 = v_{LT4} - v_{T4} = v_{in} - v_{out} \end{cases} \quad (30)$$

Equation (30) is simplified as

$$2L_T \frac{di_{D2}}{dt} + L_T \frac{di_{Q2}}{dt} - L_T \frac{di_{D4}}{dt} = 2v_{in} - v_{out} \quad (31)$$

During this stage, i_{Q1}=i_{D1}=i_{D3}=0. Equation (32) is derived from Eq.(22) and Eq.(23)

TABLE I
MAGNITUDE AND DURATION OF CURRENT SPIKE FOR THREE TOPOLOGIES

	Positive spike		Negative spike	
	Magnitude i_{mp}	Duration $t_{p\text{-}spike}$	Magnitude i_{mn}	Duration $t_{n\text{-}spike}$
Topology IIs1	0	0	$i_o-\frac{2(v_{out}-v_{in})t_{on-off}}{L_T}$	$\frac{L_T i_o}{2(v_{out}-v_{in})}$
Topology IIcb2	$i_o-\frac{v_{out}-v_{in}}{8L_{LK}+2L_T}t_{on-off}$	$\frac{i_o(8L_{LK}+2L_T)}{v_{out}-v_{in}}$	0	0
Topology Is3	$i_o-2\frac{v_{out}-v_{in}}{3L_T}t_{on-off}$	$\frac{3L_T i_o}{2(v_{out}-v_{in})}$	$0.5i_o-\frac{v_{in}-0.5v_{out}}{3L_T}t_{off-on}$	$\frac{3L_T i_o}{2v_{in}-v_{out}}$

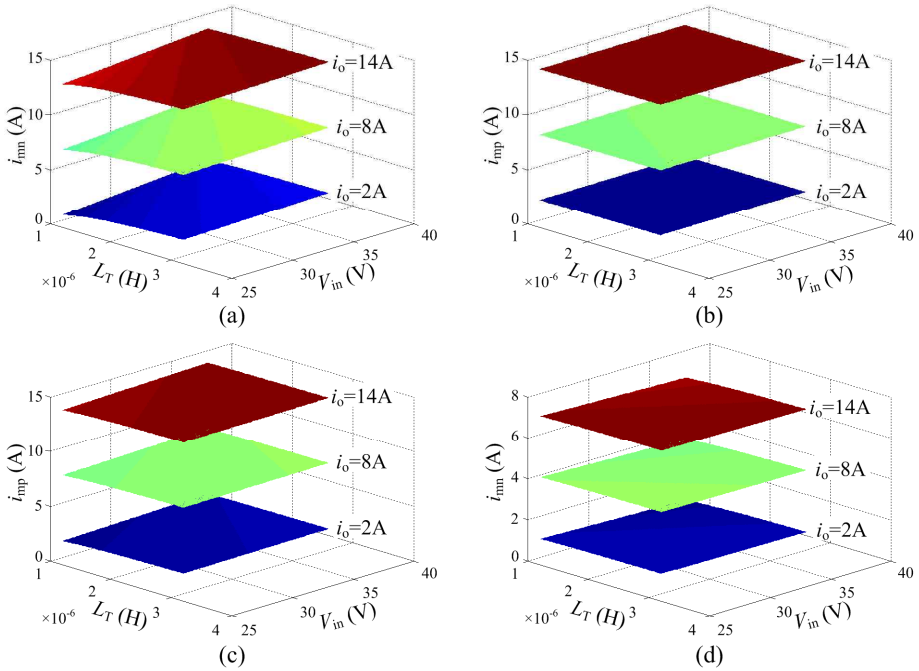


Fig. 16. Variation of spike magnitude by varying leakage inductance, input voltage and output current without spike for (a) negative spike of topology IIs1 (b) positive spike of topology IIcb2 (c) positive spike of topology Is3 and (d) negative spike of topology Is3.

$$\frac{di_{D2}}{dt}=2\frac{di_{Q2}}{dt}=-2\frac{di_{D4}}{dt} \tag{32}$$

Substitute Eq.(32) to Eq.(31) yields

$$-6L_T\frac{di_{D4}}{dt}=2v_{in}-v_{out} \tag{33}$$

The variation of i_{D4} is -0.5i_o during t_4~t_6 stage, so the duration of negative spike is

$$t_{n-spike}=t_6-t_4=\frac{3L_T i_o}{2v_{in}-v_{out}} \tag{34}$$

The negative spike is at its minimum at t_5.

$$i_{n-spike}=i_{D2}+i_{D4}=0.5i_o+\frac{v_{in}-0.5v_{out}}{3L_T}(t_5-t_4) \tag{35}$$

In Eq.(35), t_5-t_4 is equal to the rise time of MOSFET $t_{off\text{-}on}$.

IV. FACTORS ON CURRENT SPIKE

The magnitude of positive spike is

$$i_{mp}=i_{p-spike}-i_o \tag{36}$$

The magnitude of negative spike is

$$i_{mn}=i_o-i_{n-spike} \tag{37}$$

Supposing that exciting current and ripple of inductor current can be neglected, magnitude and duration of three topologies are listed in Table I. All of the analysis is based on BDR in a 42V PCU system. The specifications of PCU are shown as following.

- Input voltage: V_{in}=26V~38V;
- Output voltage: V_{out}=42V;
- Output current: i_{out}=2A~14A;
- Equivalent switch frequency: f_{eq}=20kHz

It is concluded from Table I that the magnitude and duration of spike are relevant to i_o, v_{in} and L_T (L_{LK}). Let it be supposed that L_{LK}=0.5uH. Fig.16 shows the variation of spike magnitude by varying leakage inductance (1uH~3uH), input voltage (26V~38V) and output current without spike (2A, 8A, 14A). Fig.17 shows the variation of spike duration by the

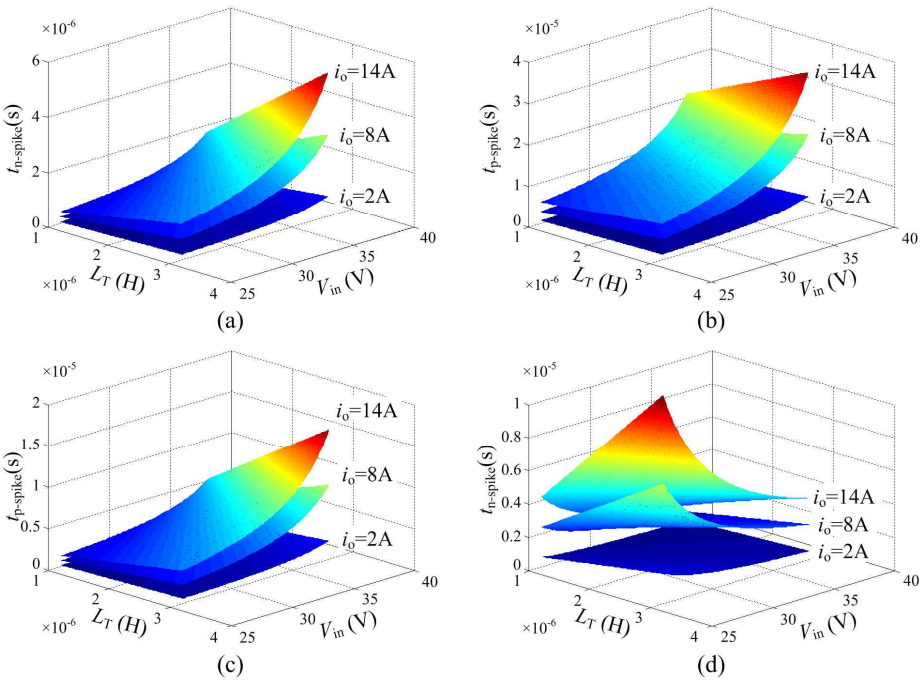


Fig. 17. Variation of spike duration by varying leakage inductance, input voltage and output current without spike for (a) negative spike of topology IIs1 (b) positive spike of topology IIcb2 (c) positive spike of topology Is3 and (d) negative spike of topology Is3.

same variation range of leakage inductance, input voltage and output current without spike.

We can conclude from Table I that the magnitude and duration of negative spike for topology IIs1 and that of positive spike for topology IIcb2 and Is3 follow the same trend as i_o, v_n and L_T change, which is embodied in Fig.16 and Fig. 17. For topology Is3, the magnitude and duration of negative spike increase as i_o and L_T increase, but fall as v_{in} increases. Among three topologies, the magnitude of negative spike for topology Is3 is almost half of the others and the spike duration of topology IIcb2 is the longest.

In a regulated-bus PCU system, v_{in} and i_o are dependent on time-varying payload power. Thus it is only possible to limit the leakage inductance to decrease the magnitude and duration of spike with time-varying load.

V. Equivalent Current Sampling Method

The output current of BDR is sampled for current sharing and parameter telemetry. But spike exists in output current, which disturbs the measurement of output current [18]. To overcome this problem, ECSM is adopted.

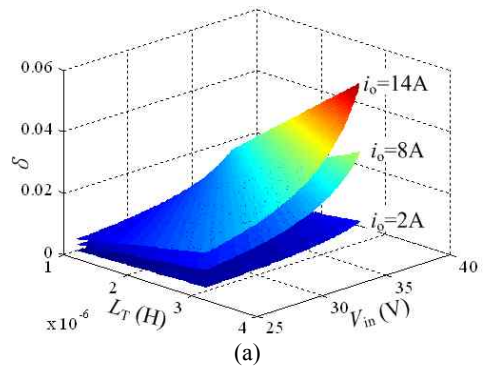
By ignoring the effect of current spike, the inductor current of topology IIs1 and Is3 are equivalent as the output current without spike, which are shown in Fig.6 and Fig.12. As is shown in Fig.9, the sum of primary current and secondary current of coupled inductor is twice of the output current without spike as to topology IIcb2. Hence the equivalent current can be sampled instead of output current. That's why we call it ECSM.

ECSM is suitable for PPCWCCs. For PPCWCCs with single inductor, the current of single inductor is equivalent as the output current without spike [21]. For PPCWCCs generated from push-pull cell II with coupled inductor, the input current and secondary current of coupled inductor can be added to substitute for output current [18]. If ECSM is adopted, the sampled current doesn't need to be filtered, which eliminates the sampling time delay and achieves excellent dynamic performance. However ECSM reduces the sampling accuracy and telemetry accuracy because of neglecting the spike.

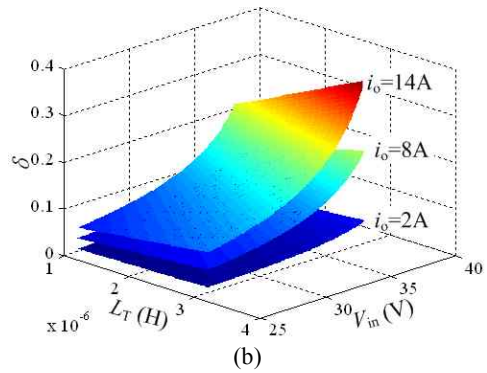
VI. Problem of Equivalent Current Sampling Method

It should be noted that the average value of equivalent current is more or less than that of output current due to the exclusion of spike. In order to achieve excellent current sharing performance, the equivalent current is sampled for inner current loop. For the reason that the reference of each inner loop is the same, the error which is introduced by ECSM will not affect current sharing performance. However, this error affects the telemetry accuracy directly. Parameter telemetry is beneficial to monitor the operation status of BDR in real time. So it is necessary to analyze the error in quality and quantity. According to analysis results, the telemetry value can be compensated to improve the accuracy.

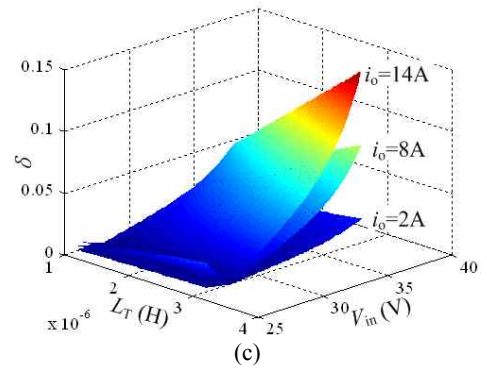
The average value of positive and negative spike is shown as Eq.(38) and (39) respectively.



(a)



(b)



(c)

Fig. 18. Variation of current sampling error rate by varying leakage inductance, input voltage and output current without spike for (a) topology IIs1 (b) topology IIcb2 (c) topology Is3.

$$S_{p-spike} = i_{mp} \times t_{p-spike} \times f_{eq} \times 0.5 \quad (38)$$

$$S_{n-spike} = i_{mn} \times t_{n-spike} \times f_{eq} \times 0.5 \quad (39)$$

The ECS error rate is

$$\delta = \frac{\left| S_{p-spike} - S_{n-spike} \right|}{i_{out}} \times 100\% \quad (40)$$

Where i_{out} is the average value of output current.

Fig. 18 shows the variation of current sampling error rate δ by varying leakage inductance (1uH~3uH), input voltage (26V~38V) and output current without spike (2A, 8A, 14A). It is concluded from Fig.18 that δ of topology IIs1 and IIcb2 increases as i_o, v_{in} and L_T increase. Similarly, δ of topology Is3 increases as i_o and L_T increase, nevertheless, it initially

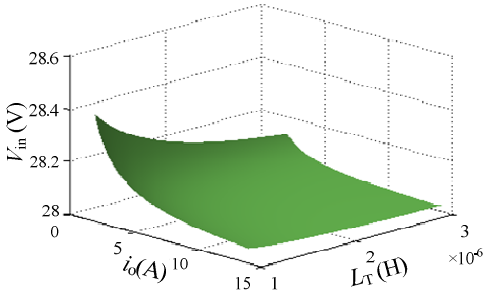


Fig. 19. Relationship among leakage inductance, input voltage and output current without spike when current sampling error rate is equal to 0 for topology Is3.

decreases and then increases as v_{in} increases. This is because that there is a series of i_o, L_T and v_{in} to satisfy $S_{p\text{-}spike}$=$S_{n\text{-}spike}$ without error. The relationship among i_o, L_T and v_{in} when δ=0 is shown in Fig.19. δ=0 won't be satisfied unless V_{in}=28V~28.4V. Among three topologies, δ for topology IIs1 is the lowest and δ for topology IIcb2 is the highest. Even if δ for topology Is3 is equal to 0 under given i_o, L_T and v_{in}, it increases quickly as i_o, L_T and v_{in} increase.

VII. Experimental Results

Three experimental prototypes are designed for experimental verification. Component values and operating conditions used for experimental tests are summarized in Table II.

The waveform of equivalent current and output current for the specific V_{in}=32V, I_{out}=7A condition, corresponding to the results in Table III, are shown in Fig.20. The error between theoretical analysis and experimental results exists, for the reason that current ripple and exciting current are neglected in theoretical analysis. In total, the experimental result is coincide with the theoretical analysis.

From the experimental waveform in Fig.20, the equivalent current i_{sample} is approximately equal to the output current without spike for topology IIs1 and Is3 or twice of the output current without spike for topology IIcb2. Therefore, i_{sample} can be easily sampled.

The ECS error rate is obtained from Eq.(41) by measuring output current i_{out} and equivalent current i_{sample}.

$$\delta = \frac{\left| i_{out} - i_{sample} \right|}{i_{out}} \times 100\% \quad (41)$$

Fig. 21 presents the calculated and measured results for input voltage v_{in} vs. the ECS error rate. Table I, Eq.(38) and (39) are derived based on the premise that the exciting current and ripple of output current are neglected. In addition, the error is existed in current measuring. That's why the measured results are out of calculated results by 1% to 2.5%. Overall, the validity of theoretical analysis is proven by measured results.

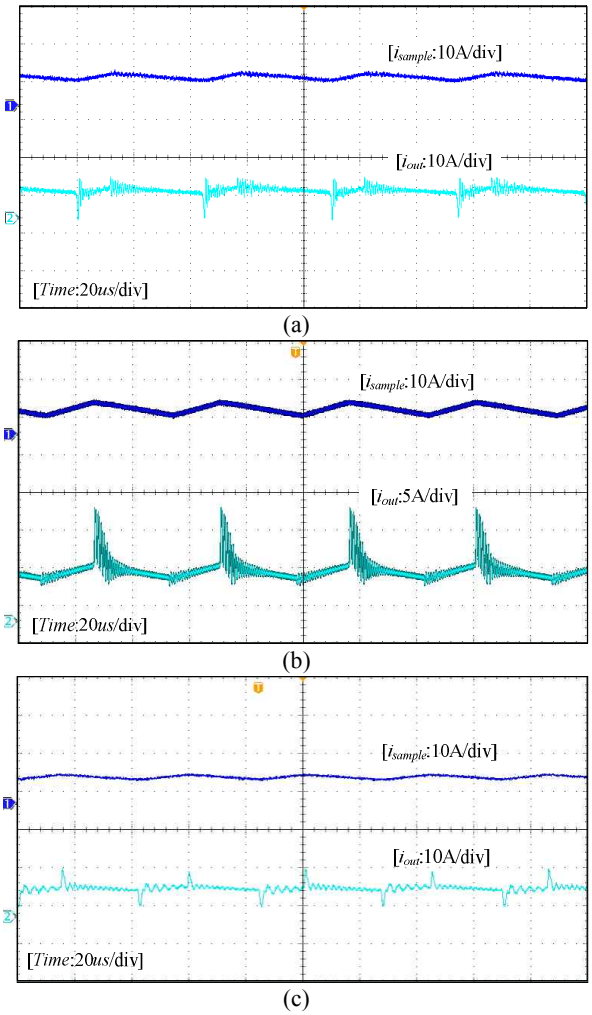


Fig. 20. Equivalent current and output current for (a) Topology IIs1 (b) Topology IIcb2 (c) Topology Is3.

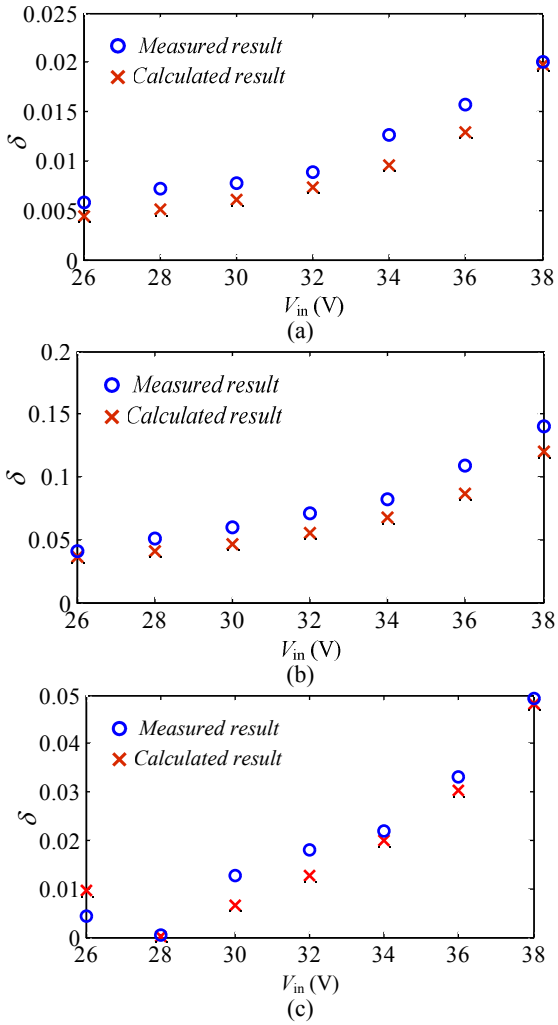


Fig. 21. Calculated and measured results of current sampling error rate for (a) topology IIs1 (b) topology IIcb2 (c) topology Is3 when L_T=2uH, I_{out}=7A.

TABLE II
COMPONENT VALUES AND OPERATING CONDITIONS FOR THREE TOPOLOGIES

	Topology IIs1	Topology IIcb2	Topology Is3
MOSFET	IRF3710 ($t_{off\text{-}on}$=58ns, $t_{on\text{-}off}$=47ns)		
Frequency	f_{Q1}=f_{Q2}=11.2 kHz, f_{Q3}=22.4 kHz	f_{Q1}=f_{Q2}=11.15 kHz	f_{Q1}=f_{Q2}= 11.57kHz
Single inductor	200.15uH	/	233.02uH
Coupling inductor	/	L_{p1}=44.02uH, L_{s1}=172.15uH, M=85.9uH	/
Transformer	L_m=465.11uH, L_{T1}=2.01uH, L_{T2}=1.97uH	L_m=458.5uH, L_{T1}=2.04uH, L_{T2}=1.98uH	L_m=389.26uH, L_{T1}=2.01uH, L_{T2}=1.95uH, L_{T3}=1.99uH, L_{T4}=1.98uH

TABLE III
THEORETICAL AND EXPERIMENTAL RESULTS FOR THREE TOPOLOGIES WHEN V_{IN}=32V AND I_O=7A

V_{in}=32V I_o=7A	Topology IIs1		Topology IIcb2		Topology Is3	
	theoretical	practical	theoretical	practical	theoretical	practical
i_{mp} (A)	/	/	6.55	7.7	6.75	5.97
i_{mn} (A)	6.58	6.4	/	/	3.3	3.98
$t_{p\text{-}spike}$ (us)	/	/	5.3	5.2	2.07	2.4
$t_{n\text{-}spike}$ (us)	0.71	0.96	/	/	1.88	1.92
i_{sample} (A)	7.052	7.05	13.23	13.02	6.91	6.87
i_{out} (A)	7	6.99	7	6.99	7	6.99

TABLE IV
THE CHANGE TREND OF CURRENT SAMPLING ERROR RATE VS. I_O, V_{IN} AND L_T FOR THREE TOPOLOGIES

		i_{mp}	$t_{p\text{-}spike}$	i_{mn}	$t_{n\text{-}spike}$	$S_{p\text{-}spike}$	$S_{n\text{-}spike}$	δ
Topology IIs1	i_o↑	/	/	↑	↑	/	↑	↑
	v_{in}↑	/	/	↑	↑	/	↑	↑
	L_T↑	/	/	↑	↑	/	↑	↑
Topology IIcb2	i_o↑	↑	↑	/	/	↑	/	↑
	v_{in}↑	↑	↑	/	/	↑	/	↑
	L_T↑	↑	↑	/	/	↑	/	↑
Topology Is3	i_o↑	↑	↑	↑	↑	↑	↑	↑
	v_{in}↑	↑	↑	↓	↓	↑	↓	initially↓then↑
	L_T↑	↑	↑	↑	↑	↑	↑	↑

VIII. CONCLUSIONS

PPCWCC which is superior to traditional push pull converter is competitive in aerospace applications. Whereas the problem that spike exists in the low-ripple current is introduced. Considering different current spike characteristics, PPCWCCs which are suitable for BDR are divided into three types, among which the leakage inductance effects are analyzed through topology IIs1, IIcb2 and Is3. ECSM is adopted to overcome the spike disturbance, but introduces current sampling error. This paper analyzes the error in quality and quantity. According to analysis results, the telemetry value can be compensated to improve the accuracy. The conclusions are drawn as follows:

① Positive spike exists in topology IIcb2 and Is3 while negative spike exists in topology IIs1 and Is3.

② ECSM which is appropriate for PPCWCCs can be summarized as the following rules: For PPCWCCs with single inductor, the current of single inductor is equivalent as the output current without spike. For PPCWCCs generated from push-pull cell II with coupled inductor, the input current and secondary current of coupled inductor can be added to substitute for output current.

③ The output current of BDR is sampled for current sharing and parameter telemetry. ECS error rate δ won't affect current sharing performance. Instead, telemetry accuracy is affected directly.

④ Table IV presents the trend of ECS error rate δ vs. i_o, v_{in} and L_T for three topologies. δ of topology IIs1 and IIcb2 increases with the increase of i_o, L_T and v_{in}. δ of topology Is3 has the same tendency as i_o and L_T increase, nevertheless, it initially decreases and then increases as v_{in} increases. When V_{in}=28V~28.4V is accomplished, there is always a series of i_o, L_T and v_{in} to satisfy $S_{p\text{-}spike}$=$S_{n\text{-}spike}$ without current sampling error.

⑤ In view of δ, topology IIcb2 is the most seriously affected by leakage inductor while topology IIs1 is the most slightly affected. Even if δ of topology Is3 is equal to 0 under given i_o, L_T and v_{in}, then it increases quickly as i_o, L_T and v_{in} increase.

⑥ The difference between measured results and calculated results exists for the reason that the calculated results neglect the exciting current and ripple of output current.

⑦ PPCWCC for BDR isn't suitable for the application that requires precisely controlled output current.

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REFERENCES

[1] N. Nicolas, L. Didier, A. Peter, etal. "A new modular and flexible power system for LEO missions," in *Proceeding of 9th European Space Power Conference*, 2011.

[2] P. Morsaniga, G. Gervasio, and G. Cuzzocrea, "Bepicolombo electrical power system," in *Proceeding of 9th European Space Power Conference*, 2011.

[3] O. Dan, "Lessons learnt in-flight-the STRV micro-satellite power system," in *Proceeding of 4th European Space Power Conference*, 1995.

[4] M. M. Hansen, "Power conditioning unit for bepicolombo transfer module," in *Proceeding of 8th European Space Power Conference*, 2008.

[5] H. Jensen and J. Laursen, "Power conditioning unit for Rosetta/Mars express," in *Proceeding of 6th European Space Power Conference*, pp. 249-256, 2002.

[6] J. P. Castiaux, E. Lecomte, and J. M. Labille, "Modular high power conditioning unit," in *Proceeding of 5th European Space Power Conference*, pp. 99-104, 1998.

[7] A. Garrigos, J. A. Carrasco, J. M. Blanes, and E. Sanchis-Kilders, "A power conditioning unit for high power GEO satellites based on the sequential switching shunt series regulator," in *Proceeding of MELECON*, pp. 1186-1189, 2006.

[8] C. S. Clark, A. H. Weinberg, and K. W. Hall, "The design and performance of a power system for the galileo system test bed (GSTB-V2/A)," in *Proceeding of 7th European*

Space Power Conference, pp.155-162, 2005.
[9] K. H. Park, C. H. Kim, and H. K. Cho. "Design considerations of a lithium ion battery management system (bms) for the STSAT-3 satellite," *Journal of Power Electronics*, Vol. 10, No. 2, pp. 210-217, Mar. 2010.
[10] D. H. Jang and S. K. Han. "Low cost high power density photovoltaic power conditioning system with an energy storage system," *Journal of Power Electronics*, Vol. 12, No. 3, pp. 487-494, May. 2012.
[11] M. S. Ali, H. S. Bae, and S. J. Lee. "Regulated peak power tracking (RPPT) System using parallel converter topologies," *Journal of Power Electronics*, Vol. 11, No. 6, pp. 870-879, Nov. 2011.
[12] D. O'Sullivan, "Space power electronics-design drivers," *ESA Journal*, Vol. 18, No. 1, pp.1-23, 1994.
[13] D. Wolfgang and D. Willi, "Generic 100V/high power bus conditioning," in *Proceeding of 7th European Space Power Conference*, 2005.
[14] L. Soubrier and E. Trehet, "High power PCU for alphabus: PSR100V," in *Proceeding of. 9th European Space Power Conference*, 2011.
[15] L. Soubrier, P. Besdel, T. Daubresse, and E. Trehet, "High performance BDR for the PCU of alphabus," in *Proceeding of 8th European Space Power Conference*, 2008.
[16] E. Sanchis-Kilders, E. Maset, and A. H. Weinberg, "ion drive propulsion MPP power conditioning system without battery," in *Proceeding of 8th European Space Power Conference*, 2008.
[17] E. Maset and A. Ferrers, "5kW Weinberg converter for battery discharging in high-power communications satellites," in *Proceeding of IEEE PESC Conference*, pp. 69-75, 2005.
[18] A. H. Weinberg and P. Rueda Boldo, "A high power, high frequency, DC to DC converter for space applications," in *Proceeding of IEEE PESC Conference*, pp. 1140-1147, 1992.
[19] Q. Chen, T. Q. Zheng, and Y. Li, "Derivation and characterization of single-inductor push-pull based topology with continuous current," *Proceedings of the CSEE*, to be published.
[20] Qian Chen, T. Q. Zheng, and Y. LI, "Continuous current push-pull based topology with coupling inductor used in spacecraft," *Transactions of china electrotechnical society*, to be published.
[21] J. Aroca, D. Olsson, and J. Maicas, "An efficient BDR topology, able to handle a large battery voltage range," in *Proceedings of 5th European Space Power Conference*. pp. 33-38, 1999.

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