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New Isolated Single-Phase AC-DC Converter for Universal Input Voltage

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Abstract

This paper investigates a new isolated single-phase AC-DC converter, which integrates a modified AC-DC buck-boost converter with a DC-DC forward converter. The front semi-stage is operated in discontinuous conduction mode (DCM) to achieve an almost unity power factor and a low total harmonic distortion of the input current. The rear semi-stage is used for step-down voltage conversion and electrical isolation. The front semi-stage uses a coupled inductor with the same winding-turn in the primary and secondary sides, which is charged in series during the switch-on period and is discharged in parallel during the switch-off period. The discharging time can be shortened. In other words, the duty ratio can be extended. This semi-stage can be operated in a larger duty-ratio range than the conventional AC-DC buck-boost converter for DCM operation. Therefore, the proposed converter is suitable for universal input voltage (90~264 V_{rms}) and a wide output-power range. Moreover, the voltage stress on the DC-link capacitor is low. Finally, a prototype circuit is implemented to verify the performance of the proposed converter.

Key words: Power factor correction, Discontinuous conduction mode, Universal input voltage

I. INTRODUCTION

Since DC power sources are widely used in many applications, including DC power supplies, battery chargers, and lighting systems, AC-DC power conversion plays an important role. Traditionally, the diode bridge rectifier is used for AC-DC power conversion. This rectifier has the advantages of a simple circuit configuration and a low cost. Nevertheless, this rectifier results in some power pollutions, such as a high pulsating input current, a low power factor, and a high total harmonic distortion of the input current (THD_i). In order to improve these power pollutions and to meet the requirements set by international regulatory standards, such as the international electrotechnical commission (IEC) and IEEE-519, power factor correction (PFC) topologies have been investigated [1]-[7]. These PFC circuits are used to cascade a DC-DC converter for DC power-supply applications. They can be divided into two approaches, two stages and single stage approaches. The two-stage structure can achieve a near unity power factor and a low THD_i. However, it suffers from the problems of high cost and a complicated control [8], [9]. Therefore, the single-stage PFC topologies have been studies to achieve good power quality and low cost in low power applications. Some single-stage structures use the boost converter in the front semi-stage, which operates in discontinuous conduction mode (DCM), to achieve a good power quality [10]-[12]. Nevertheless, the DC-link voltage of this single-stage converter is higher than the amplitude of the input voltage. Thus the DC-link voltage will be higher than 450 V at the universal input voltage (90~264 V_{rms}). Some topologies have been studied to reduce the DC-link voltage [13]-[16]. However, they result in a poor THD_i. A buck-boost converter with DCM operation is utilized in the front semi-stage of the single-stage structures to provide good power quality and a low DC-link voltage [17]-[20]. However, these converters do not provide electrical isolation [17], [18]. In [19] and [20], the leakage-inductor energy of the transformer can not be recycled.

A new isolated single-phase AC-DC converter is presented in this paper, as shown in Fig. 1. The proposed converter integrates a modified AC-DC buck-boost converter with a DC-DC forward converter. The transformer can provide electrical isolation. The tertiary winding N_3 is used for recycling the residual magnetism of the transformer to the

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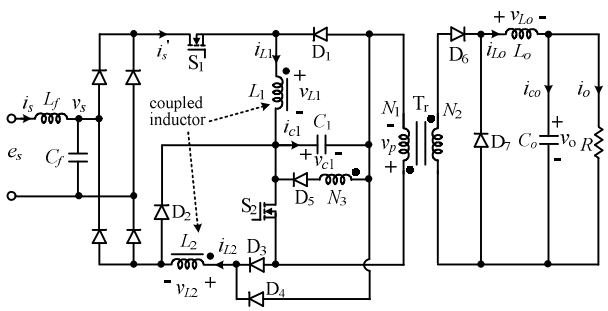


Fig. 1. Circuit configuration of the proposed converter.

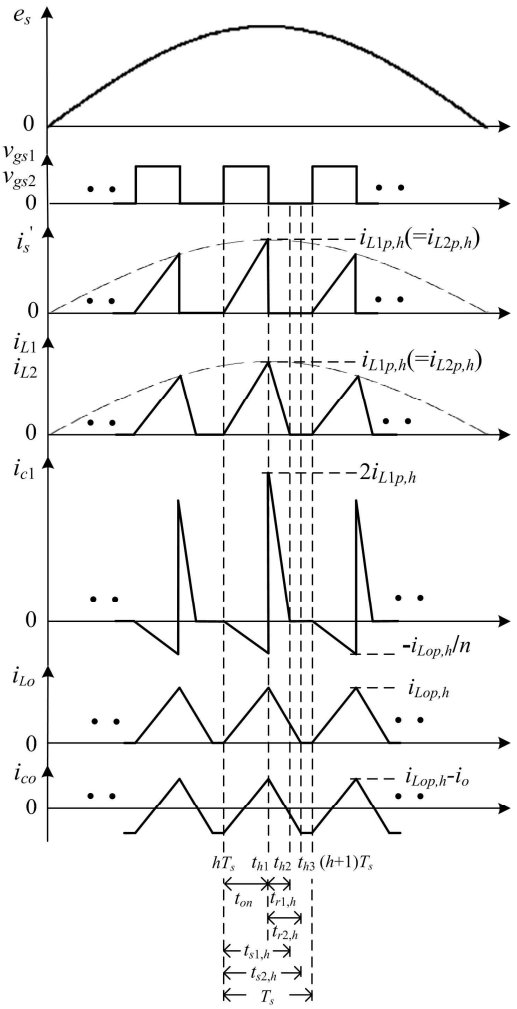


Fig. 2. Key waveforms of the proposed converter for 0<ωt<π.

capacitor C_1. The turns of the tertiary winding N_3 are equal the turns of the primary winding N_1. This converter can achieve a high power factor, a low THD_i, and a low DC-link voltage. In addition, it can be used for universal input voltage.

II. OPERATING PRINCIPLE

The two semi-stages of the proposed converter are operated in DCM with a fixed duty ratio by using a simple pulse-width modulation control strategy. The switches, S_1 and S_2, are triggered using the same control signal. A coupled inductor with same winding-turn in the primary and secondary sides is employed in the proposed converter. The primary and secondary windings of the coupled inductor are charged in series from the line source during the switch-on period and are discharged in parallel during the switch-off period. The discharge time can be shortened. The duty ratio can be extended. Thus the front semi-stage can be operated in a larger duty-ratio range than the conventional AC-DC buck-boost converter for DCM operation. Therefore, the proposed converter can be applied for universal input voltage and a wide output-power range. Fig. 2 shows some key waveforms in a half line source period. Due to the symmetrical characteristics of the single-phase system, the following operating principle is analyzed for $0 < \omega t < \pi$, where ω is the line angular frequency.

(I) Mode 1: The current-flow path is shown in Fig. 3(a). When the switches, S_1 and S_2, are turned on during time interval $[hT_s, t_{h1}]$, the primary and secondary windings of the coupled inductor are charged by series from the line source, and the energy stored in DC-link capacitor C_1 is discharged to output inductor L_o, output capacitor C_o, and the load via transformer T_r. The voltage v_p across the primary winding of the transformer is equal to v_{c1}.

(II) Mode 2: The current-flow path is shown in Fig. 3(b). While the switches, S_1 and S_2, are turned off during time interval $[t_{h1}, t_{h2}]$, the primary and secondary windings of the coupled inductor release their energies by parallel to DC-link capacitor C_1, and the energy stored in output inductor L_o is released to output capacitor C_o and the load. The residual magnetism of the transformer is recycled to capacitor C_1 via tertiary winding N_3. The voltage v_p across the primary winding of the transformer is equal to $-v_{c1}$.

(III) Mode 3: The current-flow path is shown in Fig. 3(c). The switches, S_1 and S_2, are still turned off during time interval $[t_{h2}, t_{h3}]$. The coupled-inductor currents, i_{L1} and i_{L2}, are equal to zero at $t = t_{h2}$. The energy stored in output inductor L_o is still transferred to capacitor C_o and the load.

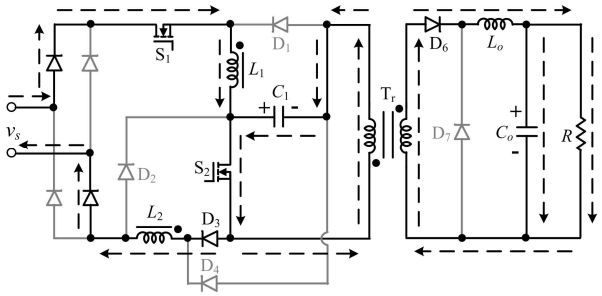
(IV) Mode 4: The current-flow path is shown in Fig. 3(d). While S_1 and S_2 are still turned off during time interval $[t_{h3}, (h+1)T_s]$, the energy stored in output inductor L_o is released to empty at $t = t_{h3}$. The load is supplied from capacitor C_o.

III. STEADY-STATE ANALYSIS

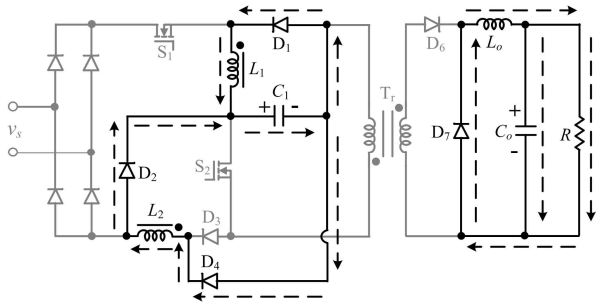
Due to the symmetrical characteristics of single-phase systems, the following analysis is discussed for $0 < \omega t < \pi$. For the sake of simplicity, the effect of the input filter is neglected. The line voltage is given as:

$$e_s(t) = v_s(t) = \sqrt{2}V_{rms}\sin\omega t = V_m \sin\omega t \qquad (1)$$

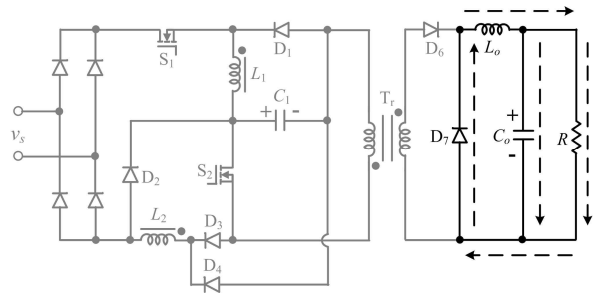
where V_{rms} and V_m are the root-mean-square value and the amplitude of the line voltage.



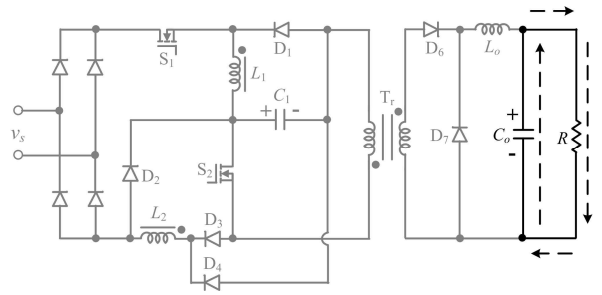
(a) Mode 1.



(b) Mode 2.



(c) Mode 3.



(d) Mode 4.

Fig. 3. Current-flow path of the proposed converter for $0<\omega t<\pi$.

Some of the parameters, such as t_{on}, t_{h1}, t_{h2}, t_{h3}, $t_{r1,h}$, $t_{r2,h}$, $t_{s1,h}$, and $t_{s2,h}$, are used for the following steady-state analyses. These parameters are defined in Fig. 2. Since the switching frequency f_s is much larger than the line frequency f_l, the line voltage can be considered as a piecewise constant during each switching period. Assuming that m is the switching number within time interval $[0, \pi/\omega]$, m is equal to $f_s/2f_l$. The following analysis is considered during switching period $[hT_s, (h+1)T_s]$, where h = 0, 1, ….., m-1. Since the primary and secondary winding turns of the coupled inductor are the same, the inductance of the coupled inductor in the primary and secondary sides are expressed as:

$$L_1 = L_2 = L \tag{2}$$

The mutual inductance M of the coupled inductor is given by

$$M = k\sqrt{L_1 L_2} = kL \tag{3}$$

where k is the coupling coefficient of the coupled inductor.

The voltages across the primary and secondary windings of the coupled inductor are as follows:

$$v_{L1} = L_1 \frac{di_{L1}}{dt} + M\frac{di_{L2}}{dt} = L\frac{di_{L1}}{dt} + kL\frac{di_{L2}}{dt} \tag{4}$$

$$v_{L2} = M\frac{di_{L1}}{dt} + L_2\frac{di_{L2}}{dt} = kL\frac{di_{L1}}{dt} + L\frac{di_{L2}}{dt} \tag{5}$$

When S_1 and S_2 are turned on, the following equations are obtained as:

$$i_{L1} = i_{L2}, \quad hT_s \le t \le t_{h1} \tag{6}$$

$$v_{L1} + v_{L2} = |e_s(t_h)|, \quad hT_s \le t \le t_{h1} \tag{7}$$

$$\frac{v_{c1}}{n} = v_{Lo} + v_o = L_o\frac{di_{Lo}(t)}{dt} + v_o, \quad hT_s \le t \le t_{h1} \tag{8}$$

where n is the turns ratio (N_1/N_2) of transformer Tr.

Substituting (4)–(6) into (7), yields:

$$\frac{di_{L1}(t)}{dt} = \frac{di_{L2}(t)}{dt} = \frac{|e_s(t_h)|}{2(1+k)L}, \quad hT_s \le t \le t_{h1} \tag{9}$$

The coupled-inductor currents, i_{L1} and i_{L2}, are derived as:

$$i_{L1}(t) = i_{L2}(t) = \frac{|e_s(t_h)|}{2(1+k)L}(t - hT_s), \quad hT_s \le t \le t_{h1} \tag{10}$$

From (8), the following equation is found to be:

$$\frac{di_{Lo}(t)}{dt} = \frac{1}{L_o}\left(\frac{v_{c1}}{n} - v_o\right), \quad hT_s \le t \le t_{h1} \tag{11}$$

At $t = t_{h1}$, the peak values of i_{L1}, i_{L2}, and i_{Lo} are given by:

$$i_{L1p,h} = i_{L2p,h} = \frac{|e_s(t_h)|}{2(1+k)L}t_{on} \tag{12}$$

$$i_{Lop,h} = \frac{1}{L_o}\left(\frac{v_{c1}}{n} - v_o\right)t_{on} \tag{13}$$

where t_{on} is equal to dT_s and d is the duty ratio.

While S_1 and S_2 are turned off, the voltages across the primary and secondary windings of the coupled inductor are obtained as:

$$v_{L1} = v_{L2} = -v_{c1}, \quad t_{h1} \le t \le t_{h2} \tag{14}$$

$$v_{Lo} = -v_o, \quad t_{h1} \le t \le t_{h3} \tag{15}$$

Substituting (4) and (5) into (14), yields:

$$\frac{di_{L1}(t)}{dt} = \frac{di_{L2}(t)}{dt} = -\frac{v_{c1}}{(1+k)L}, \quad t_{h1} \le t \le t_{h2} \tag{16}$$

Therefore, i_{L1} and i_{L2} are found to be:

$$i_{L1}(t) = i_{L2}(t) = -\frac{v_{c1}}{(1+k)L}(t - t_{h1}) + i_{L1p,h}, \quad t_{h1} \le t \le t_{h2} \tag{17}$$

From (15), the following equation is derived as:

$$\frac{di_{Lo}}{dt} = -\frac{v_o}{L_o}, \quad t_{h1} \le t \le t_{h3} \tag{18}$$

Thus:

$$i_{Lo}(t) = -\frac{v_o}{L_o}(t - t_{h1}) + i_{Lop,h}, \quad t_{h1} \le t \le t_{h3} \tag{19}$$

Since $i_{L1}(t_{h2}) = i_{L2}(t_{h2}) = 0$ and $i_{Lo}(t_{h3}) = 0$, the peak values of i_{L1}, i_{L2}, and i_{Lo} are obtained from (17) and (19).

$$i_{L1p,h} = i_{L2p,h} = \frac{v_{c1}}{(1+k)L} t_{r1,h} \tag{20}$$

$$i_{Lop,h} = \frac{v_o}{L_o} t_{r2,h} \tag{21}$$

where $t_{r1,h} = t_{h2} - t_{h1}$ and $t_{r2,h} = t_{h3} - t_{h1}$.

From (12), (13), (20), and (21), the time durations, $t_{r1,h}$ and $t_{r2,h}$, are obtained as follows:

$$t_{r1,h} = \frac{|e_s(t_h)|}{2v_{c1}} dT_s \tag{22}$$

$$t_{r2,h} = \frac{1}{v_o}\left(\frac{v_{c1}}{n} - v_o\right) dT_s \tag{23}$$

A. Unfiltered Input Current i_s'

From Fig. 2, the average unfiltered input current i_s' in one switching period T_s can be derived as:

$$i'_{s,avg}(t) = \frac{t_{on} i_{L1p}}{2T_s} = \frac{d^2 T_s V_m}{4(1+k)L} |\sin \omega t| \tag{24}$$

Equation (24) indicates that the average unfiltered input current is sinusoidal and is in phase with the input voltage. Moreover, the harmonic components of i_s' are distributed over multiples of the switching frequency. Thus it is very easy to filter out the harmonic components by employing a set of input filters L_f-C_f. The cutoff frequency of the input filter is much lower than the switching frequency. The cutoff frequency of the input filter is determined to be:

$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{25}$$

B. Voltage Gain

From Fig. 2, the average values of i_{c1} and i_{co} during time interval $[hT_s, (h+1)T_s]$ can be computed as:

$$i_{c1,h} = \frac{1}{T_s}\left(i_{L1p,h} t_{r1,h} - \frac{i_{Lop,h}}{2n} t_{on}\right) \tag{26}$$

$$i_{co,h} = \frac{1}{T_s}\left[\frac{1}{2} i_{Lop,h}(t_{on} + t_{r2,h}) - i_o T_s\right] \tag{27}$$

Substituting (1), (12), (13), (22), and (23) into (26) and (27) yields:

$$i_{c1,h} = \frac{d^2 T_s V_m^2}{4(1+k)Lv_{c1}} \sin^2 \omega t_h - \frac{d^2 T_s (v_{c1} - nv_o)}{2n^2 L_o} \tag{28}$$

$$i_{co,h} = \frac{d^2 T_s v_{c1}(v_{c1} - nv_o)}{2n^2 L_o v_o} - i_o \tag{29}$$

Thus the average value of i_{c1} during one half of line-source period $[0, \pi/\omega]$, is written as follows:

$$i_{c1,avg} = \frac{\omega}{\pi}\sum_{h=0}^{m-1} i_{c1,h} T_s = \frac{\omega}{\pi}\sum_{h=0}^{m-1}\left[\frac{d^2 T_s V_m^2}{4(1+k)Lv_{c1}} \sin^2 \omega t_h - \frac{d^2 T_s (v_{c1} - nv_o)}{2n^2 L_o}\right] T_s \tag{30}$$

Due to the fact that $m >> 1$, the above equation can be approximated as:

$$i_{c1,avg} = \frac{\omega}{\pi}\int_0^{\frac{\pi}{\omega}}\left[\frac{d^2 T_s V_m^2}{4(1+k)Lv_{c1}} \sin^2 \omega t - \frac{d^2 T_s (v_{c1} - nv_o)}{2n^2 L_o}\right] dt = \frac{d^2 T_s V_m^2}{8(1+k)Lv_{c1}} - \frac{d^2 T_s (v_{c1} - nv_o)}{2n^2 L_o} \tag{31}$$

Then, the differential equation of v_{c1} is given by:

$$\frac{dv_{c1}}{dt} = \frac{d^2 T_s}{2C_1}\left[\frac{V_m^2}{4(1+k)Lv_{c1}} - \frac{v_{c1} - nv_o}{n^2 L_o}\right] \tag{32}$$

From (29), the differential equation of v_o during one switching period is obtained as follows:

$$\frac{dv_o}{dt} = \frac{1}{C_o}\left[\frac{d^2 T_s v_{c1}(v_{c1} - nv_o)}{2n^2 L_o v_o} - \frac{v_o}{R}\right] \tag{33}$$

Thus the following equations of the DC model can be derived from (32) and (33).

$$\frac{V_m^2}{4(1+k)LV_{c1}} = \frac{V_{c1} - nV_o}{n^2 L_o} \tag{34}$$

$$\frac{D^2 T_s V_{c1}(V_{c1} - nV_o)}{2n^2 L_o V_o} = \frac{V_o}{R} \tag{35}$$

where V_{c1}, V_o, and D are the DC quantities of v_{c1}, v_o, and d, respectively.

The normalized inductor time constant of the two semi-stages are defined as follows:

$$\tau_L \equiv \frac{L}{RT_s} = \frac{Lf_s}{R} \tag{36}$$

$$\tau_{Lo} \equiv \frac{L_o}{RT_s} = \frac{L_o f_s}{R} \tag{37}$$

where f_s is the switching frequency.

By substituting (36) and (37) into (34) and (35), the voltage gain of the proposed converter is found to be:

$$G = \frac{V_o}{V_m} = G_1 G_2 \tag{38}$$

where

$$G_1 = \frac{V_{c1}}{V_m} = \sqrt{\frac{n^2 \tau_{Lo}}{4(1+k)\tau_L(1 - nG_2)}} \tag{39}$$

$$G_2 = \frac{V_o}{V_{c1}} = \frac{-D^2 + \sqrt{D^4 + 8D^2 \tau_{Lo}}}{4n\tau_{Lo}} \tag{40}$$

C. Boundary Operating Condition

In order to ensure that the two semi-stages of the proposed converter are operated in DCM, i_{L1}, i_{L2}, and i_{Lo} must go to zero during the switch-off period in each switching period. From Fig. 2, the two time durations, $t_{s1,h}$ and $t_{s2,h}$, are obtained as follows:

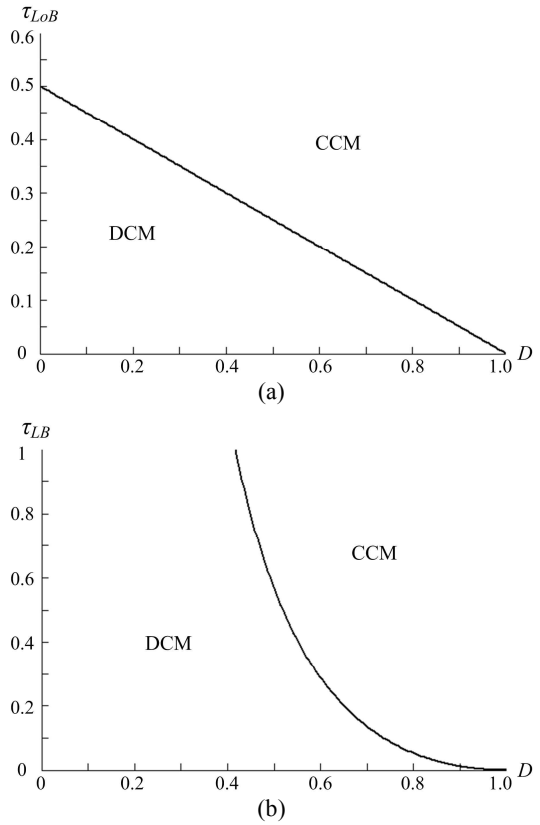


Fig. 4. Boundary condition. (a) Rear semi-stage; (b) Front semi-stage (under $\tau_{Lo} = 0.25$, $k = 1$, and $n = 1.5$).

$$t_{s1,h} = t_{on} + t_{r1,h} = \frac{DT_s(2V_{c1} + |e_s(t_h)|)}{2V_{c1}} \tag{41}$$

$$t_{s2,h} = t_{on} + t_{r2,h} = \frac{V_{c1}DT_s}{nV_o} \tag{42}$$

When the maximum of $t_{s1,h}$ is equal to T_s and $|e_s(t_h)|$ is equal to V_m, the front semi-stage of the proposed converter is operated in boundary conduction mode (BCM). Similarly, when $t_{s2,h}$ is equal to T_s, the rear semi-stage of the proposed converter is also operated in BCM. Thus by simplifying (41) and (42), the boundary voltage gains are found to be:

$$G_{1,bc} = \frac{V_{c1}}{V_m} = \frac{D}{2(1-D)} \tag{43}$$

$$G_{2,bc} = \frac{V_o}{V_{c1}} = \frac{D}{n} \tag{44}$$

$$G_{bc} = G_{1,bc}G_{2,bc} = \frac{D^2}{2n(1-D)} \tag{45}$$

When $G_1 = G_{1,bc}$ and $G_2 = G_{2,bc}$, the normalized inductor time constants in BCM are given by:

$$\tau_{LoB} = \frac{1-D}{2} \tag{46}$$

$$\tau_{LB} = \frac{4n^2\tau_{Lo}^2(1-D)^2}{(1+k)D^2(4\tau_{Lo} + D^2 - \sqrt{D^4 + 8D^2\tau_{Lo}})} \tag{47}$$

From (46) and (47), the curve of τ_{LoB} is plotted in Fig. 4(a). It can be seen that the rear semi-stage of the proposed converter is operated in DCM if $\tau_{Lo} < \tau_{LoB}$. Assuming that $\tau_{Lo} = 0.25$, $k = 1$, and $n = 1.5$, the curve of τ_{LB} is plotted in Fig. 4(b). It can be seen that the front semi-stage of the proposed converter is operated in DCM if $\tau_L < \tau_{LB}$.

IV. Selections of Inductors and Capacitors

A. Selection of Inductors L_1, L_2, and L_o

In order to ensure that the two semi-stages of the proposed converter are operated in DCM, appropriate τ_{LoB} and τ_{LB} are selected under the required voltage gain. Thus L_o, L_1, and L_2 must satisfy the following inequality.

$$L_o < \frac{R}{f_s}\tau_{LoB} \tag{48}$$

$$L_1 = L_2 = L < \frac{R}{f_s}\tau_{LB} \tag{49}$$

B. Selection of DC-Link Capacitor C_1

From (28), the average value of the current $i_{c1,h}$ per switching period can be rewritten as:

$$i_{c1,h} = \frac{D^2T_s}{2}\left[\frac{V_m^2}{4(1+k)LV_{c1}} - \frac{V_{c1} - nV_o}{n^2L_o}\right] - \frac{D^2T_sV_m^2}{8(1+k)LV_{c1}}\cos 2\omega t_h \tag{50}$$

Substituting (34) into (50), the ripple of the DC-link voltage per switching period is obtained as:

$$\Delta V_{c1,h} = \left[-\frac{D^2V_m^2}{8(1+k)LC_1f_sV_{c1}}\cos 2\omega t_h\right]T_s \tag{51}$$

Hence, the function of the ripple of the DC-link voltage per one half line-source period can be computed as:

$$\Delta V_{c1}(t) = \int_0^t\left[-\frac{D^2V_m^2}{8(1+k)LC_1f_sV_{c1}}\cos 2\omega t'\right]dt'$$
$$= -\frac{D^2V_m^2}{8(1+k)LC_1f_sV_{c1}} \times \frac{\sin 2\omega t}{2\omega} \tag{52}$$

From (52), the ripple of the DC-link voltage per one half line-source period is derived as:

$$V_{c1,ripple} = 2\left|\Delta V_{c1}(t)\right|_{peak} = \frac{D^2V_m^2}{8(1+k)\omega LC_1f_sV_{c1}} \tag{53}$$

Thus:

$$\frac{V_{c1,ripple}}{V_{c1}} = \frac{D^2V_m^2}{8(1+k)\omega LC_1f_sV_{c1}^2} = \frac{D^2}{8(1+k)\omega LC_1f_sG_1^2} \tag{54}$$

Therefore, to satisfy the specification of the ripple percentage of the DC-link voltage, capacitor C_1 needs to satisfy the following inequality:

$$C_1 \geq \frac{D^2}{8(1+k)\omega Lf_sG_1^2} \times \frac{V_{c1}}{V_{c1,ripple}} \tag{55}$$

V. Experimental Results

In order to verify the feasibility of the proposed converter, a prototype circuit has been implemented in the laboratory.

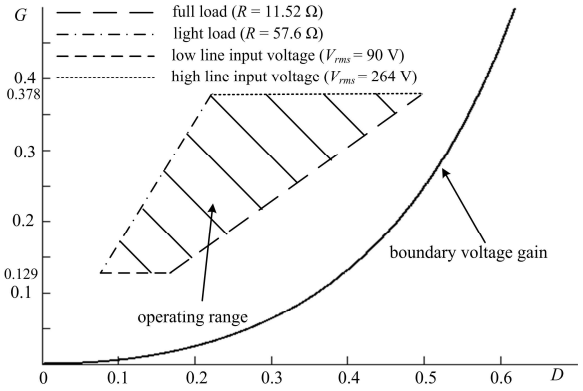
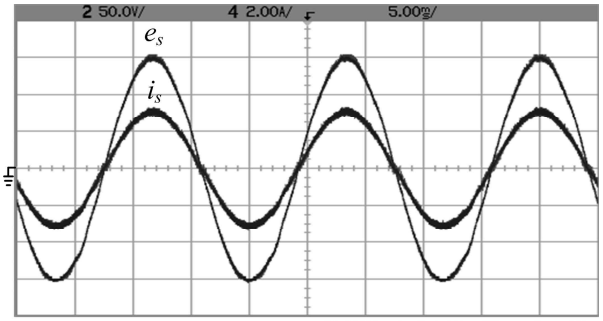
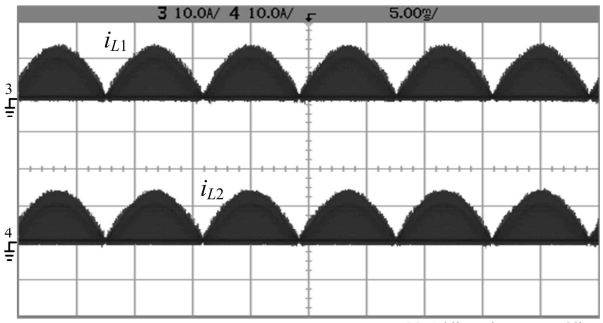


Fig. 5. Operating range of the prototype circuit.



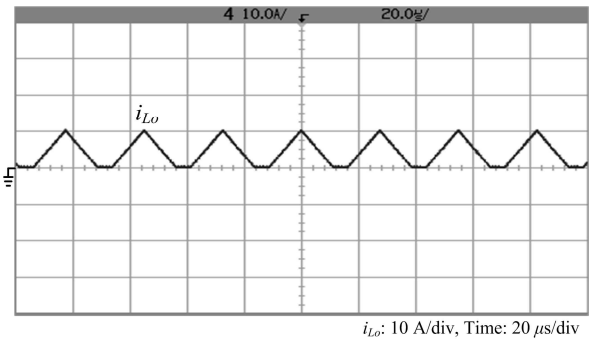
e_s: 50 V/div, i_s: 2 A/div, Time: 5 ms/div

Fig. 6. Waveforms of input voltage and input current.



i_{L1}, i_{L2}: 10 A/div, Time: 5 ms/div

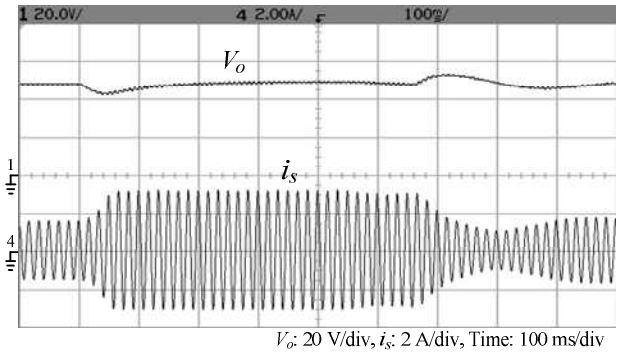
Fig. 7. Waveforms of coupled-inductor currents.



i_{Lo}: 10 A/div, Time: 20 μs/div

Fig. 8. Waveform of output-inductor current.

The electrical specifications and circuit parameters are selected to be V_{rms} = 90~264 V (V_m = 127~373 V), V_o = 48 V, P_o = 40~200 W (R = 11.52~57.6 Ω), f_l = 60 Hz, f_s = 36 kHz,



V_o: 20 V/div, i_s: 2 A/div, Time: 100 ms/div

Fig. 9. Waveforms of output voltage V_o and input current i_s under load variation between 100 W and 200 W.

L_f = 1.5 mH, C_f = 600 nF, and n = 1. From the electrical specifications, it can be seen that the voltage gain G is varied from 0.129 to 0.378. By substituting G = 0.378 and n = 1 into (45), the maximum duty ratio D_{max} is derived as 0.57. By substituting D_{max} = 0.57 into (46), τ_{LOB} is found to be 0.215. By substituting D_{max} = 0.57, τ_{LO} = 0.215, n = 1, and k = 1 into (47), τ_{LB} is given as 0.142. By using (48) and (49), inductors, L_1, L_2, and L_o, are obtained as follows:

$$L_o < \frac{R}{f_s}\tau_{LoB} = \frac{11.52}{36\text{k}} \times 0.215 = 68.8\ \mu\text{H}$$

$$L < \frac{R}{f_s}\tau_{LB} = \frac{11.52}{36\text{k}} \times 0.142 = 45.4\ \mu\text{H}$$

Due to the fact that $L_1 = L_2 = L$, L_1 and L_2 are chosen to be 34.1 μH. In addition, L_o is selected to be 54.6 μH. Thus τ_{LO} and τ_L are 0.171 and 0.107 under the full-load condition (R = 11.52 Ω), and τ_{LO} and τ_L are 0.0341 and 0.0213 under the light-load condition (R = 57.6 Ω). By substituting k = 1, n = 1, and the above values of τ_{LO} and τ_L into (38), the operating range of the prototype circuit is shown in Fig. 5. It can be seen that that the proposed converter is operated in DCM. The ripple percentage of DC-link voltage V_{c1} is considered under the conditions V_{rms} = 90 V and R = 11.52 Ω. Thus by substituting G = 0.378, τ_{LO} = 0.171, τ_L = 0.107, n = 1, and k = 1 into (38), the duty ratio D is derived as 0.5. From (39) and (40), G_2 and G_1 are found to be 0.564 and 0.677, respectively. The ripple percentage of V_{c1} is selected to be 5%. Thus capacitor C_1 can be obtained from (55).

$$C_1 \geq \frac{D^2}{8(1+k)\omega L f_s G_1^2} \times \frac{V_{c1}}{V_{c1,ripple}} = 1473\ \mu\text{F}$$

C_1 is selected to be 1640 μF, and C_o is chosen to be 1000 μF.

Some measured results under V_{rms} = 110 V, V_o = 48 V, and P_o = 200 W are shown in Figs. 6-9. Fig. 6 depicts the waveforms of the input voltage and input current. As can be seen, the input current is in phase with the input voltage. Thus the power factor is almost unity. The waveforms of the coupled-inductor current i_{L1} and i_{L2} are shown in Fig. 7. It can be seen that the front-semi stage of the proposed converter is operated in DCM. This is consistent with the operating

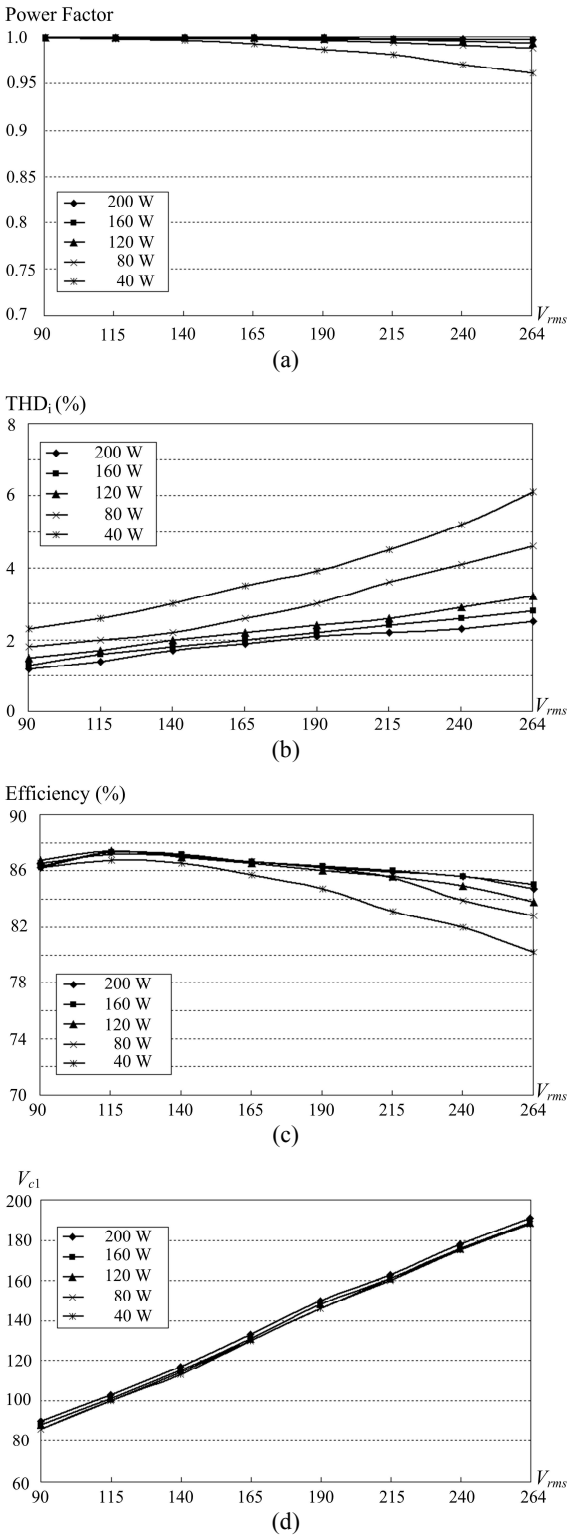


Fig. 10. Measured results under various input voltage and output power, (a) Power factor, (b) THD_i , (c) Efficiency, (d) V_{c1}.

principles. Fig. 8 shows the waveforms of the output-inductor current i_{Lo}. It can be seen that the rear semi-stage is operated in DCM. This also agrees with the operating principles. The waveforms of output voltage V_o and input current i_s under load variations between 100 W and 200 W are shown in Fig. 9. The output voltage V_o is well regulated at 48 V. Moreover, the measured power factor, THD_i, efficiency, and DC-link voltage V_{c1} under various input voltages and output powers are shown in Fig. 10. From Fig. 10(a), it can be seen that the power factor is higher than 0.96 and that an almost unity power factor is achieved under a heavy load. The THD_i is less than 6.1% as shown in Fig. 10(b). Fig. 10(c) shows the measured efficiency. It can be seen that the maximum efficiency is 87.4%. As can be seen in Fig. 10(d), DC-link voltage V_{c1} is varied with the input voltage and is less than the amplitude of the input voltage. Based on practical applications, the voltage across the capacitor must be less than 450 V. It can be seen that the maximum V_{c1} is equal to 191 V at V_{rms} = 264 V.

VI. CONCLUSIONS

A new isolated single-phase AC-DC converter is investigated in this paper. A modified AC-DC buck-boost converter and a forward DC-DC converter are integrated in the proposed converter to achieve an almost unity power factor, a low THD_i, a low DC-link voltage, electrical isolation, and an adjustable output voltage. The proposed converter is suitable for universal input voltage and a wide output power range. Moreover, the steady-state analysis of the proposed converter is presented in detail. A prototype circuit of the proposed converter is implemented in the laboratory. From the measured results, it can be seen that a high power factor, a low THD_i, and a low DC-link voltage are achieved under various input voltages and output powers.

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