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Analysis of the Admittance Component for Digitally Controlled Single-Phase Bridgeless PFC Converter

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Abstract

This paper analyzes the effect of the admittance component for the digitally controlled single-phase bridgeless power factor correction (PFC) converter. To do this, it is shown how the digital delay effects such as the digital pulse-width modulation (DPWM) and the computation delays restrict the bandwidth of the converter. After that, the admittance effect of the entire digital control system is analyzed when the bridgeless PFC converter which has the limited bandwidth is connected to the grid. From this, the waveform distortion of the input current is explained and the compensation method for the admittance component is suggested to improve the quality of the input current. Both the simulations and the experiments are performed to verify the analyses taken in this paper for the 1 kW bridgeless PFC converter prototype.

Key words: Admittance compensation, Bridgeless PFC converter, Digital current controller, *K*-factor approach

I. INTRODUCTION

Single-phase power factor correction (PFC) converters have been used for many industrial applications such as aircraft power supplies, light-emitting-diode drivers, electronic ballast circuits, and so on [1]-[5]. Among many circuit topologies for PFC operation, the bridgeless PFC topology which does not have the diode bridge for rectification of the input voltage and current is getting popular because the topology features high efficiency and simple control [6]-[8]. Generally, controllers for the bridgeless PFC converter are not different from the ones of the traditional boost PFC converters, in where a voltage controller as an outer loop and a current controller as an inner loop are employed. For the voltage controller, the bandwidth is selected to be lower than the fundamental electrical frequency to minimize the well-known double frequency power fluctuation effect for the control loop. However, for the current controller, the bandwidth is required to have as high as possible to regulate the shape of the input current as the input voltage [9]. Consequently, maximizing the bandwidth of the current controller is an important issue for the single-phase bridgeless PFC converter. The current controller can be implemented either in analog or in digital control scheme. In terms of regulating performance, analog controllers may show better results than digital controllers. However, digital controllers have more flexibility to implement entire control system including operating sequences, communication features, fault protections, and so on. Hence, adapting the digital control techniques is getting popular for the bridgeless PFC converters. Basically, most of the existing control schemes for traditional boost PFC converter can be directly applied to the bridgeless PFC converter. In [10], the current sharing and the proportional-integral (PI) controllers are designed for digital signal processor (DSP) based interleaved boost PFC converter. A predictive control strategy has been proposed in [11]. Some papers have been discussed about continuous conduction mode (CCM) and discontinuous conduction mode (DCM) operations for the single-phase boost PFC converters [12]-[15]. Reference [16] discusses that the digital delays normally degrade the performance of the digital current controller by analyzing the small-signal model considering the time delay effect as well as evaluating the stability of the converter. In [17], the transfer functions for a digitally controlled PFC converter have been described with consideration of the digital delay effects. On the other hand, the duty feed-forward schemes have been studied to improve

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the quality of the input phase current. The impedance analyses have been performed with and without the duty feed-forward scheme, and it is proven that the duty feed-forward scheme can improve the behavior of the current controller [17]. Reference [18] proposes the feed-forward control which includes a term proportional to the derivative of the reference current. The duty feed-forward schemes can be also called as "admittance compensation method" in some literatures [19]-[21] because the effect of the input voltage fluctuation can be physically modeled as an admittance component in the entire control system.

In this paper, the effect of the admittance component is analyzed for the digitally controlled single-phase bridgeless PFC converter. To consider the digital delay effects, a zero-order-hold (ZOH) which causes phase delay in high frequency regions and reduces the phase margin of the plant is included into the control-to-inductor current model. By using the derived model and assuming a type-II compensator is employed, the maximum achievable bandwidth of the converter is evaluated with the given parameters and the operating conditions. Then the design procedure for the type-II compensator based current controller is described in detail. After that, the admittance component is analyzed in the entire control loop. Apparently, the analysis taken in this paper shows that the effect of the admittance component with the digital controller is more severe than analog controllers because of the reduced bandwidth. In order to compensate the admittance component effect, the admittance compensation method which may be a similar form with the duty feed-forward schemes is introduced. The simulations and the experiments have been carried out to verify the analyses taken in this paper and the effect of the admittance compensation strategy for the 1 kW bridgeless PFC converter.

II. MODELING OF THE BRIDGELESS PFC CONVERTER

A. The Analog and the Digital Models

Fig. 1 shows the bridgeless PFC converter dealt in this paper. In terms of the control of the bridgeless PFC converter, the input phase current and the output voltage controllers are necessary. Generally, the performance of the current controller affects the performance of the PFC converter a lot. In order to design the current controller, a control-to-inductor current model for the bridgeless PFC converter may be needed. Usually, the control-to-inductor current model can be expressed as a second order function. However, the first order model as shown in (1) is also a popular solution to simplify the analysis [21].

$$G_{id}(s) = \frac{V_o}{sL} \tag{1}$$

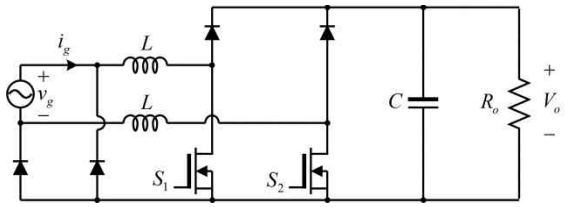


Fig. 1. Circuit configuration of the bridgeless PFC converter.

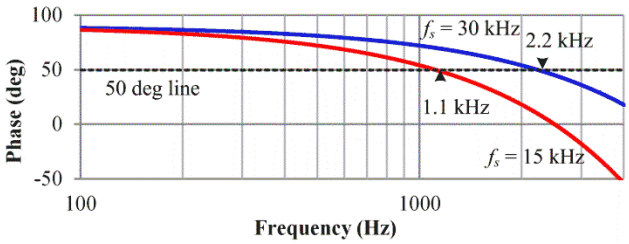


Fig. 2. Changes of θ_{idz} according to f_s.

TABLE I
THE MAXIMUM BANDWIDTH OF THE BRIDGELESS PFC CONVERTER

Phase margin	40	50	60	70
Bandwidth	0.091f_s	0.073f_s	0.055f_s	0.036f_s

where V_o represents the output dc-link voltage. Although (1) does not contain the LC resonance which can be found in the second order model, it is enough to be utilized for current controller design. If the triangular carrier waveform is employed, and the digital controller and the DPWM are updated once in a switching period, the modulator can be modeled as a ZOH [22]. By considering the typical one sample delay in a digital controller [23], the control-to-inductor current model $G_{idz}(z)$ which consider the plant model of the bridgeless PFC converter is simply modeled as,

$$G_{idz}(z) = \frac{T_s V_o}{L} \frac{1}{z(z-1)} \tag{2}$$

where T_s represent the sampling frequency which is inverse proportional to the switching frequency f_s. Equation (2) will be utilized to design the digital feedback controller which will be discussed in a later section.

B. Bandwidth limitation of the Digitally Controlled Bridgeless PFC Converter

In this section, the limitation of the current control bandwidth is discussed. To design the feedback controller, it is assumed that *K*-factor design based type-II compensator is employed. Note that a type-II compensator induces maximum 90 deg of the phase boost effect. In this paper, the target phase margin is selected to be 50 deg to operate the entire control system in stable. From (1), it can be intuitively recognized that the phase margin of the *s*-domain model can be 90 deg in the entire frequency region. Unlike the *s*-domain

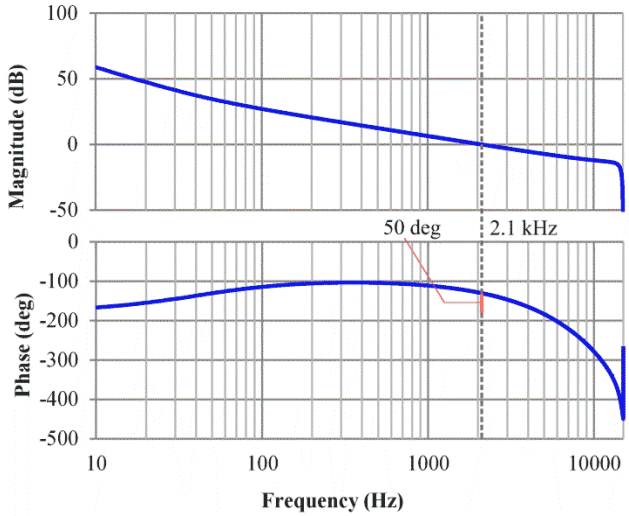


Fig. 3. Loop gain analysis of the designed control system.

TABLE II
THE PARAMETERS OF THE BRIDGELESS PFC CONVERTER

Rated power (P_o)	1 kW
Input RMS voltage (V_{g_rms})	120 V
Output dc-link voltage (V_o)	200 V
Input filter inductance (L)	800 μH
Output dc-link capacitance (C)	1120 μF
Switching frequency (f_s)	30 kHz

model, the z-domain model in (2) may have phase lagging in high frequency region because of the delays caused from the DPWM and the digital calculation delay. Accordingly, the phase margin of $G_{idz}(z)$ is reduced in high frequency regions. It should be noted that the phase margin of $G_{idz}(z)$ is the maximum achievable phase margin in the closed-loop control system with the type II compensator. By substituting $z = e^{j2\pi f_r T_s}$ and manipulating several steps, the maximum achievable phase margin can be derived as,

$$\theta_{idz} = -\tan^{-1}\left(\frac{\sin(4\pi f_r T_s)-\sin(2\pi f_r T_s)}{\cos(4\pi f_r T_s)-\cos(2\pi f_r T_s)}\right)\times\frac{180}{\pi} \quad (3)$$

where f_r is the evaluating frequency. If f_r is fixed, θ_{idz} depends on T_s from (3).

Fig. 2 illustrates the changes of θ_{idz} when the switching frequencies are 30 kHz and 15 kHz. If over 50 deg of phase margin is guaranteed in the control system, θ_{idz} should be higher than 50 deg at the crossover frequency. The frequencies which satisfy the condition above are 2.2 kHz for f_s = 30 kHz and 1.1 kHz for f_s = 15 kHz in Fig. 2. Consequently, the maximum bandwidths which secure 50 deg of phase margin are evaluated as 2.2 kHz and 1.1 kHz for f_s = 30 kHz and 15 kHz, respectively. Table I shows the maximum achievable bandwidth at the different phase margins when f_s is fixed as 30 kHz. Note that unlike an analog controller implementation which generally maximizes

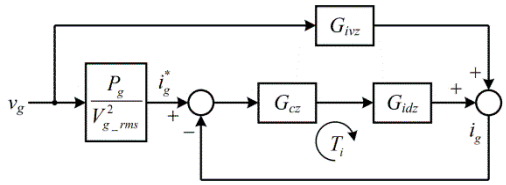


Fig. 4. Current control loop of the bridgeless PFC converter.

the control bandwidth up to 0.16f_s with 40 deg of phase margin, the bandwidth of the digital controller is much reduced as shown in Table I. This is one of the key issues which degrade the quality of the input current waveform in the digitally controlled bridgeless PFC converter.

C. Digital Current Controller Design

The general expression of a type-II based digital feedback controller is given as [24], [25],

$$G_{cz}(z) = \omega_c G_b \frac{T_s(z+1)}{2(z-1)}\left(\frac{\omega_c T_s(z+1)+2K(z-1)}{K\omega_c T_s(z+1)+2(z-1)}\right) \quad (4)$$

where ω_c and K are represented as,

$$\omega_c = \frac{2}{T_s}\tan(f_c T_s \pi) \quad (5)$$

$$K = \sqrt{\frac{\left(1+\sin\left(\left(PM-(90°-\phi_b)\right)\frac{\pi}{180}\right)\right)}{\left(1-\sin\left(\left(PM-(90°-\phi_b)\right)\frac{\pi}{180}\right)\right)}} \quad (6)$$

where f_c and PM mean the crossover frequency of the control system and the required phase margin at f_c. Note that (5) reflects the pre-warped frequency by considering the digitalization effect. In (4) and (6), G_b and ϕ_b denote the gain-boost and the phase-boost constants, respectively. Physically, G_b and ϕ_b are the required gain and phase which are adjusted by the feedback controller to achieve the desired design specification. In this paper, for a stable operation of the digitally controlled bridgeless PFC converter, the crossover frequency and the phase margin of the digital control system are chosen as,

$$f_c = 0.07 f_s \qquad PM = 50\,\text{deg} \quad (7)$$

The converter parameters are shown in Table II. By using the parameters in the table and the design specification, G_b, ϕ_b and K are calculated as,

$$\begin{aligned} G_b &= |G_{idz}(z)| = 25.62 \approx 0.0524 \\ \phi_b &= \angle|G_{idz}(z)| = 127.8\,\text{deg} \\ K &\approx 52.08 \end{aligned} \quad (8)$$

By substituting these values into (4), the digital feedback controller $G_{cz}(z)$ is numerically derived as,

$$G_{cz}(z) = 0.04842\frac{(z+1)(z-0.9915)}{(z-1)(z+0.8418)} \quad (9)$$

On the other hand, by using Table II, the numerical expression of the control-to-inductor current model $G_{idz}(z)$

can be calculated as,

$$G_{idz}(z)=\frac{8.333}{z(z-1)} \tag{10}$$

From (9) and (10), the loop-gain of the digital current control system $T_i(z)$ is derived as,

$$T_i(z)=G_{cz}(z)G_{idz}(z)=\frac{0.4035(z+1)(z-0.9915)}{z(z+0.8418)(z-1)^2} \tag{11}$$

The loop-gain of the current control system versus the frequency ranges from 10 Hz to the Nyquist frequency 15 kHz is shown in Fig. 3. As shown in the figure, the crossover frequency and the phase margin at the crossover frequency of $T_i(z)$ satisfies the required design specification $0.07f_s$(=2.1 kHz) and 50 deg.

III. ADMITTANCE COMPENSATION

A. Derivation of the Admittance Component in Z-domain

Fig. 4 shows the current control model of the bridgeless PFC converter shown in Fig. 1. From Fig. 4, the digital control model for the input current i_g is given as,

$$i_g(z)=\frac{G_{ivz}(z)}{1+T_i(z)}v_g(z)+\frac{T_i(z)}{1+T_i(z)}\frac{P_g}{V_{g\_rms}^2}v_g(z) \tag{12}$$

where P_g means the input power. The input power stage line-to-current model $G_{ivz}(z)$ is represented as,

$$G_{ivz}(z)=\frac{T_s}{L}\frac{1}{z(z-1)} \tag{13}$$

As similar to the method in [21], from (11), the closed-loop input admittance model in z-domain is derived as,

$$Y_z(z)=\frac{i_g(z)}{v_g(z)}=\frac{G_{ivz}(z)}{1+T_i(z)}+\frac{T_i(z)}{1+T_i(z)}\frac{P_g}{V_{g\_rms}^2} \tag{14}$$

B. Analysis of the Admittance Component

Equation (14) can be separated into the two components below.

$$Y_{zv}(z)=\frac{G_{ivz}(z)}{1+T_i(z)},\qquad Y_{zi}(z)=\frac{T_i(z)}{1+T_i(z)}\frac{P_g}{V_{g\_rms}^2} \tag{15}$$

Fig. 5 shows the frequency responses of $Y_{zv}(z)$, $Y_{zi}(z)$, and $Y_z(z)$ when P_g is 500 W. In physical, $Y_{zi}(z)$ represents the admittance component for the closed-loop duty-to-inductor current, and $Y_{zv}(z)$ means the closed-loop input power admittance component. As shown in Fig. 5, the magnitude of $Y_{zi}(z)$ is almost constant in the evaluated frequency range. Furthermore, the phase of $Y_{zi}(z)$ is also unvarying near the fundament frequency 60 Hz, but getting lagged in higher frequencies. Both of the magnitude and the phase of $Y_{zi}(z)$ shows a good agreement with a normal feedback control system. However, a large phase leading is observed at the low frequency region for $Y_{zv}(z)$. The magnitude of $Y_{zv}(z)$ is even more than $Y_{zi}(z)$ over 16 Hz. Consequently, the admittance of the entire control system over 16 Hz is mainly determined by $Y_{zv}(z)$. Generally, the fundamental and the third harmonic components affect the shape of the input current. In Fig. 5, the phases of the admittance component are leading at the fundamental frequency 60 Hz and the third harmonic frequency 180 Hz. This implies the input current will lead the input voltage. On the other hand, the response of $Y_z(z)$ depends on the input power P_g from (14) which includes $Y_{zi}(z)$. Fig. 6 shows the frequency responses of $Y_z(z)$ at different input power levels. As shown in the figure, more phase lagging is found under lower P_g conditions near the fundamental frequency. Consequently, it is supposed that the phase leading effect is dominant as P_g becomes lower. If an analog controller is applied so that the bandwidth of the entire control system is large enough to overcome the admittance component, the shape of the input current can be a beautiful sinusoidal waveform even with only a simple feedback control. However, in the digitally controlled bridgeless PFC converter, the admittance component cannot be compensated even at the fundamental frequency because of the lower bandwidth of the digital current controller from this analysis. This explains why the admittance compensation loop is essentially required in the digital PFC control.

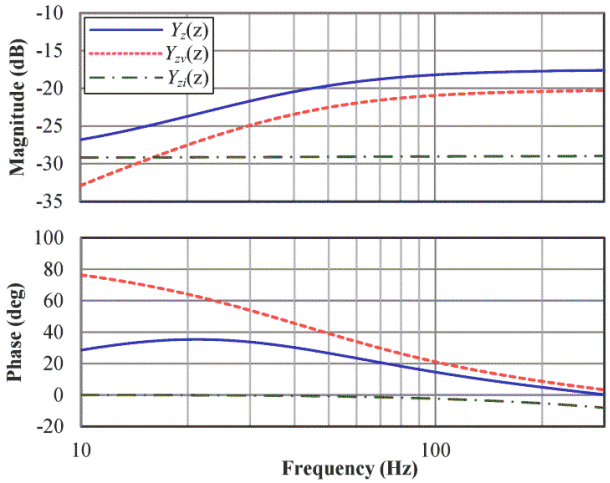


Fig. 5. Frequency responses of the admittance components.

C. Admittance Compensation

The admittance compensation methods have been emphasized in many previous studies [16] – [18]. There are basically two methods, the current reference correction and the duty feed-forward, to compensate the admittance component. Especially, many research papers have been discussed about the duty feed-forward method [14] – [15]. In this paper, the duty feed-forward method as shown in Fig. 7 is employed to compensate the admittance component. Without the duty feed-forward scheme, the input current i_g is

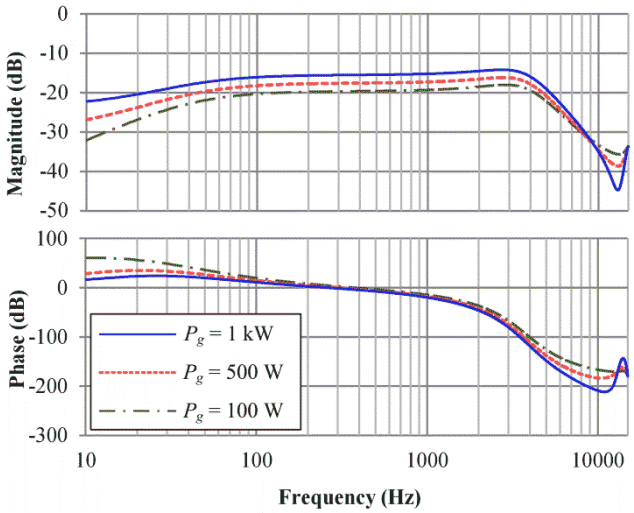


Fig. 6. Frequency responses of the admittance component at the different power levels.

simply written as,

$$i_g(z) = d_{fb}G_{idz}(z) + v_g G_{ivz}(z) \tag{16}$$

In fact, from (2) and (13), there is a relation between $G_{idz}(z)$ and $G_{ivz}(z)$ as below.

$$G_{idz}(z) = V_o G_{ivz}(z) \tag{17}$$

By considering the feed-forward duty d_{ff}, i_g is represented as,

$$\begin{aligned} i_g(z) &= \left(d_{fb} - d_{ff}\right)G_{idz}(z) + v_g G_{ivz}(z) \\ &= d_{fb}G_{idz}(z) - \frac{v_g}{V_o}V_o G_{ivz}(z) + v_g G_{ivz}(z) = d_{fb}G_{idz}(z) \end{aligned} \tag{18}$$

From (18), it can be seen that ideally $G_{ivz}(z)$ is no longer existed in i_g by using d_{ff}. In fact, there is a digital sampling effect which is modeled as the ZOH between the feed-forward duty d_{ff} and the input voltage v_g. However, the sampling frequency is 500 times faster than the fundamental frequency in this paper, and the phase delay effect caused by the ZOH is just 0.036° which can be ignored for the fundamental frequency.

IV. SIMULATION

The simulations were carried out to address the effects of the bandwidth limitation and the admittance component. For the simulation, a simulation software package PSIM was utilized. The same simulation parameters in Table II were also applied. As the feedback controller, the controller in (9) was implemented.

Fig. 8 compares the input phase current and the duty references of the bridgeless PFC converter without and with the admittance compensation. Note that the output voltage and the output power are the same in both of the cases. In Fig. 8(a), the input phase current i_g is severely distorted because of the phase leading current effect which is caused by the

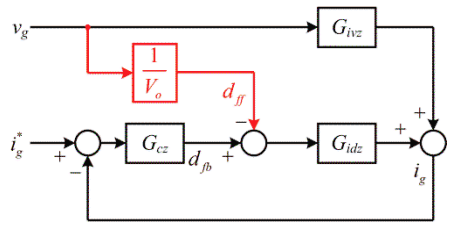
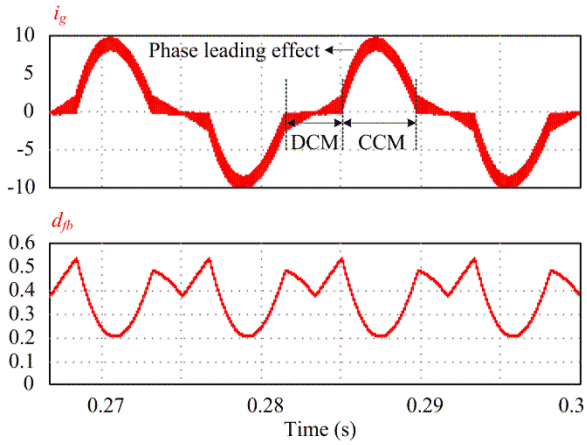
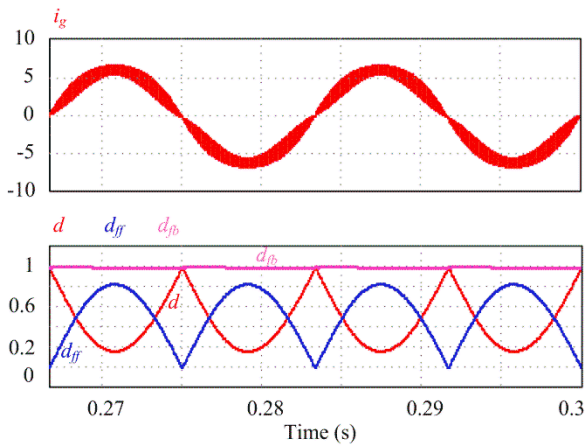


Fig. 7. Duty feed-forward method for admittance compensation.



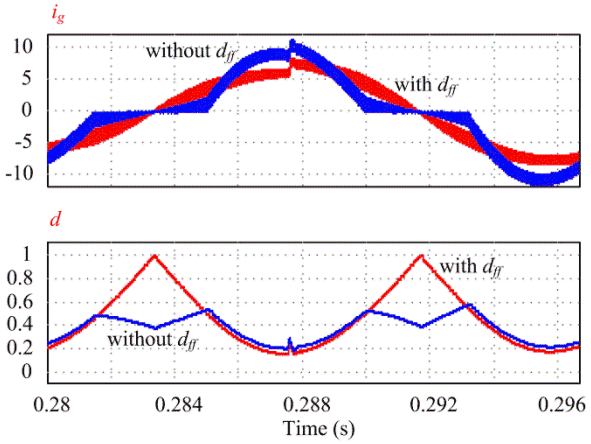
(a)



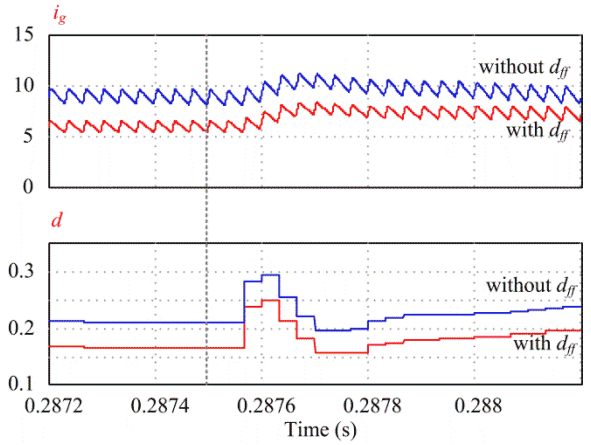
(b)

Fig. 8. Comparison of the simulation results. (a) without the admittance compensation. (b) with the admittance compensation.

admittance component. In the result, the zero crossing points (ZCP) occurred in advance of normal ZCPs. Consequently, the zero current clamping effect is dominant in the current response because of the advanced ZCPs. In addition to this, the system is operated in DCM which deteriorates the input current quality near the ZCPs. Note that the duty reference d_{fb} never reach to 1.0 which is the ideal duty reference near ZCPs of the input voltage. Even if the current is increased so that the system goes into CCM, the shape of the input current is not pure sinusoidal but phase leaded sinusoidal because of the phase leading effect of the admittance component. Fig. 8(b) shows the input current response when both the feedback controller and the admittance compensation strategy are



(a)



(b)

Fig. 9. Comparison of the transient response. (a) normal view. (b) zoomed in view.

applied. As shown in the figure, i_g is well regulated as a sinusoidal shape, and the distortion near the ZCPs are much smaller than in Fig. 8(a). In terms of the duty cycles, the variation of the duty cycle from the feedback control d_{fb} is very small because the feed-forward duty d_{ff} takes most of the required duty variation for the input voltage fluctuation. Consequently, the total duty cycle d to the modulator is mainly reflecting the shape of the inversed d_{ff}. Compared to Fig. 8(b), the maximum amplitude of the input current waveform in Fig. 8(a) is almost 1.5 times higher than the one in Fig. 8(b) even if the operating power is the same. Accordingly, it requires higher current rating of the power semiconductors, and increases the cost. Fig. 9 shows the transient responses of the bridgeless PFC converter with and without the admittance compensation. In Fig. 9(a), the current reference is increased by 25 percent in step at t = 0.2875 s. Fig. 9(b) compares the zoomed in waveforms of the input current i_g and the total duty cycle d with and without the admittance compensation. As in Fig. 9(b), the magnitude of the overshoot and the tendency of the duty variance are almost similar in both the cases. This implies that the

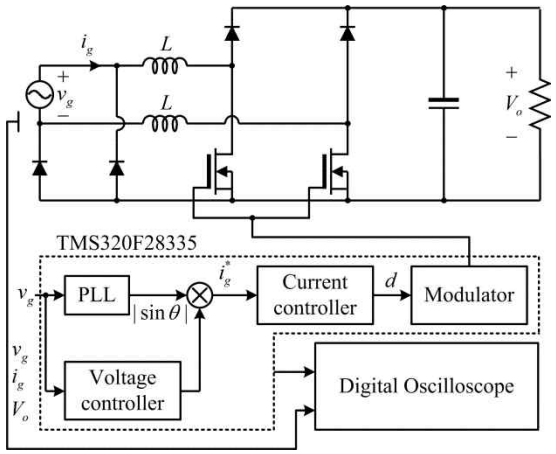
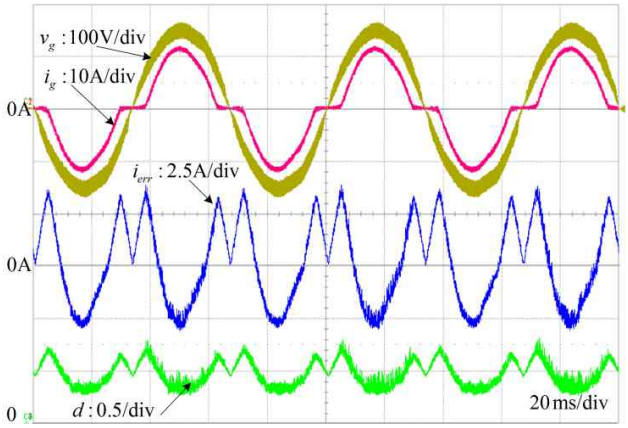


Fig. 10. Experimental setup.

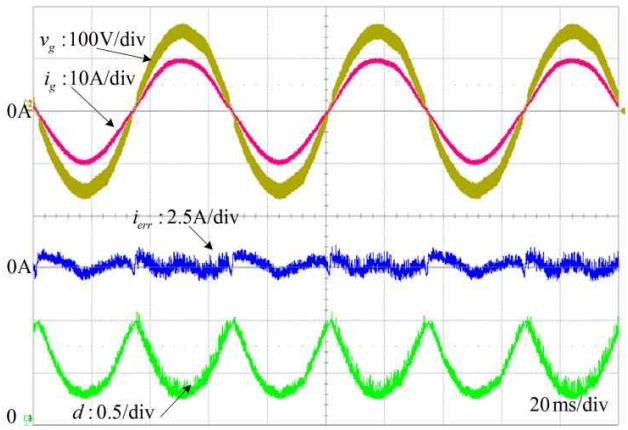
characteristics of the feedback controller in the two control strategies are almost the same. From this, paradoxically, the quality of the input current is mainly determined by the admittance compensation in the digitally controlled bridgeless PFC converter. Regarding the magnitude of the peak current, i_g without the admittance compensation is higher than the case with the admittance compensation, because the input voltage fluctuation acts as a disturbance which may not be compensated by the feedback controller only. Accordingly, the admittance compensation method can be also considered as a feed-forward controller to compensate the predictable disturbance in the view point of the control theory.

V. EXPERIMENTAL RESULTS

In order to verify the analysis taken in this paper, the experiments have been carried out using the bridgeless PFC converter which has the same parameters in Table II. Fig. 10 shows the experimental configuration for the test. The phase locked loop (PLL) algorithm is implemented to generate the sinusoidal reference. To implement the digital control algorithm, Texas Instruments' 32 bit DSP TMS320F28335 has been employed. The DSP board includes the 4 channel digital-to-analog converter (DAC) to monitor the DSP inside variables through the digital oscilloscope. The digital controller derived in (9) has been implemented as the feedback controller for the all experiments. Fig. 11 compares the steady state current waveforms with and without the admittance compensation. In Fig. 11(a), the input current is severely distorted near ZCPs as similar in Fig. 8(a). The maximum current error between the current reference and the actual phase current is around 3.5 A. On the other hand, if the admittance compensation is applied, the shape of the input current becomes more sinusoidal as shown in Fig. 11(b). The distortion near ZCPs is much reduced compare to the previous case. With the admittance compensation, the phase current error ranges within 1.25 A. Fig. 12 compares the step

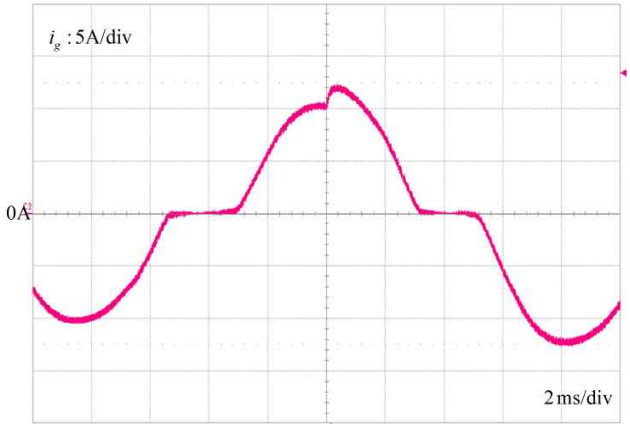


(a)

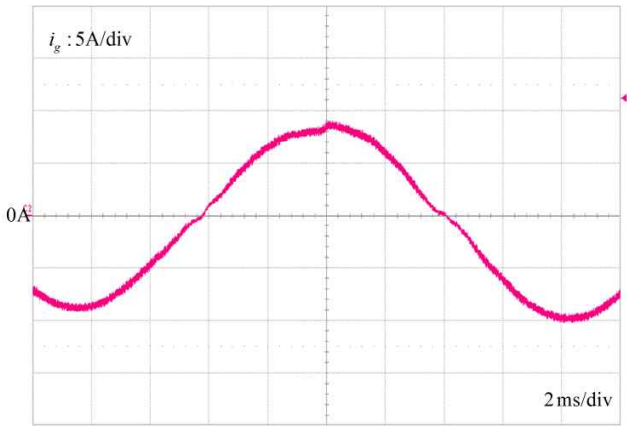


(b)

Fig. 11. Comparison of the experimental results. (a) without the admittance compensation. (b) with the admittance compensation.



(a)



(b)

Fig. 12. Comparison of the step current responses. (a) without the admittance compensation. (b) with the admittance compensation.

current responses without and with the admittance compensation. At t = 0.01 s, the magnitude of the current reference is changed from 8 A to 10 A. In order to be free from the dynamics of the voltage control effect, the current reference itself was changed, and the voltage control loop was not considered. In both of the cases, there are not severe overshoot or ringing at the phase current, and the shapes of the current responses are similar to the simulation results in the previous section. In Fig. 12(a), it is found that the magnitude of the phase current near the peak of the reference always has a current error. This means that the current regulation is not performed very well without the admittance compensation as expected.

VI. CONCLUSION

The limitations of the digital current controller and the admittance component were discussed for the digitally controlled bridgeless PFC converter. The z-domain transfer function of the bridgeless PFC converter was derived. By analyzing the maximum achievable bandwidth of the digital current controller, it had been shown that the phase current distortion which is caused by the admittance component in the control system and the limited bandwidth of the controller is inevitable with the digital feedback controller only. To compensate the admittance component, the duty feed-forward method was discussed. Both the simulation and the experimental results for the 1 kW single-phase bridgeless PFC converter prototype support the analyses in the paper.

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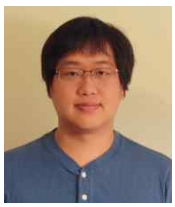

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