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Control Method for Reducing the THD of Grid Current of Three-Phase Grid-Connected Inverters Under Distorted Grid Voltages

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Abstract

This paper proposes a control method for reducing the total harmonic distortion (THD) of the grid current of three-phase grid-connected inverter systems when the grid voltage is distorted. The THD of the grid current caused by grid voltage harmonics is derived by considering the phase delay and magnitude attenuation due to the hardware low-pass filter (LPF). The Cauchy-Schwarz inequality theory is used in order to search more easily for the minimum point of the THD. Both the gain and angle of the compensation voltage at the minimum point of the THD of the grid current are derived with the variation of cut-off frequencies of the hardware LPF. Simulation and experimental results show the validity of the proposed control methods.

Key words: Current control, Grid-connected inverter, Harmonic distortion, Total harmonic distortion (THD)

I. INTRODUCTION

Recently, the demand for renewal energy sources (RESs) such as solar energy, wind energy, and hydrogen energy has dramatically increased in order to reduce the fossil energy. The RESs are normally connected to the utility grid through grid-connected PWM inverters, which supply the active and reactive powers to the main grid [1], [2]. For small distributed grid-connected inverters, an output current control is preferred. Therefore, the most important issue for current controlled grid-connected inverters is that the grid current harmonic regulation is more stringent than that of other power electronics applications. Standards for grid-connected inverters such as IEEE 1547 [3] provide guidance on the levels of total harmonic current distortion. When a grid voltage is distorted, the distorted grid voltage acts as an external disturbance for the grid current control system, resulting in a distorted grid current. The low-order harmonics in the grid current are not attenuated by the natural filtering effect of the grid inductance. As a result, bulky and costly passive filters are required.

One method for suppressing low-order harmonics is to increase the bandwidth of a proportional integral (PI) controller [4]-[6]. Although the current distortion can be reduced as the system bandwidth increases by increasing the proportional and integral gains at the PI controller, the noise immunity of the system is reduced. A proportional resonance (PR) regulator can provide an infinite gain at a selected resonant frequency to reduce the effect of unwanted harmonics [7]-[10]. However, harmonics suppression by a PR regulator is limited to several low-order harmonics. In addition, the system may become unstable when the harmonics to be removed is out of the bandwidth of the system. Another approach for reducing current harmonics is to incorporate the variation of the grid voltage control through an additional feedback path [11]. The suppression ability can be enhanced by increasing the output impedance of the grid-connected inverter.

An inductor current feedback scheme with a feed-forward grid voltage disturbance rejection is proposed for reducing the total harmonic distortion (THD) of the grid current of a three-level inverter with an LCL filter [12]. The selected harmonics of the line current in the active filter can be compensated by using a closed loop current control on the

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synchronous reference frame [13] or by using an indirect reference current generator technique with a selective harmonics compensator [14]. The harmonic currents in a three-phase grid-connected inverter are compensated with the feedforward of selective harmonic grid voltage [15]. These feedforward selective harmonics compensation methods require additional sensing or a large amount of on-line computations. When the number of the selective harmonics increases, the computational cost of both the PR regulator and the feedforward selective harmonics compensation methods also increases.

In this paper, a control method for reducing the THD of the grid current under distorted grid voltages at the three-phase grid-connected inverter is proposed. The THD of the grid current caused by grid voltage harmonics is derived. Then, both the gain and phase angle of the compensation voltage for minimizing the THD of the current are derived. Simulation and experimental results are carried out in order to validate the performance of the control method proposed in this paper.

II. PROPOSED CONTROL METHOD

Fig. 1 shows the current control loop for suppressing the low-order harmonic grid current at the three-phase grid-connected inverter. The *d-q* grid current references can be calculated from the desired active and reactive powers, and PI controllers are used to regulate the *d-q* grid currents. The outputs of the *d-q* grid current controllers ΔV_{gd} and ΔV_{gq}, which denote variations of the inverter voltage, are added to the fundamental *d-q* grid voltages in order to obtain a good dynamic response with the feedforward of the grid voltage. In order to reduce the harmonic grid current, the compensating voltages V_{α_c} and V_{β_c} are added to the α-β reference voltages. A PLL controller is used to synchronize the inverter voltage to the grid voltage.

A hardware low-pass filter (LPF) has been usually used to reduce high frequency noises or ripples at the grid voltage. The transfer function of the hardware LPF is expressed as $1/[1+s/(2\pi f_c)]$, where f_c is the cut-off frequency of the LPF.

The magnitude attenuation and phase delay for the k'th harmonic due to the LPF are expressed as follows.

$$A_{fk} = \frac{1}{\sqrt{1+(f_k/f_c)^2}} \tag{1}$$

$$\theta_{fk} = \tan^{-1}\left(\frac{f_k}{f_c}\right). \tag{2}$$

The filtered grid voltages are used at both the current control system and the PLL controller.

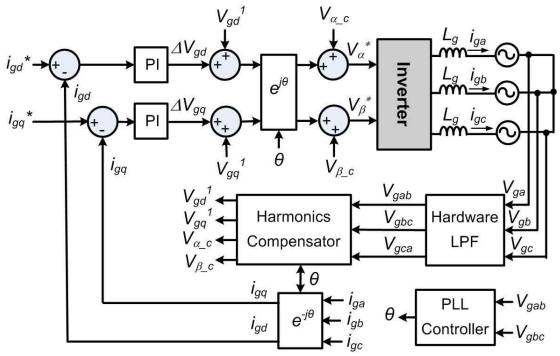


Fig. 1. Current control for suppressing harmonic grid current.

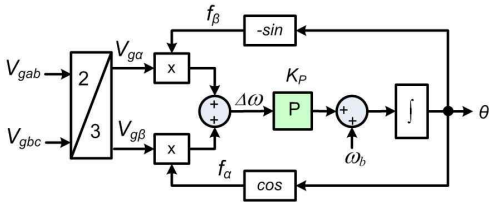


Fig. 2. Block diagram of the PLL controller.

A. PLL Controller

Fig. 2 shows a block diagram of the PLL controller based on the *pq* theory [16], [17], which is used to synchronize the phase of the inverter output voltage with the grid voltage.

In order to synchronize the PLL output angle θ with the grid voltage angle θ_g, the α and β components of the input voltage at the PLL can be calculated from the measured line grid voltages V_{gab} and V_{gbc} through

$$V_{g\alpha} = \frac{2}{3}V_{gab} + \frac{1}{3}V_{gbc} = V_p \cos(\theta_g - \theta_{f1}) \tag{3}$$

$$V_{g\beta} = \frac{1}{\sqrt{3}}V_{gbc} = V_p \sin(\theta_g - \theta_{f1}) \tag{4}$$

where V_p and θ_g are the peak and phase angle of the grid voltage, respectively, and θ_{f1} is a phase angle of the fundamental grid voltage.

The α and β components of the input voltage $V_{g\alpha}$ and $V_{g\beta}$ lag the grid voltage by θ_{f1} due to the hardware LPF. Two feedback signals labeled f_α and f_β are obtained by the cosine and sine of the PLL output angle θ. By the sum of the products of the feedback signals and the α-β input voltages which are the two-axis voltages in the stationary reference frame, a variation of the angular frequency $\Delta\omega$ corresponding to a phase detector (PD) can be expressed as

$$\Delta\omega = V_{g\alpha} \cdot f_\beta + V_{g\beta} \cdot f_\alpha \ . \tag{5}$$

By substituting (3) and (4) into (5), the PD is derived as.

$$\Delta\omega = V_p \cos(\theta_g - \theta_{f1} - \theta) \ . \tag{6}$$

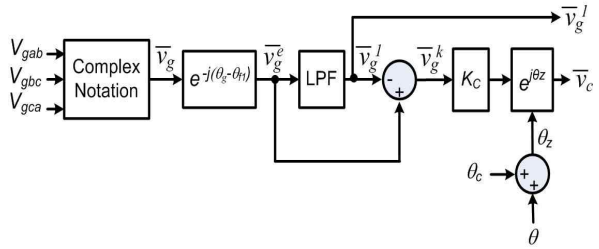


Fig. 3. Block diagram of the harmonics compensator.

Through the *P*-controller, the feedforward of the base angular frequency ω_b=2π×60Hz and an integrator, the PLL output angle θ can be obtained from

$$\theta = \int (K_P \Delta\omega + \omega_b) dt \,. \tag{7}$$

When the PLL output angle θ approaches θ_g-θ_{f1}, the phase is locked.

B. Harmonic Compensation

Fig. 3 shows a block diagram of the harmonics compensator for suppressing the low-order harmonic grid current. Using complex notation, the distorted grid voltage can be expressed as

$$\bar{v}_g = A_{f1} \cdot V_g^1 e^{j(\theta_g - \theta_{f1})} + \sum_{k=5}^{\infty} A_{fK} \cdot V_g^k e^{j(k\theta_g - \theta_{fk})} \,. \tag{8}$$

where $V_g^{\,1}$ is the fundamental voltage, $V_g^{\,k}$ is the *k*'th harmonic voltage, and θ_{fk} is the phase angle of the *k*'th harmonic voltage.

The grid voltage in the synchronous reference frame rotating at (θ_g -θ_{f1}) is given by

$$\bar{v}_g^e = A_{f1} \cdot V_g^1 + \sum_{k=5}^{\infty} A_{fk} \cdot V_g^k e^{j(k\theta_g - \theta_{fk} - \theta_g + \theta_{f1})} \,. \tag{9}$$

where $A_g^{\,1}$ and $A_g^{\,k}$ are the fundamental component and the *k*'th harmonic of the hardware LPF output, respectively.

As shown in Fig. 3, a LPF with a low cut-off frequency is used to pass only the fundamental component of the grid voltage. By subtracting the fundamental voltage from the grid voltage, the harmonic voltages can be extracted from (9), and then it is multiplied by the compensation gain K_c.

$$K_c \cdot \bar{v}_g^k = K_c \cdot \sum_{k=5}^{\infty} A_{fk} \cdot V_g^k e^{j(k\theta_g - \theta_{fk} - \theta_g + \theta_{f1})} \tag{10}$$

In order to eliminate the voltages with a fundamental frequency and to include a compensation angle θ_c in (10), equation (10) is multiplied by $e^{j(\theta g - \theta f1 + \theta c)}$. Thus the compensation voltage v_c is defined as follows, and it is split into the α-β compensation voltages V_{α_c} and V_{β_c}.

$$\bar{v}_c = K_c \cdot \sum_{k=5}^{\infty} A_{fk} \cdot V_g^k e^{j(k\theta_g - \theta_{fk} + \theta_c)} = V_{\alpha\_c} + jV_{\beta\_c} \tag{11}$$

Both the magnitude and phase of the compensation voltage can be adjusted by the gain K_c and the angle θ_c. As shown in Fig. 1, the α-β compensation voltages in the stationary reference frame, V_{α_c} and V_{β_c} are added to the α-β reference voltages at the grid current control loop for reducing the harmonic grid current caused by distorted grid voltages.

III. Compensation Gain and Angle

The compensation gain K_c and angle θ_c are determined on minimizing the THD of the grid current. At first, from Fig. 1, the inverter output voltage vector, v_o can be expressed as

$$\bar{v}_o = \Delta V_g \cdot e^{j\theta} + V_g^1 \cdot e^{j\theta} + \bar{v}_c \tag{12}$$

where ΔV_g is a variation in the grid voltage, which can be obtained from the *d*-*q* current controller outputs in Fig. 1.

By dividing the difference between the inverter output voltage vector and the grid voltage vector by the impedance of the grid-side inductor, the grid current vector is derived as

$$\bar{i}_g = \frac{\bar{v}_o - \bar{v}_g}{Z_{gk}} \tag{13}$$

where the *k*'th harmonic grid impedance, $Z_{gk} = j2\pi f_k L_g$.

By substituting (8) and (12) into (13), the fundamental and harmonic components of the grid current are given by

$$\bar{i}_g^1 = \frac{\Delta V_g \cdot e^{j\theta}}{Z_{g1}} \tag{14}$$

$$\bar{i}_g^k = \frac{\sum_{k=5}^{\infty} V_g^k e^{jk\theta_g} (K_c A_{fk} e^{j(-\theta_{fk} + \theta_c)} - 1)}{Z_{gk}} \tag{15}$$

From (14) and (15), the THD of the grid current is derived as

$$THD = \frac{\left|\bar{i}_g^k\right|}{\left|\bar{i}_g^1\right|} = \sum_{k=5}^{\infty} \frac{V_g^k}{2\pi L_g I_g^1} \cdot \frac{\sqrt{1 + (K_c A_{fk})^2 - 2K_c A_{fk} \cos(-\theta_{fk} + \theta_c)}}{f_k} \,. \tag{16}$$

The Cauchy-Schwarz inequality theory is applied in order to search more easily for the minimum point of the THD [18]. The Cauchy-Schwarz inequality is

$$\left| \sum_{k=1}^{n} x_k y_k \right|^2 \le \sum_{i=1}^{n} \left|x_k\right|^2 \sum_{i=1}^{n} \left|y_k\right|^2 \,. \tag{17}$$

Since the left side of the Cauchy-Schwarz inequality corresponds to the THD in (16), the right side of the Cauchy-Schwarz inequality corresponds to the right side of equation (16) as in

$$\left|x_k\right|^2 = \left| \frac{V_g^k}{2\pi L_g I_g^1} \right|^2 \tag{18}$$

$$\left|y_k\right|^2 = \frac{1 + (K_c A_{fk})^2 - 2K_c A_{fk} \cos(-\theta_{fk} + \theta_c)}{f_k^{\,2}} \,. \tag{19}$$

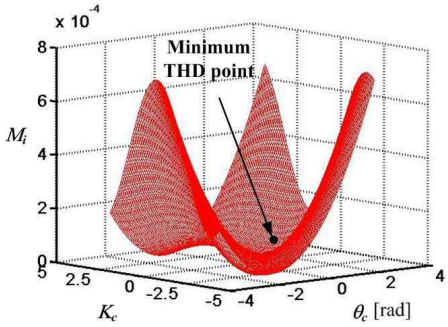
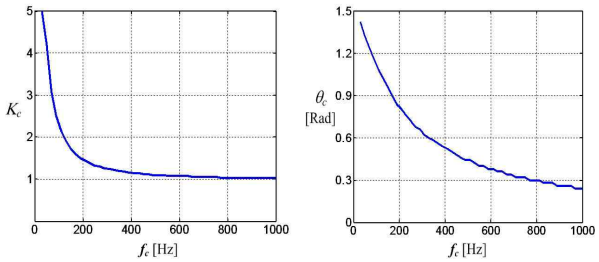


Fig. 4. Converging process to a minimum point of THD.



(a) (b)

Fig. 5. Plots of compensation factors with a variation of f_c : (a) plot of K_c , (b) plot of θ_c.

M_i is defined as

$$M_i = \sum_{k=5}^{\infty} |y_k|^2 = \sum_{k=5}^{\infty} \frac{1+(K_c A_{fk})^2 - 2K_c A_{fk}\cos(-\theta_{fk}+\theta_c)}{f_k^{\,2}} \quad (20)$$

Because the THD has its minimum value when M_i in (20) is minimized, M_i is used instead of the THD. Both the compensation gain K_c and angle θ_c are continuously changed until M_i approaches its minimum value. Finally, the values of K_c and θ_c at the minimum point of M_i can be obtained.

In this paper, the 5th, 7th, and 11th harmonics of the grid current, which are the lowest harmonics in a three-phase grid-connected inverter, are reduced. Fig. 4 shows the converging process to the minimum point of M_i with a variation of both K_c and θ_c at f_c = 500Hz. The cut-off frequency of the hardware LPF is determined by considering the phase delay and magnitude attenuation for the fundamental component of the grid voltage with a 60Hz frequency.

Fig. 5 shows the plots of K_c and θ_c with a variation of the cut-off frequency of the hardware LPF. Both K_c and θ_c are dependent on the cut-off frequency of the LPF, and both of the values decrease as the cut-off frequency increases.

IV. Simulation and Experimental Results

A. Simulation Results

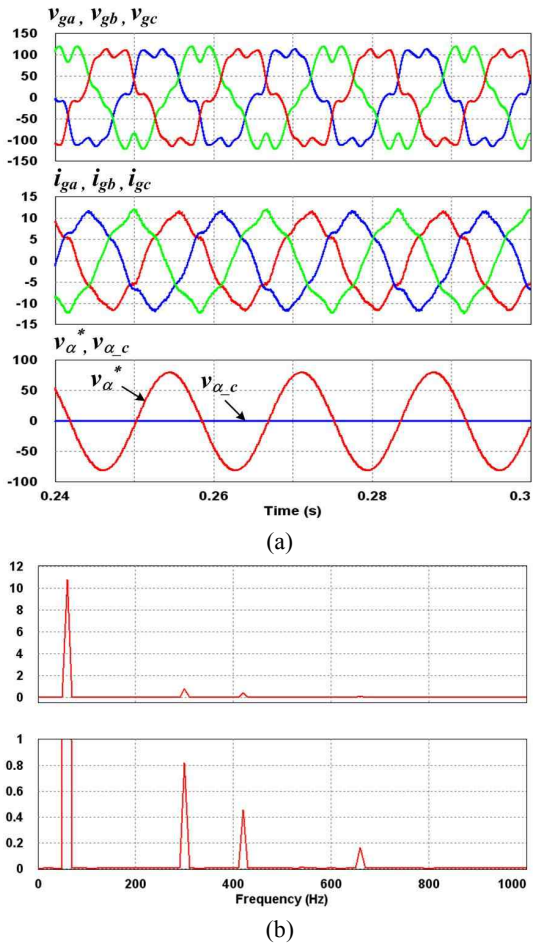
To verify the validity of the proposed control method, a simulation has been performed by using the PSIM program. The circuit rating and parameters used in the simulation and experiment are shown in Table I. Since the cut-off frequency of the hardware LPF is 500Hz, K_c and θ_c are selected as 1.1 and 0.43 rad, respectively, from Fig. 5.

Fig. 6 shows the simulation result without a compensation method. The α-axis reference voltage has a sinusoidal waveform, because the compensation voltage is zero. The grid current has low-order harmonics like the 5th, 7th, and 11th due to the grid voltage harmonics. Therefore, the THD

TABLE I.

System Rating and Parameters

Rated power	3 kVA
Grid voltage (Line-to-Line)	110 V
Grid frequency	60 Hz
DC input voltage	250V
Switching frequency	8 KHz
Grid-side inductance L_g	0.24 mH



(a)

(b)

Fig. 6. Simulation results without compensation method: (a) three-phase grid line voltages and currents, α-axis reference and compensation voltages , (b) FFT analysis of a-phase grid current.

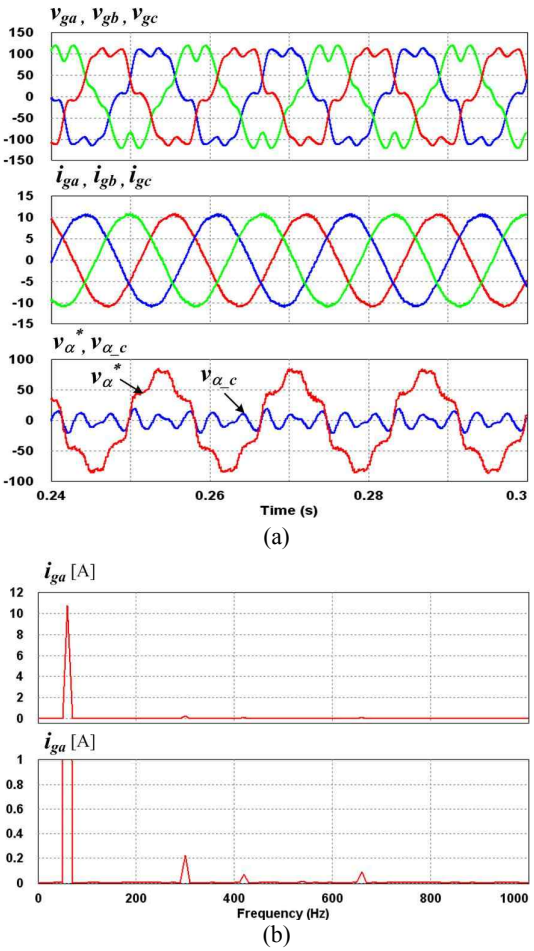


Fig. 7. Simulation results with compensation method: (a) three-phase grid line voltages and currents, α-axis reference and compensation voltages (b) FFT analysis of a-phase grid current.

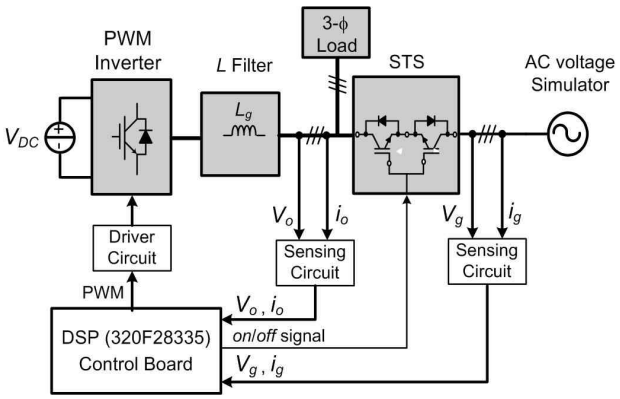


Fig. 8. Hardware configuration.

of the grid current calculated by the FFT analysis is 8.7%.

Fig. 7 shows the simulation results when the compensation method is applied. The α-axis reference voltage is not sinusoidal due to the α-axis compensation voltage. The THD of the grid current is reduced to 2.3%.

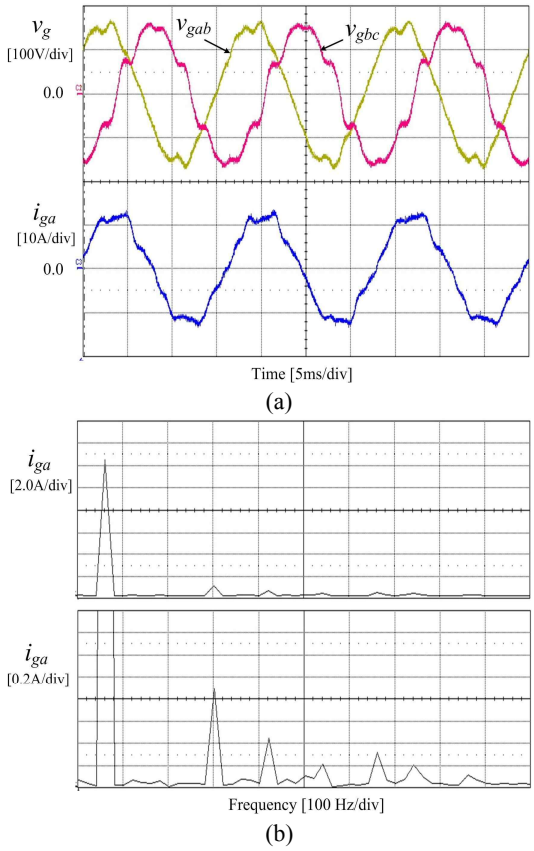


Fig. 9. Experimental results without compensation method: (a) grid line voltages and a-phase grid current, (b) FFT analysis of a-phase grid current.

B. Experimental Results

An experimental test was performed by using a 3kVA prototype three-phase grid-connected inverter in a DSP system based on a TMS320F28335, as shown in Fig. 8. The output voltages and currents of the three-phase PWM inverter and the 3-phase grid voltages and currents are measured and inputted through a 12-bit A/D converter embedded in the DSP. The three-phase AC switch, with two IGBTs per phase connected in anti-serial, is used as the STS. The grid-on/grid–off signal for the AC switch is generated by the DSP controller. A programmable three-phase ac source is used to emulate the main grid voltage as a distorted grid voltage generation.

Fig. 9 shows the experiment results of the grid voltage and current and the results of the FFT analysis of the grid current without the compensation method. Since the grid current has some low-order harmonics like the 5th, 7th, and 11th due to a distorted grid voltage, the measured THD of the current is about 8.5%. Fig. 10 shows the experiment results when the compensation method is applied. It can be seen that the measured THD of the grid current is significantly reduced to 2.8%. Fig. 11 shows the α-axis reference and compensation voltages, and the β-axis reference and compensation voltages

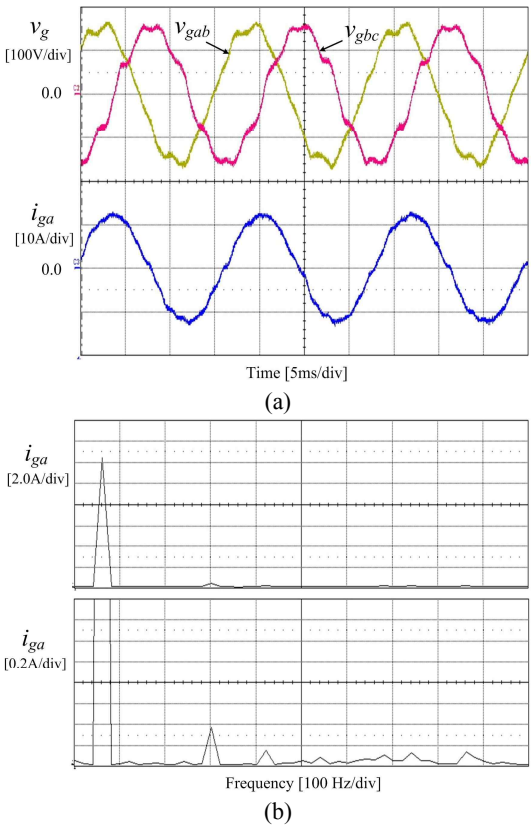


Fig. 10. Experimental results with compensation method: (a) grid line voltages and a-phase grid current, (b) FFT analysis of a-phase grid current.

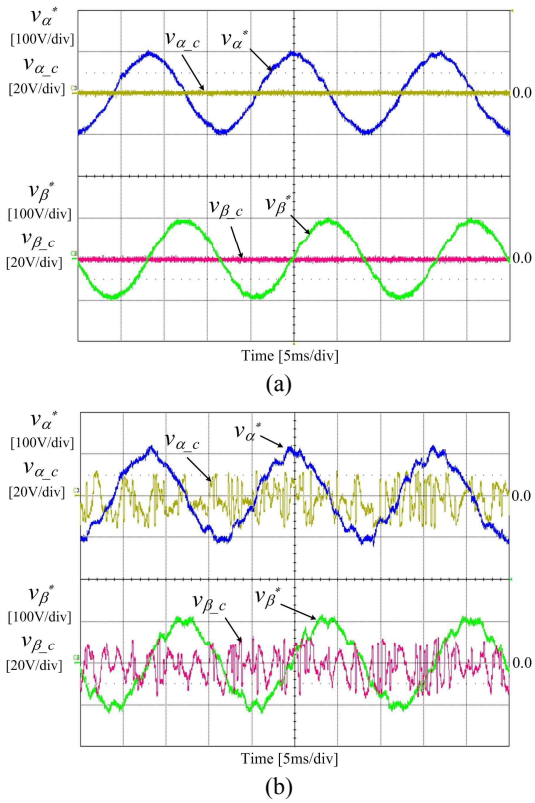


Fig. 11. Waveforms for α-axis reference and compensation voltages, and β-axis reference and compensation voltages: (a) with compensation method, (b) without compensation method.

without and with the compensation method, respectively. As shown in Fig. 11 (a), the α-β reference voltages have a sinusoidal waveform, because the compensation voltages are zero. As shown in Fig. 11 (b), the α-β reference voltage are distorted due to the compensation voltages when the compensation method is used.

V. CONCLUSIONS

This paper proposes a control method for reducing the THD of the grid current under distorted grid voltages in a three-phase grid-connected inverter. The THD of the grid current due to grid voltage harmonics by considering the phase delay and magnitude attenuation due to the hardware LPF is derived. Since the THD can be simplified by using the Cauchy-Schwarz inequality theory, it is easy to search for the minimum point of the THD. Variations in both the gain and phase angle of the compensation voltage for minimizing the THD of the current are investigated according to the cut-off frequency of the hardware LPF. When unwanted harmonics are changed, only the gain and phase angle of the compensation voltage are changed. Simulation and experimental results verify that the THD of the grid current under a distorted grid voltage can be significantly reduced by more than three times, when the proposed compensation method is used.

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