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Low-Cost High-Efficiency PDP Sustaining Driver with a Resonance Bias Level Shift

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Abstract

A highly efficient sustaining driver is proposed for plasma display panels (PDPs). When the PDP is charged and discharged, the proposed sustaining driver employs an address voltage source used in an addressing period. A voltage source is used for fully charging the panel to the sustaining voltage, and an initial inductor current helps the panel discharge to 0 V. The resonance between the panel and an inductor is made by shifting the voltage and current bias level when charging and discharging the panel. As a result, the proposed circuit can reduce power consumption, switching loss, heat dissipation, and production cost. Experimental results of a 42-inch PDP are provided to verify the operation and features of the proposed circuit.

Key words: Energy recovery circuit, Plasma display panel (PDP), Sustaining driver

I. INTRODUCTION

Recently, plasma display panel (PDP) televisions are receiving attention along with a boom in 3D software and contents because PDPs can provide comfortable and realistic 3D images. PDPs are driven with the address display separation method, which has three steps, namely, resetting, addressing, and sustaining [1]. Fig. 1 shows the power flow and driving boards in a PDP. V_b, V_{SET}, and V_{SCAN} are made by V_S in Y and X drivers. In the reset period, many voltages such as V_b, V_{SET}, and V_S are used to initialize the PDP in the Y and X drivers. The address voltage, V_a, (about 70 V) and V_{SCAN}, are also used to make an image on the PDP with an address driver during the addressing step. In the last period, the image is made by the high frequency sustaining voltage, V_S, (about 200 V) rectangular pulse in the Y and X drivers. A logic board controls signals and power flows. Given that the PDP is regarded as a capacitive load (C_p), an energy recovery circuit (ERC) is essential to reduce electromagnetic interference (EMI) noise and considerable energy loss of $fC_pV_s^2$ in the sustaining period. The operating frequency and sustaining voltage are defined by f and V_S, respectively. Many ERCs have been suggested [2]–[12] to relieve the above problem.

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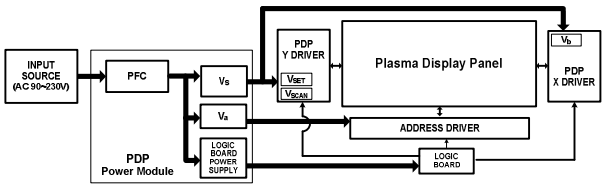


Fig. 1. Power module and driving boards in PDP.

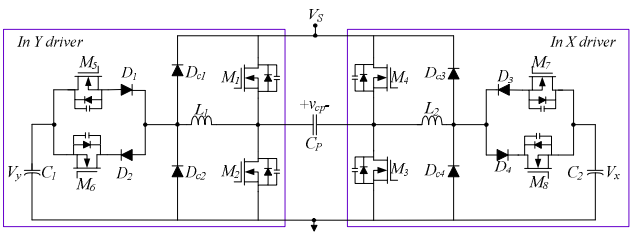
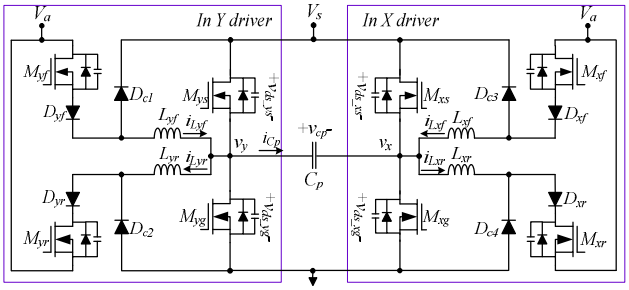
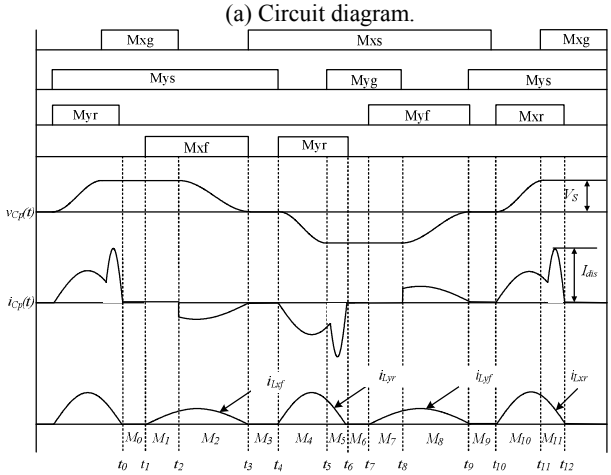


Fig. 2. Circuit diagram of the commercialized ERC.

Fig. 2 shows the commercialized Weber and Wood ERC employed by many PDP companies. Although the Weber and Wood circuit has been employed by many PDP makers, it still has some undesirable drawbacks. When charging and discharging the PDP, parasitic components, such as equivalent series resistor (ESR) and diode forward voltage drop, prevent the panel from being fully charged to V_S and discharged to 0 V [10]–[12]. This scenario results in hard switching operation in all H-bridge inverter switches, excessive surge current, serious power dissipation, EMI noise, and undesirable voltage oscillation across the PDP. As

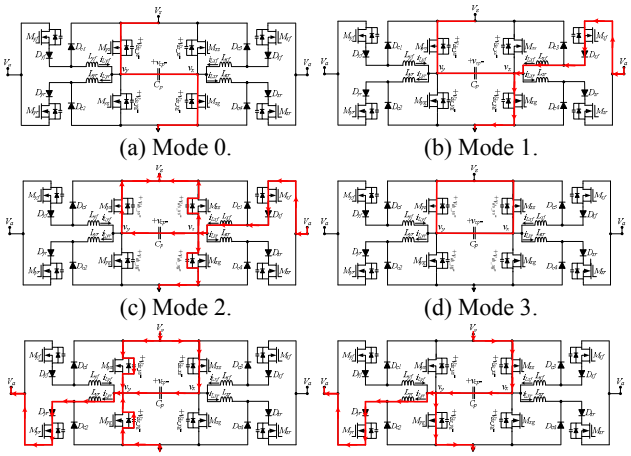


(a) Circuit diagram.



(b) Key waveforms.

Fig. 3. The proposed ERC.



(a) Mode 0. (b) Mode 1.

(c) Mode 2. (d) Mode 3.

(e) Mode 4. (f) Mode 5.

Fig. 4. Current flow diagram of each mode.

worldwide energy regulations for TVs are strengthened, PDP industries have been much more interested in higher efficiency [13]. Therefore, the conventional ERC needs to improve its power conversion efficiency. Furthermore, the voltage source, $V_S/2$, creates a bias level for energy recovery. This voltage is made by the sustaining power supply in the energy recovery capacitor. The energy recovery capacitor is charged or discharged with a large sinusoidal current in high frequency, and the bias voltage has a large ripple. These events result in heat problems in the capacitor, and the unstable voltage source prevents the panel voltage from being charged or discharged fully. To solve these problems, several parallel-connected film capacitors with low ESR must be used. However, this approach increases the cost of production. With the development of large-screen and high resolution PDPs, the drawbacks of these problems could be serious.

To overcome these drawbacks, this paper presents a new ERC by using the address voltage source and the initial inductor current. The proposed ERC has no additional voltage sources because the proposed ERC uses an address voltage as energy recovery bias source. By using the voltage source and current source for charging and discharging the C_p, the energy in the PDP can be fully recovered and injected. Zero-voltage switching (ZVS) is present in switches although some parasitic components, such as parasitic ESR or forward voltage drop of a diode, exist. Better performance can be obtained by dividing the energy recovery path without increasing the number of inductor. Thus, the proposed ERC can have high efficiency, a simple structure, and low cost.

II. The Proposed Circuit and Operational Principle

Fig. 3 shows the circuit diagram and key waveforms of the proposed ERC. The address voltage source, V_a, is used as an energy recovery bias voltage source, and the sustaining voltage source, V_S, is used for gas discharge. Four inductors are employed to improve ERC performance by dividing paths for charging and discharging the PDP [4–5]. An operational principle of the proposed circuit is explained as follows. The circuit operation has 12 modes. However, given that mode 0 to mode 5 and mode 6 to mode 11 are symmetric, mode 0 to mode 5 will only be considered. Fig. 4 shows the current flow from mode 0 to mode 4. V_a is assumed to be less than half of V_S, R_{esr} is a parasitic resistance, and V_{f_on} is a forward drop of a diode.

***Mode 0* (t_0 to t_1)**: M_{ys} and M_{xg} have been turned on and the panel voltage, v_{cp}, is V_S.

***Mode 1* (t_1 to t_2)**: Mode 1 begins when M_{xf} is turned on at t_1. A current of L_{xf} is built up until t_2 with slope of V_a/L_{xf}.

$$i_{Lxf}(t) = \frac{V_a}{L_{xf}}(t - t_1) \tag{1}$$

***Mode 2* (t_2 to t_3)**: When M_{xg} is turned off at t_2, the panel voltage, v_{cp}, is discharged to 0 V by a series resonance between the panel capacitor C_p and the inductor L_{xf} with the built-up current and V_a bias voltage in mode 2. When the panel is discharged, the panel voltage with the parasitic component can be obtained as follows:

$$v_{Cp}(t) = V_S - \left(\frac{I_{Lxf}(t_2)}{\omega C_p}\right) e^{-\frac{t}{\tau}} \sin(\omega t)$$
$$-(V_S - V_a - V_{f\_on})\left[1 - e^{-t/\tau}\left(\cos\omega t + \left(R_{esr} / 2\omega L_{xf}\right)\sin\omega t\right)\right], \tag{2}$$

where $\tau = 2L_{xf} / R_{esr}$ and $\omega = \sqrt{1/L_{xf}C_p - \left(R_{esr} / 2L_{xf}\right)^2}$.

The peak value of the inductor current is smaller than that of the prior circuit because the ERC inductance can be made larger.

***Mode 3* (t_3 to t_4)**: M_{xs} is turned on at t_3, and the panel voltage, v_{cp}, is clamped to 0 V. In this mode, the switch, M_{xs}, can turn on the ZVS condition and the panel can be fully discharged to 0 V. The current source, $i_{Lxf}(t_2)$, can help fully discharge the panel to 0 V without the effect of parasitic components, such as voltage drop of diodes and parasitic ESR.

***Mode 4* (t_4 to t_5)**: Mode 4 is started when M_{ys} is turned off and M_{yr} is turned on. In mode 4, the panel voltage can be charged to V_S by a series resonance of panel capacitor C_p and inductor L_{yr} with the $V_S - V_a$ voltage bias. When the panel is charged, the panel voltage can be expressed as follows:

$$v_{Cp}(t)=(V_S-V_a-V_{f\_on})\left[1-e^{-t/\tau}\left(\begin{matrix}\cos\omega t\\ +\left(R_{esr}/2\omega L_{yr}\right)\sin\omega t\end{matrix}\right)\right] \quad (3)$$

where $\tau = 2L_{yr}/R_{esr}$ and $\omega=\sqrt{1/L_{yr}C_p-\left(R_{esr}/2L_{yr}\right)^2}$.

***Mode 5* (t_5 to t_6)**: After the panel voltage is charged to V_S, M_{yg} is turned on and the gas discharge can occur in mode 5. Given that the voltage source above a half of V_S is used, the panel voltage can be charged fully to Vs and M_{yg}. The switch of the H-bridge inverter can also achieve ZVS even if parasitic components exist. When the remaining current of L_{yr} is decreased to zero, mode 5 is finished. The ERC switch, M_{yr}, and the diode, D_{yr}, are turned off when the remaining inductor current, i_{Lyr}, becomes zero at t_5.

$$i_{Lyr}(t)=i_{Lyr}(t_5)-\frac{V_a}{L_{yr}}(t-t_5) \quad (4)$$

The panel voltage can be fully charged to V_S and discharged to 0 V by using the address voltage and the built-up inductor current sources even though non-idealities, such as synchronous rectifier and forward voltage drop of the ERC diode, are present. The switches of the H-bridge inverter can then achieve ZVS. The switching loss of the diodes and switches in ERC can be reduced because these components are turned off when the inductor current is zero. Furthermore, given that the ERC inductances can be designed to be larger than the conventional inductances, the proposed ERC has smaller peak value and root mean square (RMS) value of the ERC inductor current. Thus, conduction loss can be reduced. By dividing the ERC current paths, we can reduce the power consumption and heat dissipation in ERC devices such as D_{yf}, D_{xf}, M_{yf}, and M_{xf}. A falling transition time from V_S to 0 V can be also made longer than a rising time from 0 V to V_S to obtain reduced power consumption because the transition time is not related to gas discharge. Although the conventional ERC has used an additional film capacitor for making the bias voltage, the proposed circuit has no additional voltage for the ERC without an additional film capacitor. A problem arises when the large sinusoidal current flows to the address voltage source, but the film capacitors

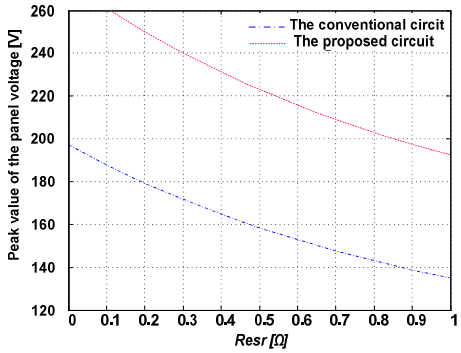
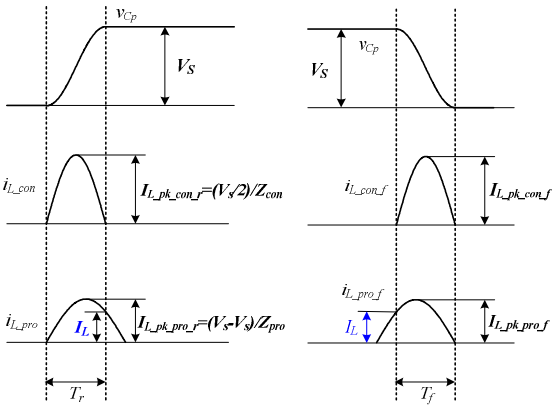


Fig. 5. The peak value of the panel voltage according to the *Resr*: C_p= 80 nF, V_{f_on}=1.0 V, V_S= 200 V, $\Delta T_r = \Delta T_f$= 500 ns.



(a) Ring transition. (b) Falling transition.

Fig. 6. ERC inductor current and the panel voltage during rising and falling transition in the proposed and conventional ERCs.

have already been compensating the pulsating current made in the address period [8]. In addition, the dividing energy recovery path can achieve better performance in the proposed circuit without increasing cost [6]. Thus, the proposed circuit can remove the additional voltage source without increasing the number of film capacitors. The proposed ERC has higher efficiency, better performance, and lower cost compared with conventional ERCs.

III. FEATURES OF THE PROPOSED CIRCUIT

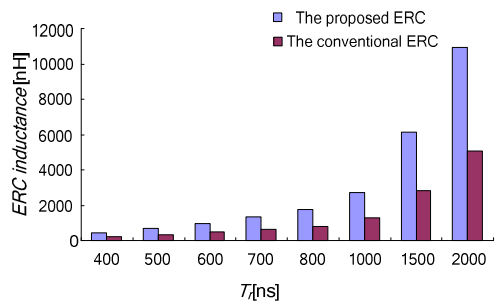
A.ZVS Operation in H-bridge Switches without Considering Parasitic Components

The proposed circuit enables full charging and discharging of the panel by utilizing a voltage source and a current source. Parasitic resistance and diode forward voltage drop are always present in the driving board. These components lead to the failure of energy in the panel capacitor to recover and fed fully. When the panel is charged, the panel voltage with a conventional circuit can be expressed as follows:

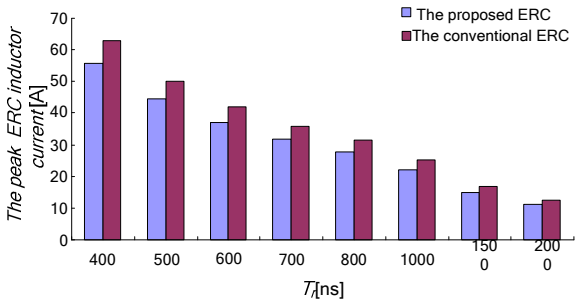
$$v_{Cp\_con}=\left(\frac{V_S}{2}-V_{f\_on}\right)\left[1-e^{-t/\tau}\left(\cos\omega t+\frac{R_{esr}}{2\omega L_1}\sin\omega t\right)\right], \quad (5)$$

where $\tau = 2L_1/R_{esr}$ and $\omega=\sqrt{1/L_1C_p-\left(R_{esr}/2L_1\right)^2}$.

However, the proposed circuit can increase the panel voltage



(a) ERC inductance.



(b) Peak inductor current value.

Fig. 7. ERC inductances and peak inductor current value according to T_r.

to V_S and decrease to 0 V sufficiently. When the panel is charged, the panel voltage can be expressed as follows:

$$v_{Cp\_pro}(t)=(V_S-V_a-V_{f\_on})\left[1-e^{-t/\tau}\left(\begin{matrix}\cos\omega t\\ +\left(R_{esr}/2\omega L_{yr}\right)\sin\omega t\end{matrix}\right)\right], \quad (6)$$

where $\tau=2L_{yr}/R_{esr}$ and $\omega=\sqrt{1/L_{yr}C_p-\left(R_{esr}/2L_{yr}\right)^2}$. If the V_a is 70 V, the peak value of the panel voltage can be illustrated according to the ESR (see Fig. 4). In Fig. 4, the proposed ERC can charge the panel V_S fully despite having parasitic resistors with diode forward voltage drop. Although the parasitic resistance is 0.6 Ω, the panel voltage can be V_S because the resonance voltage bias level is 129 V. Moreover, the panel voltage can be about 220 V. When the panel is discharged, the panel voltage can be reduced to 0 V with a shifting bias current level. Given that the panel is charged and discharged fully, the panel can accomplish zero voltage turn-on of all main power switches M_{ys} to M_{xg}, and the switching loss and EMI problem can be solved.

B.Less Conduction Loss by the Larger ERC Inductance

The peak ERC inductor current value of the proposed ERC is smaller than that of the conventional ERC. Fig. 6(a) shows the ERC inductor current and the panel voltage during rising transition from 0 V to V_S in the proposed and in the conventional ERCs. Considering that the rising time, T_r, is designed to be the same, the peak ERC inductor current values, namely, the $I_{L\_pk\_con\_r}$ of the conventional circuit and

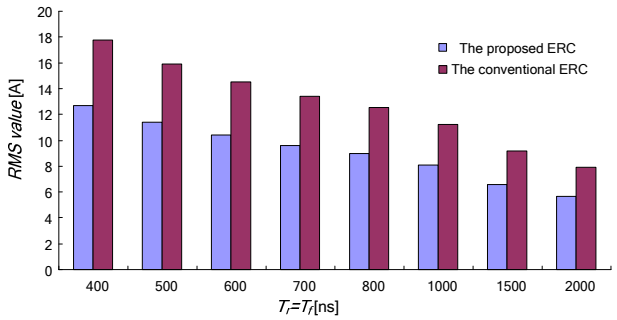


Fig. 8. RMS value of ERC inductor current according to transition time.

the $I_{L\text{-}pk\_pro\_r}$ of the proposed circuit, can be defined as follows:

$$I_{L\_pk\_con\_r}=\frac{V_S}{2Z_{con}} \quad (7)$$

$$I_{L\_pk\_pro\_r}=\frac{\left(V_S-V_a\right)}{Z_{pro}}, \quad (8)$$

where $Z_{con}=\sqrt{L_{cov\_r}/C_p}$ and $Z_{pro}=\sqrt{L_{pro\_r}/C_p}$ without considering parasitic components. The ERC inductances L_{con_r} of the conventional circuit and L_{pro_r} of the proposed circuit are designed with desired T_r:

$$L_{con\_r}=\left(\frac{T_r}{\pi}\right)^2\frac{1}{C_p} \quad (9)$$

$$L_{pro\_r}=\left(\frac{T_r}{\cos^{-1}\left(V_a/\left(V_a-V_s\right)\right)}\right)^2\frac{1}{C_p}. \quad (10)$$

During the falling transition with the same rising time, the inductances, such as L_{con_f} of the conventional circuit and L_{pro_f} of the proposed circuit, are designed for the desired T_f:

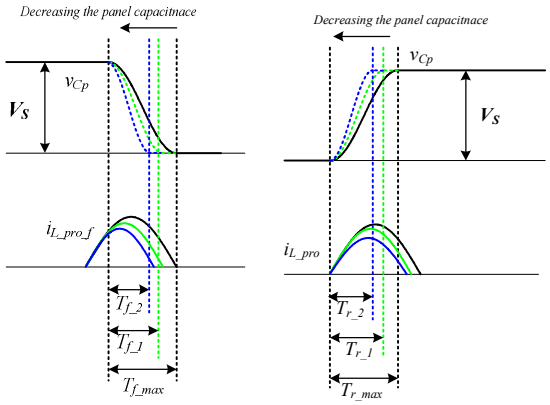
$$L_{con\_f}=\left(\frac{T_f}{\pi}\right)^2\frac{1}{C_p} \quad (11)$$

$$L_{pro\_f}=\left(\frac{T_r}{\cos^{-1}\left(V_a/\left(V_a-V_s\right)\right)}\right)^2\frac{1}{C_p}. \quad (12)$$

As shown in Fig. 6(b), the inductor current is built up in the proposed ERC before the transition time, whereas simple resonance is made during the transition time in the conventional ERC. The peak ERC inductor current values, such as $I_{L\_pk\_con\_f}$ of the conventional circuit and $I_{L\text{-}pk\_pro\_f}$ of the proposed circuit, can be defined in the falling time as follows:

$$I_{L\_pk\_con\_f}=I_{L\_pk\_con\_r}=\frac{V_S}{2Z_{con}} \quad (13)$$

$$I_{L\_pk\_pro\_f}=\frac{\left(V_S-V_a\right)}{Z_{pro}}. \quad (14)$$



(a) Falling transition time. (b) Rising transition time.

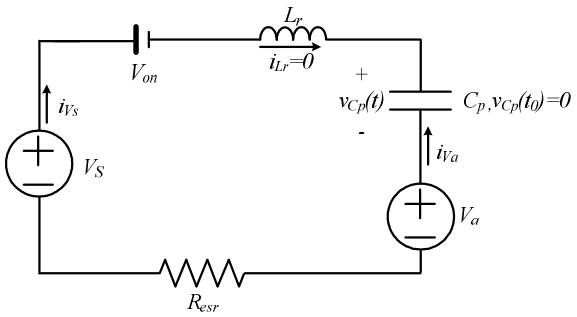
Fig. 9. Transition time variation according to panel capacitance.

If the falling time is the same in the conventional and the proposed ERC, the inductances and peak ERC inductor current values are the same as those in the case of the rising time. If the falling time is equal to the rising time, the initial current value has to be equal to the inductor current when the panel voltage is charged to V_S (see Fig. 7). Furthermore, given that the falling time is designed to be longer than the rising time in the proposed ERC, the peak inductor current value in the proposed ERC is much smaller than that of the conventional ERC. Waveforms of the inductor currents are of a sinusoidal shape. Given that the peak value of the inductor current is small, its RMS value is likewise small. Fig. 8 shows the RMS value of ERC inductor currents with the same transition time in the proposed and conventional circuits during a half switching cycle. The RMS value of all the inductor currents in the conventional and proposed ERC can be obtained as follows:

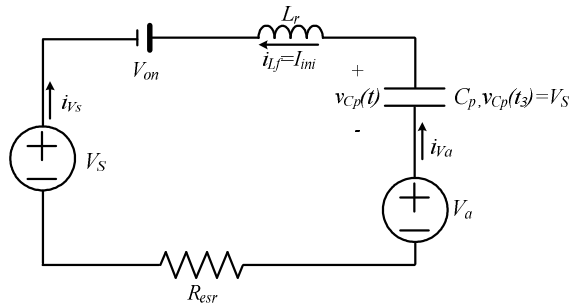
$$I_{RMS\_all\_L\_cov}=\sqrt{\frac{1}{T_s}\left(\int_0^{T_r} {I_{L\_pk\_cov}}^2 sin^2(\omega_r t)dt + \int_{T_s/2-T_f}^{T_s/2} {I_{L\_pk\_cov}}^2 sin^2\left(\omega_r\left(t-T_s/2+T_f\right)\right)dt\right)} = I_{L\_pk\_cov}\sqrt{\frac{T_r}{T_s}} \quad (15)$$

$$I_{RMS\_all\_L\_pro}=\sqrt{\frac{1}{T_s}\int_0^{T_m} {I_{L\_pk\_pro}}^2 sin^2(\omega_r t)dt} = I_{L\_pk\_pro}\sqrt{\frac{T_m}{2T_s}}, \quad (16)$$

where T_s is the switching period, T_r is the rising time, T_f is the falling time, and w_r is the resonant frequency. Fig. 8 shows the RMS value in the proposed and conventional ERC according to the transition time with T_r=T_f and T_s=200 kHz. As shown in Fig. 8, the RMS value of the inductor currents of the proposed ERC is smaller than that of the conventional circuit. In the commercial case with 400 ns transition time,

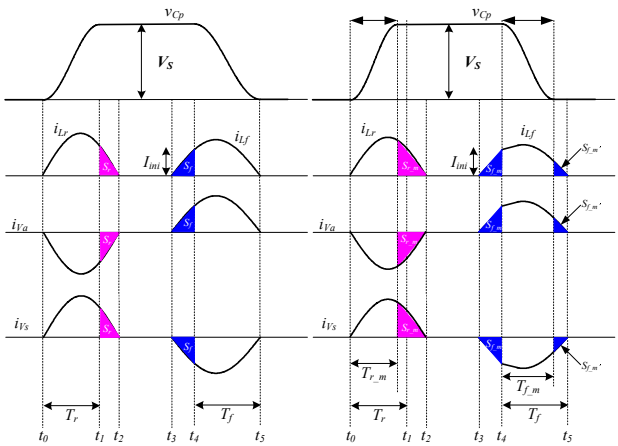


(a) Charging the panel.



(b) Discharging the panel.

Fig. 10. Equivalent circuit during energy recovery operation.

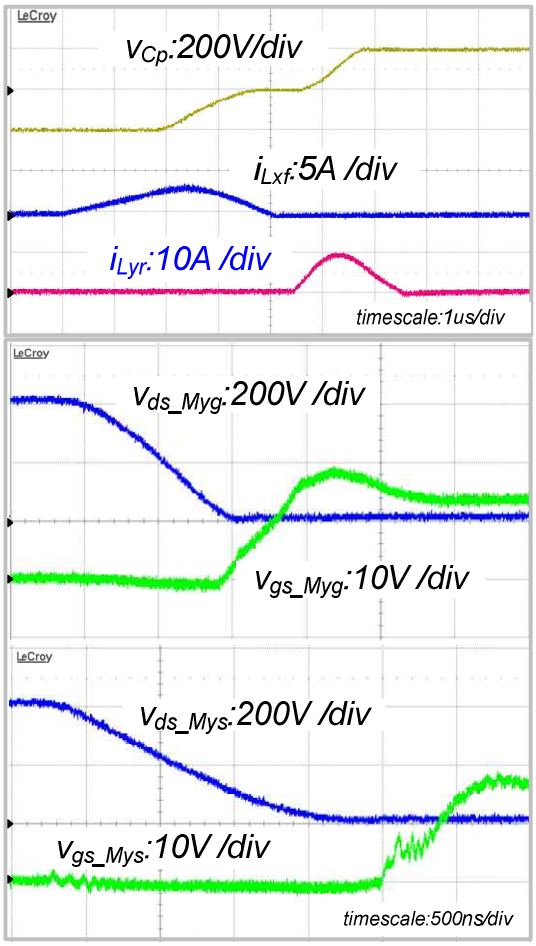


(a) In the largest panel capacitance. (b) In the smallest panel capacitance.

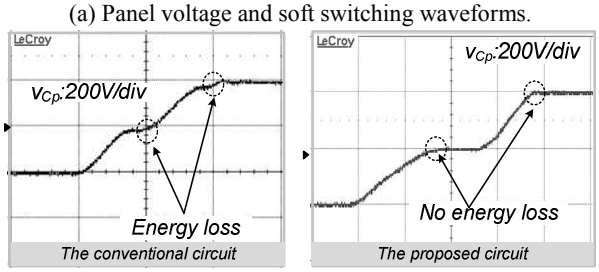
Fig. 11. Panel voltage and current waveforms.

the RMS value of the inductor current is smaller in the proposed ERC to enable the reduction of power consumption in the switches and the parasitic resistor. If the falling time is designed to be slow, the RMS values of the falling inductor currents will be much smaller, so the power consumption can be reduced further.

C.Equilibrium State of the Address Voltage Source



(a) Panel voltage and soft switching waveforms.



(b) Comparison of the panel voltage.

Fig. 12. Experimental waveforms.

Panel capacitance is changed according to the displayed image [14], [15]. Fig. 9 shows that the transition time changes because the panel capacitance is varied by the image. ERC inductance should be designed to satisfy T_{r_max} and T_{f_max} for the largest panel capacitance by trial and error. Although the panel capacitance is varied according to the image, the equilibrium state of the address voltage is not destroyed because the quantity of flow in the address voltage is the same in every switching cycle. Fig. 10 shows an equivalent circuit during charging and discharging of the panel. Although the bias voltage is $V_S - V_a$ when charging the panel, the initial current helps the energy in the panel to be recovered in discharging. Fig. 11 represents the currents of the address and the sustain voltage source during energy recovery operation in the largest panel capacitance and the smallest panel capacitance. The energy for charging the panel is equal to that of discharging the panel. As such, the energy is the same between flowing out and into the address voltage source during one switching cycle, and the equilibrium state is not broken. As shown in Fig. 11(a), ERC inductance is designed to satisfy the transition time in the case of the largest panel capacitance. The remaining energy of the ERC inductor after charging the panel is the same as the built-up current energy at t_4 before discharging the panel. The area of S_r is equal to the energy transferred from V_S to V_a, and the area of S_f is equal to the energy delivered from V_a to V_S. To complete the energy recovery operation perfectly, the two transferred energies have to be the same:

$$\text{Area of } S_r = \text{Area of } S_f. \tag{17}$$

Therefore, the equilibrium state of V_a is not broken, and the V_a voltage source is not changed. When the panel capacitance is reduced according to the image, the transition time becomes shorter than normal (see Fig. 11(b)). When the rising transition time is shorter, the remaining energy of the ERC inductor is larger than that of the normal state, and the energy transferred from V_S to V_a is increased. Although the panel capacitance is reduced, the built-up time of the ERC inductor is the same. Thus, the initial current is not changed when discharging the panel. Given that the panel capacitance is reduced, the falling transition time is shorter and the ERC current remains after discharging the panel (see Fig. 11(b)). The remaining energy is transferred only from V_a to V_S because the additional energy is accumulated in V_a during the rising transition time.

$$\text{Area of } S_{r\_m} = \text{Area of } S_{f\_m} + \text{Area of } S_{f\_m} \tag{18}$$

Eq. (17) shows that energy is always the same; thus, the equilibrium state of the Vs is not changed even though panel capacitance is varied by the image. Given that V_a is not decreased or increased, the reliability of the data driver IC is not a problem.

D.Design of Rising and Falling Inductance

To reduce the reactive power loss and to obtain good gas discharge uniformity, the inductances of L_{yr}, L_{xr}, L_{yf}, and L_{xf} are designed by considering the rising and falling time of sustaining pulse. To obtain the desired rising time $T_r(t_4 \sim t_5 = t_{10} \sim t_{11})$ and falling time $T_f(t_2 \sim t_3 = t_8 \sim t_9)$, the inductors are selected as follows:

$$L_{yr} = L_{xr} = \frac{1}{C_p}\left(\frac{T_r}{\cos^{-1}\left[1 - V_S/(V_S - V_a)\right]}\right)^2, \tag{19}$$

where δT ($t_1 \sim t_2 = t_7 \sim t_8$) and $\theta = \tan^{-1}(\sqrt{LC_p}/\delta T)$.

IV. EXPERIMENTAL RESULTS

An experiment of the proposed ERC for verifying operation is performed with a 42-inch PDP, which has about 80 nF of panel capacitance, C_p, in 200 V sustaining voltage, and 70 V address voltage at 50 kHz. The components in this circuit and the conventional circuit are as follows: the H-bridge switches M_{ys}, M_{yg}, M_{xs}, and M_{xg}: IXYS63N25, M_{yr}, M_{yf}, M_{xs}, and M_{xf}: IXYS63N25, diodes: 30CPF06, the inductor L_{yr}=L_{xr} for T_r(t_4~t_5)=1.5 μs: 9 μH, the inductor L_{yf}=L_{xf} for T_f(t_2~t_3) = 2.5 μs: 45 μH considering gas discharge and power loss. Fig. 12 shows the experimental results. Fig. 12(a) shows that v_{cp} is charged from 0 V to V_S and discharged from V_S to 0 V fully. Before the panel is discharged, the currents of L_{xf} and L_{yf} are built up to compensate for the parasitic components. After the panel is charged, the energy of the inductor is sufficient to overcome the effect of the parasitic components as the currents of L_{xr} and L_{yr} remain. Fig. 12(a) shows waveforms of soft switching in the H-bridge inverter switches. The switches in the H-bridge inverter achieve ZVS (see Fig. 12(a)). The conventional circuit experiences energy loss when charging and discharging the panel. By contrast, the proposed circuit has no energy loss (see Fig. 11(b)). The energy recovery efficiency can be defined as follows:

$$\eta = \frac{P_{ow} - P_o}{P_{ow}}, \tag{20}$$

where P_{ow} is the power consumption without ERC, and P_o is the power consumption with ERC. Fig. 13 shows the energy recovery efficiency of the proposed ERC and the conventional Weber and Wood ERC according to the sustaining voltage. When the built up time is 1.5 μs, the panel is not discharged to 0 V fully, and the conduction loss is large. Therefore, the efficiency is less than those of the prior circuit in 200 V sustaining voltage. The proposed ERC is noted to have more than 97% energy recovery efficiency. The proposed circuit has less power consumption with the 2 μs built-up time for discharging the panel than the conventional circuit does during energy recovery operation. Therefore, experimental waveforms and results coincide with the theoretical key waveforms and features of the proposed ERC.

V. CONCLUSIONS

A cost effective and high performance ERC has been proposed in this paper. The proposed ERC has used two sources, namely, the voltage source and the current source, to obtain energy recovery operation. The panel voltage can be fully charged to V_S and discharged to 0 V. The switches of the H-bridge inverter can achieve ZVS even if parasitic components exist. Moreover, the proposed ERC has low cost because of the lack of an additional ERC voltage source. The proposed ERC can obtain high efficiency and performance by dividing the recovery path. Experimental results based on the 42-inch PDP are provided to verify the effectiveness of the proposed ERC.

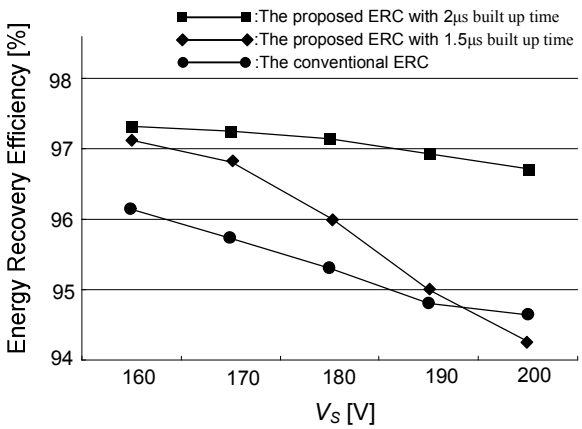


Fig. 13. The energy recovery efficiency.

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