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New Three-Phase Multilevel Inverter with Shared Power Switches

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Abstract

Despite the advantages offered by multilevel inverters, one of the main drawbacks that prevents their widespread use is their circuit complexity as the number of power switches employed is usually high. This paper presents a new multilevel inverter topology with a considerable reduction in the number of power switches used through the switch-sharing approach. The fact that the proposed inverter applies two bidirectional power switches for sharing among the three phases does not prevent it from producing seven levels in the line-to-line output voltage waveforms. A modified scheme of space vector modulation via the application of virtual voltage vectors is developed to generate the PWM signals of the power switches. The performance of the proposed inverter is investigated through MATLAB/SIMULINK simulations and is practically tested using a laboratory prototype with a DSP-based modulator. The results demonstrate the satisfactory performance of the inverter and verify the effectiveness of the modulation method.

Key words: Bidirectional switches, Digital Signal Processor (DSP), Multilevel inverter, Space vector modulation, Virtual vector

I. INTRODUCTION

In renewable energy generation systems such as photovoltaic (PV) systems, the inverter has become the most important component as it converts the DC power from the PV modules into AC power to be fed to the grid. The inverter also plays a significant role in electric motor drive systems especially in variable speed drives (VSD) where a considerable level of energy saving can be accomplished. These drives ensure that electric machines consume only the required amount of energy for the conducted tasks, hence reducing power loss and improving overall efficiency.

A common topology for the inverters applied in such systems is the conventional full-bridge configuration. In PV systems for instance, although the inverter can meet the specifications needed via a very high switching operation, it also increases the switching loss, acoustic noise and level of interference to other equipment [1]. In motor drive systems, the current distortion which results from non-sinusoidal voltage reduces the motor efficiency and introduces undesirable vibrating torque. In addition, the high dv/dt stress exposes the motor insulation to the risk of breakdown [2]. A promising solution to these problems has been proposed with the introduction of the multilevel inverter.

Multilevel inverters offer improved quality in terms of output waveforms with a lower total harmonic distortion and a better harmonic spectrum, which then leads to a reduction in the filter's size. In addition, decreases in the level of electromagnetic interference, in the switching loss and in the dv/dt stress can also be achieved [3]-[5]. A number of circuit topologies have been proposed and many modulation and control techniques have been developed to accommodate their potential widespread utilization in industrial applications.

There are three well-known multilevel topologies which have been continuously investigated namely the diode-clamped inverter, the capacitor-clamped inverter and the cascaded H-bridge inverter [6]. The most common modulation strategies applied to these topologies include the selective harmonic elimination [7], the carrier-based pulse width modulation [8] and the space vector pulse width modulation [9]. In a search for more innovative designs, recent studies have introduced modifications to the existing topologies [10]-[12]. Other studies have introduced combinations of various low and high switching frequencies to develop hybrid control methods [13], [14].

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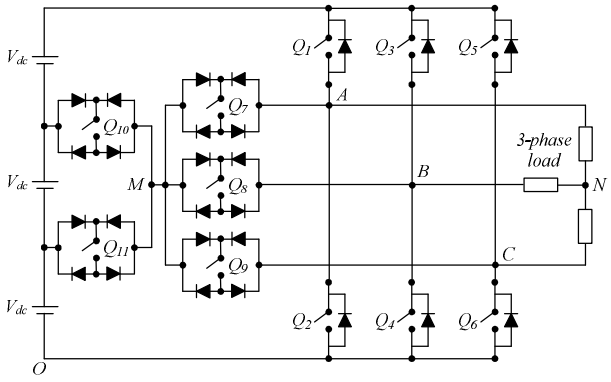


Fig. 1. Circuit topology of the proposed three-phase multilevel inverter.

The tendency and motivation for conducting research on new topologies and control strategies are mainly due to the multilevel circuit's complexity. These circuits usually involve a high number of power switches that need to be properly controlled by an effective and efficient controller. One way to ease this complexity is by reducing the number of power switches through the use of more power diodes. This can be realized by using bidirectional switches which have been employed in single-phase modified H-bridge multilevel inverters [15]-[18]. The inverter comprises a typical single-phase H-bridge circuit configuration with a bidirectional switch to produce five output voltage levels. In another recent publication, this circuit topology has been extended to generate seven voltage levels by inserting an additional bidirectional switch [1]. Based on the modified single-phase five-level H-bridge topology, a cascaded three-phase structure was proposed [19].

This paper presents a new three-phase multilevel inverter topology based on the modified full-bridge configuration with bidirectional-switch-sharing capability. The next section provides the details of the proposed topology. Towards the end of this paper, the modulation strategy and a power loss analysis are described. The subsequent sections discuss the simulation and experimental results under balanced and unbalanced load conditions. Finally, conclusions are drawn in the last section.

II. THE PROPOSED TOPOLOGY

Fig. 1 shows the circuit topology of the proposed three-phase multilevel inverter. The circuit is formed from the combination of the conventional three-phase full-bridge configuration with five bidirectional switching devices arranged in the manner shown in the figure. The proposed inverter is able to produce seven voltage levels in the line-to-line output voltage waveforms of the following amplitudes: $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, V_{dc}, $2V_{dc}$, $3V_{dc}$ and 0. To generate the seven voltage levels at a low switching frequency, the inverter has to operate according to the following 18 operational modes below:

Mode 1 ($V_{AB} = 0$, $V_{BC} = -3V_{dc}$, $V_{CA} = 3V_{dc}$): Q_2 is on, linking node A to the ground; Q_4 is on, linking node B to the ground; and Q_5 is on, linking node C to $3V_{dc}$. All of the other switches are off. Fig. 2(a) shows the current path during this mode.

Mode 2 ($V_{AB} = V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = 2V_{dc}$): Q_7 and Q_{11} are on, linking node A to V_{dc}; Q_4 is on, linking node B to the ground; and Q_5 is on, linking node C to $3V_{dc}$. All of the other switches are off. Fig. 2(b) shows the current path during this mode.

Mode 3 ($V_{AB} = 2V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = V_{dc}$): Q_7 and Q_{10} are on, linking node A to $2V_{dc}$; Q_4 is on, linking node B to the ground; and Q_5 is on, linking node C to $3V_{dc}$. All of the other switches are off. Fig. 2(c) shows the current path during this mode.

Mode 4 ($V_{AB} = 3V_{dc}$, $V_{BC} = -3V_{dc}$, $V_{CA} = 0$): Q_1 is on, linking node A to $3V_{dc}$; Q_4 is on, linking node B to the ground; and Q_5 is on, linking node C to $3V_{dc}$. All of the other switches are off. Fig. 2(d) shows the current path during this mode.

Mode 5 ($V_{AB} = 3V_{dc}$, $V_{BC} = -2V_{dc}$, $V_{CA} = -V_{dc}$): Q_1 is on, linking node A to $3V_{dc}$; Q_4 is on, linking node B to the ground; and Q_9 and Q_{10} are on, linking node C to $2V_{dc}$. All of the other switches are off. Fig. 2(e) shows the current path during this mode.

Mode 6 ($V_{AB} = 3V_{dc}$, $V_{BC} = -V_{dc}$, $V_{CA} = -2V_{dc}$): Q_1 is on, linking node A to $3V_{dc}$; Q_4 is on, linking node B to the ground; and Q_9 and Q_{11} are on, linking node C to V_{dc}. All of the other switches are off. Fig. 2(f) shows the current path during this mode.

Mode 7 ($V_{AB} = 3V_{dc}$, $V_{BC} = 0$, $V_{CA} = -3V_{dc}$): Q_1 is on, linking node A to $3V_{dc}$; Q_4 is on, linking node B to the ground; and Q_6 is on, linking node C to the ground. All of the other switches are off. Fig. 2(g) shows the current path during this mode.

Mode 8 ($V_{AB} = 2V_{dc}$, $V_{BC} = V_{dc}$, $V_{CA} = -3V_{dc}$): Q_1 is on, linking node A to $3V_{dc}$; Q_8 and Q_{11} are on, linking node B to V_{dc}; and Q_6 is on, linking node C to the ground. All of the other switches are off. Fig. 2(h) shows the current path during this mode.

Mode 9 ($V_{AB} = V_{dc}$, $V_{BC} = 2V_{dc}$, $V_{CA} = -3V_{dc}$): Q_1 is on, linking node A to $3V_{dc}$; Q_8 and Q_{10} are on, linking node B to $2V_{dc}$; and Q_6 is on, linking node C to the ground. All of the other switches are off. Fig. 2(i) shows the current path during this mode.

Mode 10 ($V_{AB} = 0$, $V_{BC} = 3V_{dc}$, $V_{CA} = -3V_{dc}$): Q_1 is on, linking node A to $3V_{dc}$; Q_3 is on, linking node B to $3V_{dc}$; and Q_6 is on, linking node C to the ground. All of the other switches are off. Fig. 2(j) shows the current path during this mode.

Mode 11 ($V_{AB} = -V_{dc}$, $V_{BC} = 3V_{dc}$, $V_{CA} = -2V_{dc}$): Q_7 and Q_{10} are on, linking node A to $2V_{dc}$; Q_3 is on, linking node B to $3V_{dc}$; and Q_6 is on, linking node C to the ground. All of the other switches are off. Fig. 2(k) shows the current path during this mode.

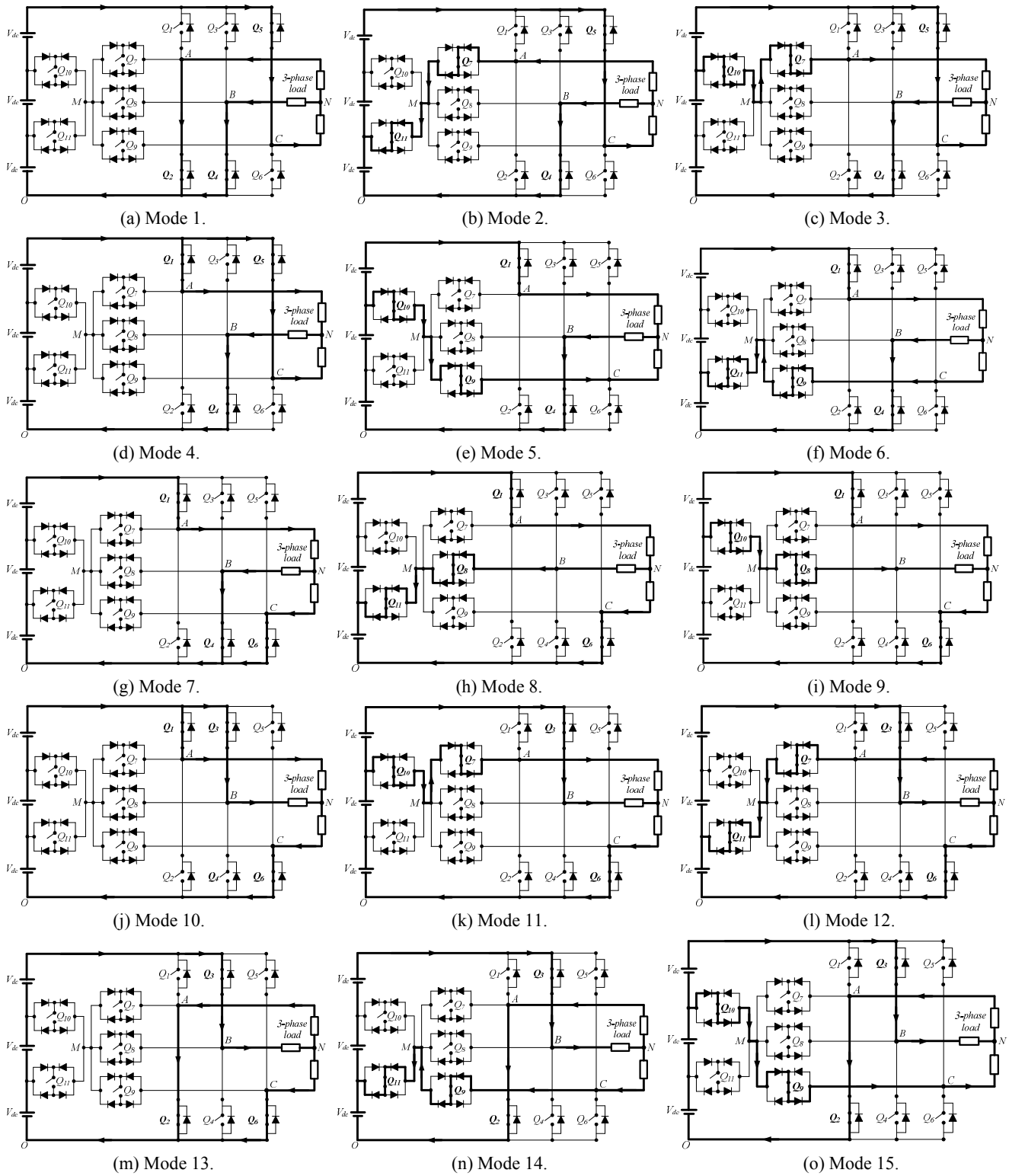
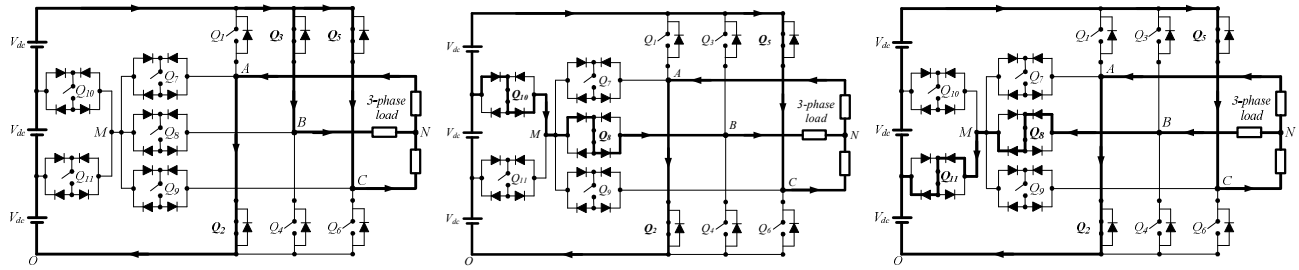


Fig. 2. Operational modes to generate seven voltage levels in the line-to-line output voltage waveforms at low switching frequency operation.

Mode 12 (V_{AB} = -2V_{dc}, V_{BC} = 3V_{dc}, V_{CA} = -V_{dc}): Q_7 and Q_{11} are on, linking node A to V_{dc}; Q_3 is on, linking node B to 3V_{dc}; and Q_6 is on, linking node C to the ground. All of the other switches are off. Fig. 2(l) shows the current path during this



(p) Mode 16. (q) Mode 17. (r) Mode 18.

Fig. 2. (Continued) Operational modes to generate seven voltage levels in the line-to-line output voltage waveforms at low switching frequency operation.

TABLE I
COMPARISON BETWEEN THE PROPOSED INVERTER AND THE THREE WELL-KNOWN INVERTERS IN TERMS OF THE NUMBER OF DEVICES USED

Multilevel inverter structure	Diode-clamped inverter	Capacitor-clamped inverter	Cascaded H-bridge inverter	Proposed inverter
Main switches	18	18	18	11
Main diodes	18	18	18	26
Clamping diodes	12	0	0	0
Clamping capacitor	0	9	0	0
Total	48	45	36	37

mode.

Mode 13 (V_{AB} = -3V_{dc}, V_{BC} = 3V_{dc}, V_{CA} = 0): Q_2 is on, linking node A to the ground; Q_3 is on, linking node B to 3V_{dc}; and Q_6 is on, linking node C to the ground. All of the other switches are off. Fig. 2(m) shows the current path during this mode.

Mode 14 (V_{AB} = -3V_{dc}, V_{BC} = 2V_{dc}, V_{CA} = V_{dc}): Q_2 is on, linking node A to the ground; Q_3 is on, linking node B to 3V_{dc}; and Q_9 and Q_{11} are on, linking node C to V_{dc}. All of the other switches are off. Fig. 2(n) shows the current path during this mode.

Mode 15 (V_{AB} = -3V_{dc}, V_{BC} = V_{dc}, V_{CA} = 2V_{dc}): Q_2 is on, linking node A to the ground; Q_3 is on, linking node B to 3V_{dc}; and Q_9 and Q_{10} are on, linking node C to 2V_{dc}. All of the other switches are off. Fig. 2(o) shows the current path during this mode.

Mode 16 (V_{AB} = -3V_{dc}, V_{BC} = 0, V_{CA} = 3V_{dc}): Q_2 is on, linking node A to the ground; Q_3 is on, linking node B to 3V_{dc}; and Q_5 is on, linking node C to 3V_{dc}. All of the other switches are off. Fig. 2(p) shows the current path during this mode.

Mode 17 (V_{AB} = -2V_{dc}, V_{BC} = -V_{dc}, V_{CA} = 3V_{dc}): Q_2 is on, linking node A to the ground; Q_8 and Q_{10} are on, linking node B to 2V_{dc}; and Q_5 is on, linking node C to 3V_{dc}. All of the other switches are off. Fig. 2(q) shows the current path during this mode.

Mode 18 (V_{AB} = -V_{dc}, V_{BC} = -2V_{dc}, V_{CA} = 3V_{dc}): Q_2 is on, linking node A to the ground; Q_8 and Q_{11} are on, linking node B to V_{dc}; and Q_5 is on, linking node C to 3V_{dc}. All of the other switches are off. Fig. 2(r) shows the current path during this mode.

Note that switches Q_{10} and Q_{11} are activated to generate the voltage levels of -2V_{dc}, -V_{dc}, V_{dc} and 2V_{dc} for the line-to-line voltage waveforms of the three phases. They are actually shared among the three phases. The switch-sharing capability offered by this inverter further reduces the number of switches, thus it greatly eases the circuit complexity. Table I summarizes a comparison of the number of devices used between the proposed inverter and the three equivalent well-known multilevel inverter topologies. Although the cascaded H-bridge structure appears to use the lowest total number of devices, it still employs a higher number of main switches which then increases the complexity of the control circuit when compared to the proposed topology.

III. ADAPTATION OF SPACE VECTOR PWM

In this paper, a high switching frequency strategy i.e. space vector pulse width modulation (SVPWM) is considered since the low switching frequency methods suffer from the low order voltage harmonics. This is mainly due to the absence of a large number of levels in the line-to-line output voltage waveforms. Referring to Fig. 1, each arm consists of two main power switches and a bidirectional switch. The two bidirectional switches (Q_{10} and Q_{11}) are shared among the three arms. Considering only one arm, say phase A, four switching states can be defined. *State 0* is obtained when Q_2 is on while Q_1, Q_7, Q_{10} and Q_{11} are off which results in V_{AO} = 0. *State 1* is produced when only Q_7 and Q_{11} are on, leading to V_{AO} = V_{dc}. *State 2* is the same as *State 1* except that Q_{10} is on, instead of Q_{11}, contributing to V_{AO}= 2V_{dc}. To get *State 3*, only Q_1 is on, which results in V_{AO} = 3V_{dc}. The same applies for phases B and C. Table II provides the definitions of switching states for the three phases.

TABLE II

DEFINITION OF SWITCHING STATES

		Switching states											
		Phase A (S_A)				Phase B (S_B)				Phase C (S_C)			
		0	1	2	3	0	1	2	3	0	1	2	3
Active switch	Q_1				√								
	Q_2	√											
	Q_3								√				
	Q_4					√							
	Q_5												√
	Q_6									√			
	Q_7		√	√									
	Q_8						√	√					
	Q_9										√	√	
	Q_{10}			√				√				√	
	Q_{11}		√				√				√		
V_{JO}	0	√				√				√			
	V_{dc}		√				√				√		
	$2V_{dc}$			√				√				√	
	$3V_{dc}$				√				√				√

Note: $J = A$ for phase A, $J = B$ for phase B, $J = C$ for phase C

By taking into account the three arms, 46 possible switching state combinations can be generated in the form of $S_AS_BS_C$ in which S_A represents the switching state of arm or phase A, S_B for phase B, and S_C for phase C. The line-to-line and phase output voltages can be represented in terms of the switching states as given in (1) and (2) below:

$$\begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = V_{dc} \begin{bmatrix} S_A - S_B \\ S_B - S_C \\ S_C - S_A \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2S_A - S_B - S_C \\ 2S_B - S_C - S_A \\ 2S_C - S_A - S_B \end{bmatrix} \tag{2}$$

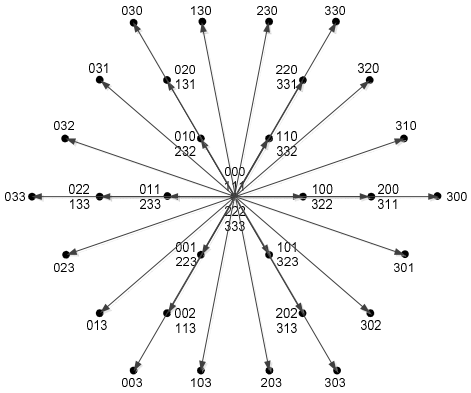
The voltage vectors can be achieved by Park's transformation as in (3):

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} \tag{3}$$

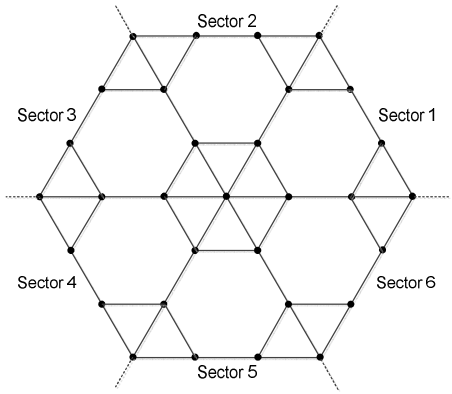
Thus:

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} 2S_A - S_B - S_C \\ 2S_B - S_C - S_A \\ 2S_C - S_A - S_B \end{bmatrix} \tag{4}$$

(4) is only valid when neither of the two states in the switching state combinations have *State 1* and *State 2* at the same time since Q_{10} and Q_{11} cannot be active simultaneously. Hence, 31 voltage vectors can be obtained. Fig. 3 portrays the overall voltage vectors and the resulting voltage vector hexagon. It can be seen that the vector hexagon of the proposed inverter is different than that of a conventional multilevel inverter which produces seven levels in the line-to-line output voltage waveforms. Every sector consists of three triangles and a hexagon. This is as a result of using two shared bidirectional switches in the proposed topology which results in the elimination of six voltage vectors of magnitude $\sqrt{3}V_{dc}$. Therefore, the conventional concept of space vector modulation has to be modified in order to adapt to the changes in the vector hexagon.



(a) Voltage vectors.



(b) Vector hexagon.

Fig. 3. Voltage vectors and the resulting hexagon.

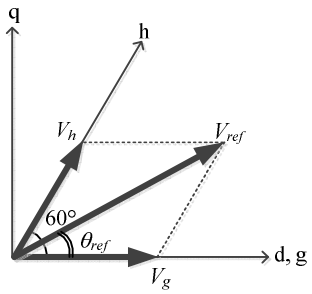


Fig. 4. The 60°-spaced g-h coordinate system.

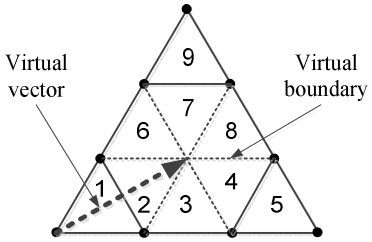


Fig. 5. Adaptation of space vector concept with the introduction of a virtual vector in sector 1.

To simplify the calculations in the algorithm, the 60°-spaced g-h coordinate system [20] is used to represent the voltage vectors. This coordinate system has two axes in which one of them is in the horizontal position (g-axis), while the other (h-axis) is inclined at an angle of 60° from the horizontal axis as shown in Fig. 4. By using this coordinate system, all of the voltage vectors have coordinates in integer form to allow fixed-point rather than floating-point calculations to be performed. In order to do the conversion to the g-h plane, the following are applied:

$$V_g = V_{ref}\left(\cos\theta_{ref} - \frac{\sin\theta_{ref}}{\sqrt{3}}\right) \tag{5}$$

$$V_h = V_{ref}\left(\frac{2\sin\theta_{ref}}{\sqrt{3}}\right) \tag{6}$$

where

$$V_{ref} = \sqrt{V_d^{\,2} + V_q^{\,2}} \tag{7}$$

and

$$\theta_{ref} = \tan^{-1}\left(\frac{V_q}{V_d}\right) \tag{8}$$

To describe the adaptation made, consider sector 1 of the vector hexagon as shown in Fig. 5. A virtual vector with a magnitude of $\sqrt{2}\,V_{dc}$ (based on the g-h vector space) is introduced so that three virtual boundaries that pass through the virtual vector's coordinate can be drawn. With the virtual boundaries, nine triangles can be formed. Any voltage reference vector that falls within triangles 1, 5 and 9, in Fig. 5, can be represented by a sum of different portions of the three nearest vectors that form the triangles. In other words, the conventional space vector concept applies. However, if the reference vector lies within triangles 2, 3, 4, 6, 7 and 8, the two nearest vectors are only considered to represent the reference vector. Hence, the calculation of the switching time for the two nearest vectors is done using the following equations:

$$T_{1,g} = \frac{(V_{ref,g} - V_{2,g})T_S}{V_{1,g} - V_{2,g}} \tag{9}$$

$$T_{2,g} = T_S - T_{1,g} \tag{10}$$

and:

$$T_{2,h} = \frac{(V_{ref,h} - V_{2,h})T_S}{V_{1,h} - V_{2,h}} \tag{11}$$

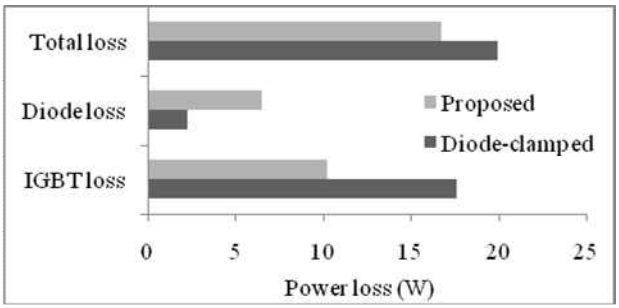


Fig. 6. Power loss comparison.

$$T_{1,h} = T_S - T_{2,h} \tag{12}$$

where $V_{1,g}$ and $V_{2,g}$ are the g-components of the two nearest vectors, $V_{1,h}$ and $V_{2,h}$ are the h-components of the vectors, $T_{1,g}$ and $T_{2,g}$ are the switching times calculated using the g-components of the vectors, $T_{1,h}$ and $T_{2,h}$ are the switching times calculated using the h-components of the vectors, and T_s is the sampling time. To obtain T_1 and T_2, the average is calculated as below:

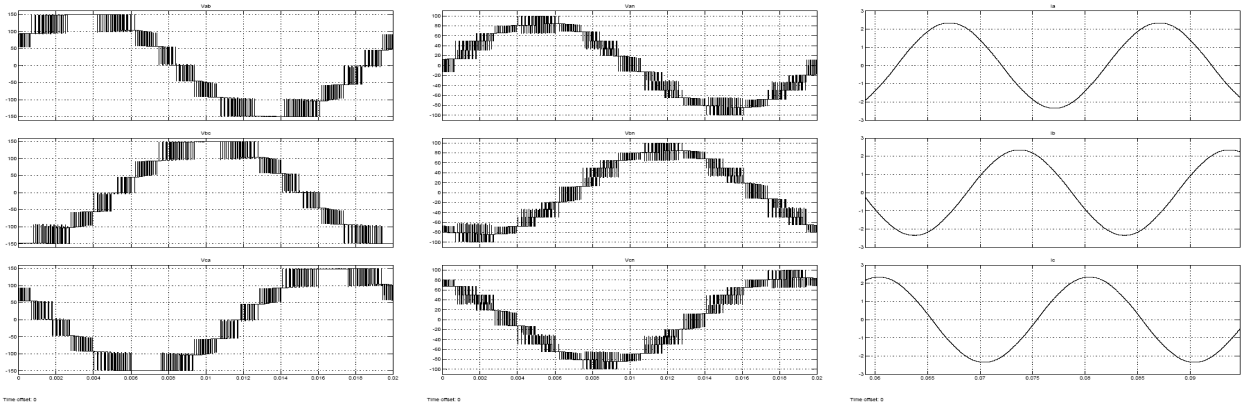
$$T_1 = \frac{(T_{1,g} - T_{1,h})}{2} \tag{13}$$

$$T_2 = \frac{(T_{2,g} - T_{2,h})}{2} \tag{14}$$

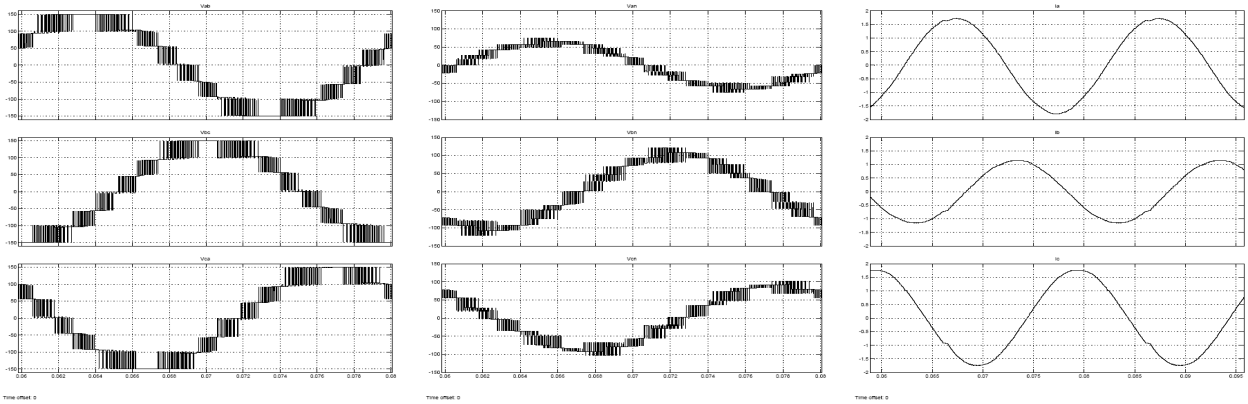
(13) and (14) are valid if both $T_{1,g}$ and $T_{2,h}$ do not become infinity. If $T_{1,g}$ becomes infinity, then $T_1 = T_{1,h}$ and $T_2 = T_{2,h}$. If $T_{2,h}$ becomes infinity, then $T_1 = T_{1,g}$ and $T_2 = T_{2,g}$. Note that the virtual vector is not included in the calculation since its function is to divide the original hexagon in every sector, as displayed in Fig. 3(b), into six triangles formed by the virtual boundaries.

IV. Power Loss Analysis

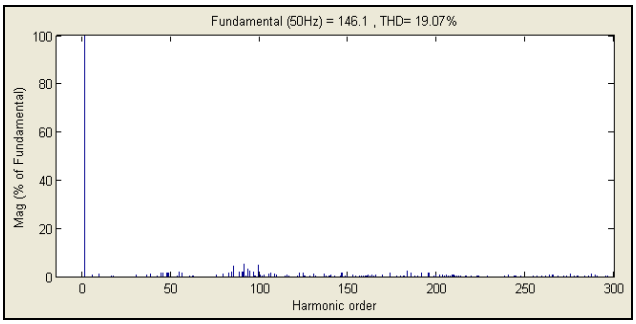
In order to investigate the power loss generated by the proposed topology, a MATLAB/SIMULINK model has been developed. In this analysis, only the conduction loss and switching loss of the semiconductor devices are considered while the off-state loss is neglected since the leakage current during the off-state is negligibly small [21]. To have a meaningful assessment of the power loss analysis, a comparison is then made with the equivalent diode-clamped multilevel inverter topology. The conduction loss is approximated from the forward voltage drop across the device and the conducted current in which the relationship of both are usually presented in a datasheet in the form of a curve. The switching loss of the IGBT, which is due to the turn-on and turn-off commutations as well as the reverse recovery of the freewheeling diode, is estimated from the energy loss curve with respect to the current. As for the diodes in the bidirectional switches, the switching loss due to



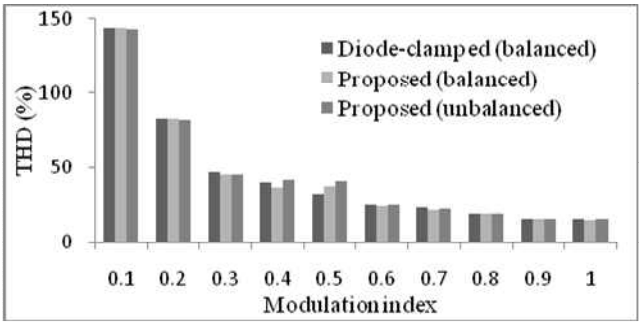
(a) V_{AB}, V_{BC} & V_{CA} for balanced R load. (b) V_{AN}, V_{BN} & V_{CN} for balanced R load. (c) I_A, I_B & I_C for balanced RL load.



(d) V_{AB}, V_{BC} & V_{CA} for unbalanced R load. (e) V_{AN}, V_{BN} & V_{CN} for unbalanced R load. (f) I_A, I_B & I_C for unbalanced RL load.



(g) Line-to-line voltage harmonic spectrum for balanced R load.



(h) Line-to-line voltage THD comparison.

Fig. 7. Simulation results.

the reverse recovery process can be derived from the reverse recovery time and reverse recovery current curves.

In this analysis, the datasheets of the IGBT module IRG4PC40UDPbF and the ultrafast, soft recovery diode HFA15TB60 are chosen to derive the equations of the conduction and switching losses. By using the MATLAB curve-fitting tool, the related curves given in the datasheets can be approximated in order to build the mathematical models that represent the power loss [22]. The results are as follows:

$$P_{cond,IGBT} = \frac{1}{T_p}\int_0^{T_p}\left(3.141e^{0.003496i(t)} - 2.296e^{-0.01392i(t)}\right)i(t)dt \tag{15}$$

$$P_{cond,diode} = \frac{1}{T_p}\int_0^{T_p}\left(1.454e^{0.008335i(t)} - 0.5567e^{-0.1443i(t)}\right)i(t)dt \tag{16}$$

$$E_{sw,IGBT} = 15.62e^{0.009769i(t)} - 15.62e^{0.009764i(t)} \tag{17}$$

$$E_{sw,diode} = (16.5e^{-0.0019866i(t)} - 10.3e^{-0.0799716i(t)} - 2.78e^{-0.077215i(t)} + 1.734e^{-0.1552i(t)})\times 10^{-6} \tag{18}$$

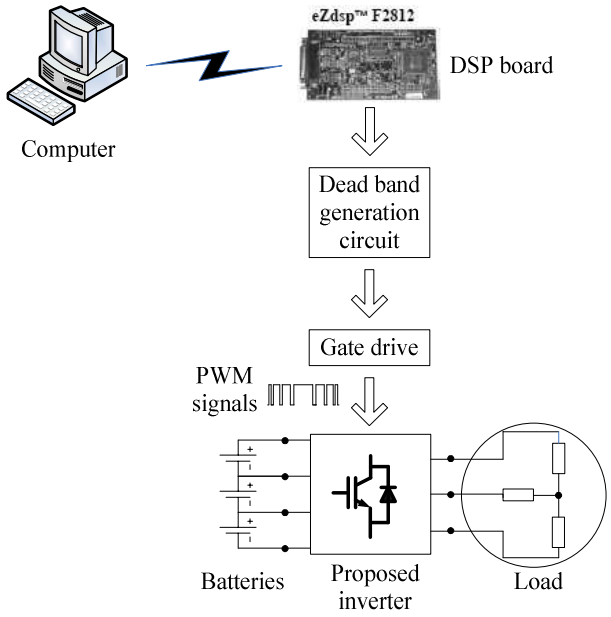


Fig. 8. Experimental setup.

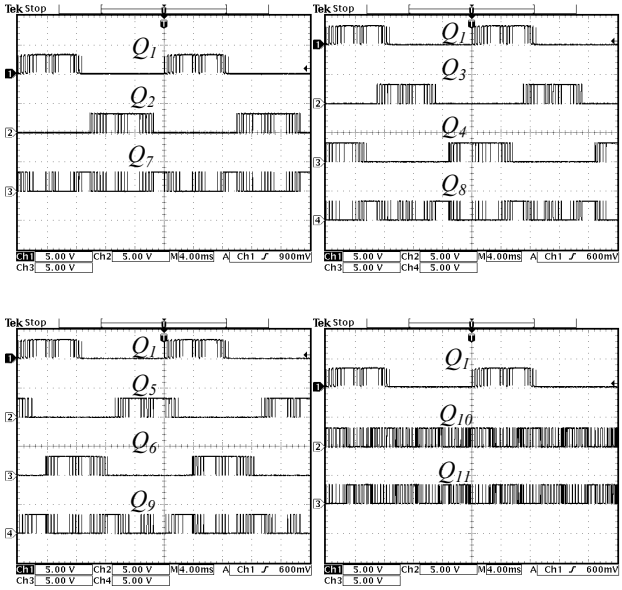


Fig. 9. Gating signals at modulation index of 0.8.

$$P_{sw,IGBT} = \frac{1}{T_p}\sum E_{sw,IGBT} \tag{19}$$

$$P_{sw,diode} = \frac{1}{T_p}\sum E_{sw,diode} \tag{20}$$

$$P_{total} = P_{cond,IGBT} + P_{cond,diode} + P_{sw,IGBT} + P_{sw,diode} \tag{21}$$

where T_p is the period for one cycle, $P_{cond,IGBT}$ is the IGBT conduction power loss, $P_{cond,diode}$ is the diode conduction power loss, $E_{sw,IGBT}$ is the IGBT switching energy loss, $E_{sw,diode}$ is the diode switching energy loss, $P_{sw,IGBT}$ is the IGBT switching power loss, $P_{sw,diode}$ is the diode switching power loss, and P_{total} is the total power loss.

Fig. 6 shows the power loss of the proposed inverter as compared to that of the equivalent diode-clamped inverter when both inverters are supplied with a 150-V DC input voltage and are connected to a resistive load of 30.5 Ω per phase. The switching frequency is set at 4.6 kHz for the proposed and diode-clamped inverters to apply the modified SVPWM and the conventional SVPWM at a modulation index of 0.8. The proposed inverter records a total power loss of 16% less than that of the diode-clamped inverter. By considering only the conduction and switching losses in estimating the inverter's efficiency, the proposed inverter produces an efficiency of 95.59% as opposed to 94.74% for the diode-clamped inverter.

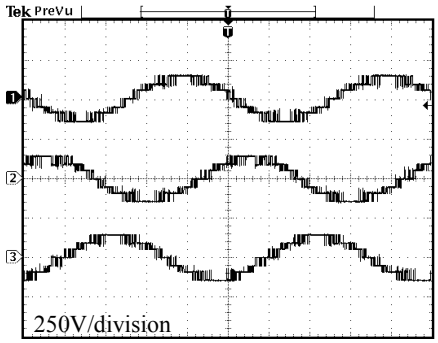
V. Simulation Verification

The proposed circuit configuration is simulated using MATLAB/SIMULINK software. The voltage sources produce an output of 150 V, and a balanced three-phase Y-connected resistive load of 30.5 Ω per phase is used. To study the performance under an unbalanced load, resistances with the following values are used: 30.5 Ω (phase A), 81.0 Ω (phase B) and 48.6 Ω (phase C). The modified space vector modulation is employed with a switching frequency of 4.6 kHz to generate the PWM switching signals.

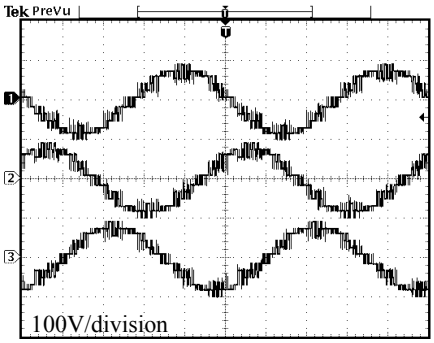
At a modulation index of 0.8, the line-to-line and phase output voltage waveforms are shown in Fig. 7(a) and (b), respectively, for a balanced load, while Fig. 7(c) and (d) display those for an unbalanced load. With the inclusion of an inductance of 68 mH per phase, a Y-connected RL load is introduced. At the same modulation index, the output current waveforms are given in Fig. 7(e) and (f) for balanced and unbalanced RL loads, respectively. Fig. 7(g) illustrates the harmonic spectrum for the line-to-line voltage under the balanced condition.

For the purpose of comparison, the equivalent diode-clamped multilevel inverter is also simulated with the same conditions as those of the proposed inverter. The conventional space vector modulation technique is applied for a 4.6-kHz switching frequency. The total harmonic distortion (THD) for the line-to-line voltages of both the proposed and benchmark inverters are compared and displayed in Fig. 7(h). It can be seen that the THD of the proposed inverter under a balanced load is slightly lower than that of the benchmark for all values of the modulation index except for the value of 0.5 in which the absence of the $\sqrt{3}V_{dc}$ voltage vector contributes to a significant increase in THD for the proposed inverter.

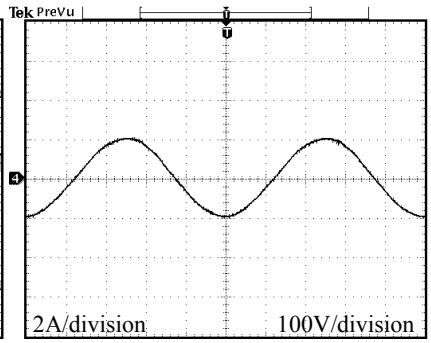
The case is different for an unbalanced load whereby the THD records comparable readings except at the 0.4 and 0.5 modulation indices. A significant increase of 4.8% and 28.3% are observed at the 0.4 and 0.5 modulation indices, respectively, when compared with the THD of the diode-camped inverter.



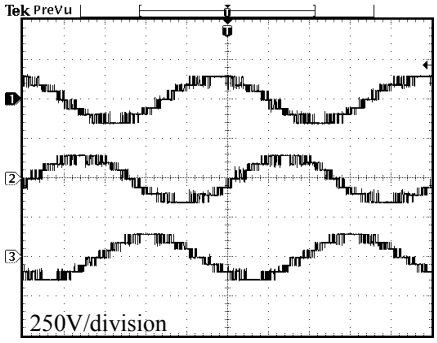
(a) V_{AB}, V_{BC} & V_{CA} for balanced R load.



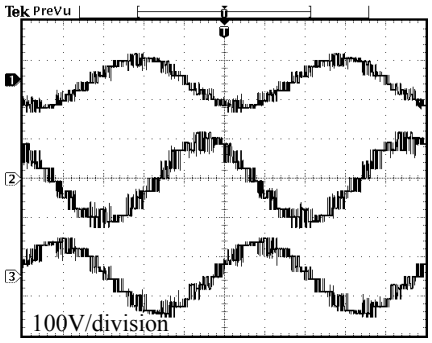
(b) V_{AN}, V_{BN} & V_{CN} for balanced R load.



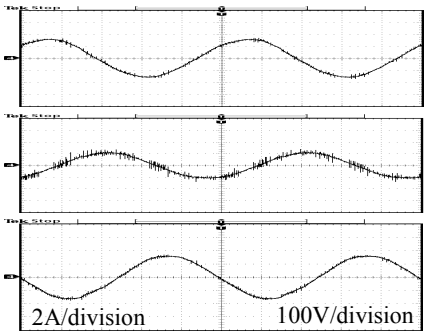
(c) I_A for balanced RL load.



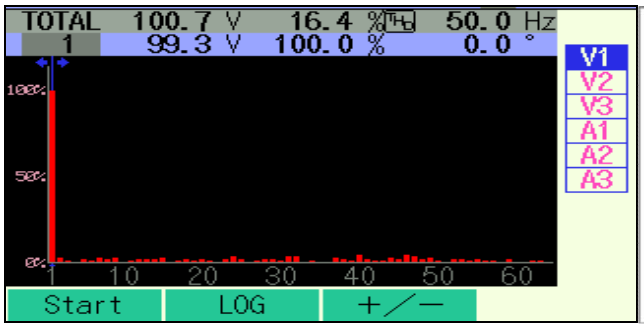
(d) V_{AB}, V_{BC} & V_{CA} for unbalanced R load.



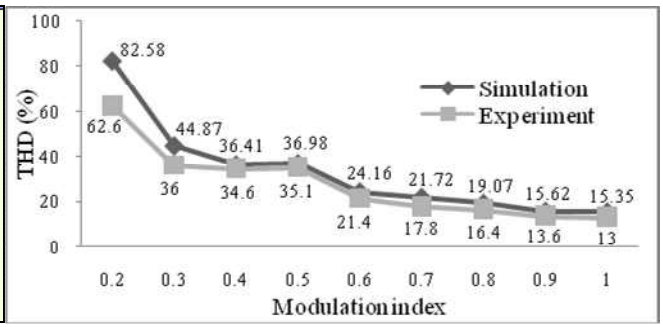
(e) V_{AN}, V_{BN} & V_{CN} for unbalanced R load.



(f) I_A, I_B & I_C for unbalanced RL load



(g) Line-to-line voltage harmonic spectrum for balanced R load.



(h) Line-to-line voltage THD comparison for balanced R load.

Fig. 10. Experimental results.

When the THD of the proposed inverter under a balanced load is regarded as the reference, the THD under an unbalanced load is noticeably higher by 14.0% and 10.3% at the abovementioned modulation indices. It can also be observed that the THD decreases as the modulation index increases for both balanced and unbalanced loads, which is similar to the behavior of the diode-clamped inverter.

VI. IMPLEMENTATION

A prototype of the proposed inverter has been constructed. A diagram of the experimental setup is presented in Fig. 8. Three NiMH batteries of 50 V, 13 Ah capacity each are used to supply the inverter. 600 V IGBTs act as the switching power devices and 30 A, 1200 V hyperfast diodes are utilized to construct the bidirectional switches. The load consists of a three-phase Y-connected resistance of 30.5 Ω per phase. An inductance of 68 mH per phase is added to form the RL load. An unbalanced load is achieved by using 81.0 Ω and 48.6 Ω to replace the resistances in phase B and C. The modified space vector modulation algorithm is implemented using a DSP controller board (eZdsp F2812). A 32-bit, 150-MHz, fixed-point TMS320F2812 processor executes the algorithm with a sampling frequency of 4.6 kHz in order to generate the PWM pulses for the power switches through dead band generation circuits and gate drives.

The gating pulses captured using a Tektronix TDS3054C oscilloscope are displayed in Fig. 9. Fig. 10(a)-(g) presents the experimental results at a modulation index of 0.8. The line-to-line and phase output voltage waveforms are shown in Fig. 10(a) and (b), respectively, for a balanced load. Fig. 10(c) portrays the output current waveform from a balanced

RL load. Those waveforms are also given in Fig. 10(d)-(f) for an unbalanced load. The balanced line-to-line voltage harmonic spectrum obtained from a power quality analyzer is shown in Fig. 10(g). By comparing the experimental results with the simulation counterparts, it can be seen that both display a lot of similarities. For instance, at a modulation index of 0.8, the rms value of the fundamental output of the line-to-line voltage which is recorded to be 103.3 V ($146.1/\sqrt{2}$ from Fig. 7(g)) from the simulation which does not differ too much from that obtained from the experiment, namely 99.3 V (from Figure 10(g)). Fig. 10(h) which lists the THD values from both the simulation and the experiment further proves that they are comparable. The similarities between simulation and experiment results verify the inverter's practicality.

VII. CONCLUSION

In this paper, a new multilevel inverter topology that exploits the sharing capability of power switches has been presented. The proposed inverter is able to produce seven levels in the line-to-line output voltages where two bidirectional power switches are shared among the three phases. The fact that several voltage vectors are eliminated makes way for the suggested adaptation of the conventional space vector modulation technique with the introduction of virtual voltage vectors. Simplified computation has been achieved with the use of the 60° coordinate system. This modified strategy has been implemented using a TMS320F2812 DSP and tested with a hardware prototype of the proposed inverter. The experimental results obtained show close agreement with those from the simulation. Owing to the reduced circuit complexity through the use of a smaller number of power switches and the successful implementation of the suggested modulation method, the proposed inverter provides a good alternative for various applications. Furthermore, the switch-sharing feature illustrated in this configuration portrays the inverter's uniqueness which may result in further exploration to achieve a power-circuit-simplicity advantage.

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