

Controlled-Type ZVS Technique without Auxiliary Components for Micro-inverters

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Abstract

This paper proposes a Boundary Current Mode (BCM) control scheme to realize soft switching on a conventional single phase full bridge DC/AC inverter. This technique with the advantages of no auxiliary components, low cost, high efficiency, and simple in control, is attractive for micro-inverter applications. The operation principle and characteristic waveforms of the proposed soft switching technique are analyzed in theory. A digital controller is provided based on that theory. To balance the requirements of efficiency, switching frequency, and inductor size, the design considerations are discussed in detail to guide in BCM inverter construction. A 150W prototype is built under these guidelines to implement the BCM control scheme. Simulation and experiment results demonstrate the feasibilities of the proposed soft switching technique.

Key words: BCM, Inverters, Soft-switching techniques

I. INTRODUCTION

Micro-inverters have received a great deal of attention from industry and in academic fields due to its advantages of easy installation, simple maintenance, maximum energy harvest and safe operation. However, cost, power density, efficiency and reliability still present major barriers to the implementation of micro-inverters on a large scale [1]. A higher switching frequency is an effective way to increase the power density and reduce the cost. However, a higher switching frequency induces higher power losses and more EMI. To solve these problems and maintain a high frequency, soft switching is one of the best options. A variety of soft switching techniques have been proposed for inverter applications [2]-[14]. They can be classified into three groups: load resonant [2], [3], resonant link [4]-[9], and resonant transition [10]-[14]. However, most of these require special

inverter topologies, auxiliary resonant components, additional switches, and complex control algorithms, resulting in size and cost increases in inverter systems.

To reduce the number of resonant components, several soft switching techniques have been proposed in the last decade [15]-[19]. Some of these techniques employ a partial inverter circuit to form the resonant network [15]-[18]. For example, literature [15], [16] employ a leakage inductor of the flyback transformer to achieve ZVS on the main switch. Literature [17] employs a parasitic capacitor of the main switches and leakage inductor of the transformer to form the resonant network. Literature [18] proposed a ZVS control for a buck PFC converter, which employed the intrinsic capacitors of semiconductors and a buck inductor to form a resonant circuit. Literature [19] is based on DCM operation to realize ZCS control. No resonant components are required in [19]. The realization of the ZCS depends entirely on the current-zero-detection circuit.

In this paper, a soft switching technique is proposed based on the conventional full-bridge DC/AC inverter topology. The parasitic capacitors of the MOSFETs and the filter inductor in the inverter are employed to form a resonant network. By adopting a digital controller, the inductor current is constrained to operating under the Boundary Current Mode and zero voltage switching (ZVS) operation is realized.

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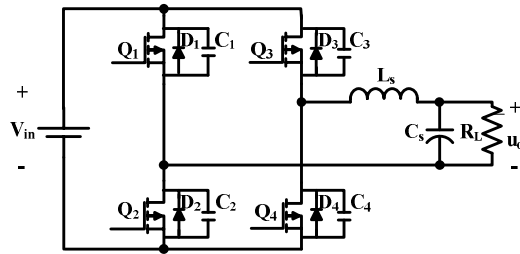


Fig. 1. Single-phase inverter topology.

Compared with the ZVS techniques in [15]-[17], which require additional resonant components and complex driver signals, the proposed BCM inverter requires no auxiliary components. Moreover, the control circuit is simple since only a pair of high frequency signals complementary to each other are required. Compared with the ZVS in [18], which has a non-operation period dependent on V_{in}/V_o , the BCM operation is controlled wholly with driver signals. Compared with the ZCS in [19], the BCM inverter does not require a current-zero-detection circuit, which is sensitive to noise.

This paper is laid out as follows. The operating principle and controller design of the BCM inverter are analyzed in section II. Section III discusses the design guideline for the BCM inverter with an example provided. In sections IV and V simulations are carried out and an experiment prototype is built to implement the proposed control scheme and design guideline. Section VI concludes that the controlled-type ZVS technique and design guideline are feasible and effective.

II. OPERATION PRINCIPLE AND CONTROL DESIGN

A. Operation Principle

Fig.1. shows a full-bridge topology for a single-phase inverter with one leg (Q1 and Q2) operating at a high switching frequency and the other leg (Q3 and Q4) operating at the line frequency. The body diode and the parasitic output capacitor of the MOSFET are represented as the diode and capacitor anti-parallel connected with the switch in Fig. 1. To generate the ZVS condition during commutations, the inductor current is intentionally operated bi-directionally in every switching cycle, as shown in Fig. 2, which is referred to as the BCM in this paper.

To simplify the analysis, assume that the whole inverter system has achieved the steady state. Depending on the polarity of the output voltage, the operation of the inverter can be divided into two modes: 1. $V_o > 0$; 2. $V_o < 0$. Each mode has six stages as shown in Fig. 3 and Fig. 4. The detailed analysis is as follows.

1. Mode 1 ($V_o > 0$)

Stage 1 [t_0-t_1]: During this stage Q₂ and Q₃ are on, whereas Q₁ and Q₄ are off. The DC voltage transfers energy to the

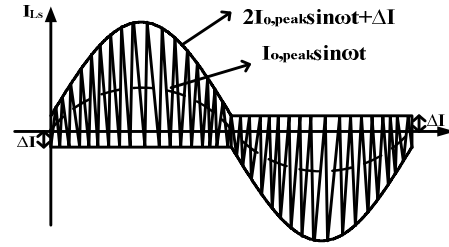


Fig.. 2. Inductor current waveform.

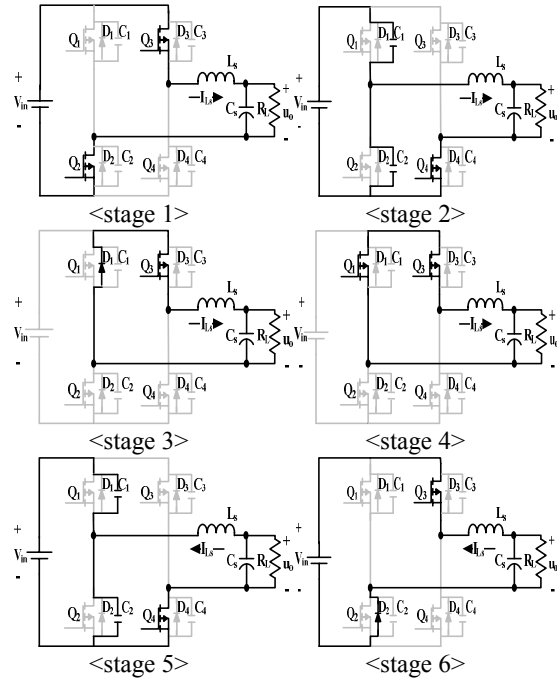


Fig. 3. Operation stages for the BCM inverter.

inductor and the inductor current increases linearly. The voltage across body capacitor C₂ is zero, and the voltage across capacitor C₁ is equal to the input voltage

$$\begin{cases} i_{Ls}(t) = \frac{(V_{in} - u_o)}{L_s} t + i_{Ls}(t_0) \\ V_{C_2}(t) = 0 \\ V_{C_1}(t) = V_{in} \end{cases} \quad (1)$$

Stage 2 [t_1-t_2]: When the inductor current reaches the expected peak current at time t_1 , Q₂ is turned off. The output capacitors of MOSFETs C₁ and C₂ are charged and discharged respectively through the inductor current until C₁ is fully discharged. The status expressions are depicted as:

$$\begin{cases} V_{C_2}(t) = k_1 \cos(\omega t) + k_2 \sin(\omega t) + V_d - V_o \\ i_{Ls}(t) = \frac{1}{Z_0} (-k_1 \sin(\omega t) + k_2 \cos(\omega t)) \end{cases} \quad (2)$$

Where:

$$k_1 = \frac{V_o \cos(\omega t_1) - I_p + Z_0 \sin(\omega t_2)}{\cos \omega(t_1 - t_2)}$$

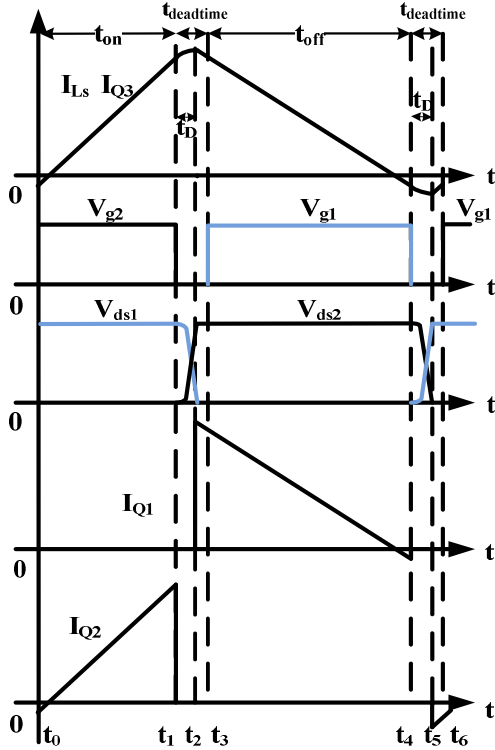


Fig. 4. Key waveforms in one switching cycle.

$$k_2 = \frac{V_o \sin(\omega_0 t_1) + I_p + Z_0 \cos(\omega_0 t_2)}{\cos \omega_0 (t_1 - t_2)}, \quad \omega_0 = \frac{1}{\sqrt{2CL_s}}$$

$$Z_0 = \sqrt{L_s / 2C}, \quad C_1 = C_2 = C$$

Stage 3 [t_2 - t_3]: As C_2 is charged to the DC bus voltage, the inductor current freewheels through body diode D_1 , creating the zero voltage switching condition for Q_1 . The inductor current flows through body diode D_1 and decreases linearly, as shown in <stage 3> of Fig. 3.

$$\begin{cases} i_{Ls}(t) = \frac{(-u_o)}{L_s} t + i_{Ls}(t_2) \\ V_{C_2}(t) = V_{in} \\ V_{C_1}(t) = 0 \end{cases} \quad (3)$$

Stage 4 [t_3 - t_4]: At time t_3 , with the arrival of the driver signal for Q_1 , the conductivity of the MOSFET increases. Thus, the inductor current can be regarded as shifting from the body diode D_1 "channel" to the Q_1 conductive "channel". With the output voltage across inductor L_s , the inductor current decreases linearly to zero and then increases in the negative direction. The status equations are the same as those in stage 3.

Stage 5 [t_4 - t_5]: At time t_4 , Q_1 is turned off. The negative peak current charges capacitor C_1 to the DC bus voltage and discharges capacitor C_2 to the zero voltage, respectively. The status equations are the same as those in stage 2.

Stage 6 [t_5 - t_6]: When the voltage across C_1 reaches the DC bus voltage, and the voltage across C_2 reaches zero, body diode D_2 freewheels the inductor current. The status equations are the same as those in stage 1.

2. Mode 2 ($V_o < 0$)

Since the analysis for this mode is complementary to the afore-presented $V_o > 0$ mode, it will be omitted here.

It is worth noting that a power MOSFET is commonly considered as a unidirectional switch since it blocks voltage only in one direction. However, a power MOSFET can conduct current in both directions. The operation of low voltage power MOSFETs in their third quadrant (when $V_{ds} < 0$ and $I_{ds} < 0$) is widely used in synchronous rectifier buck converters. The use of higher voltage (i.e. 600V in our case) power MOSFET in the third quadrant is less common, but it follows a similar operation principle.

B. Control Design

Assuming that the dead time is much smaller than the turn-on time and turn-off time, according to the voltage-second balance across inductor L_s , an expression can be easily derived as:

$$(V_{in} - u_o)t_{on} = u_o t_{off} \quad (4)$$

Where t_{on} stands for the turn-on time; t_{off} stands for the turn-off time; and $t_{deadtime}$ stands for the dead time, as illustrated in Fig. 4, which is ignored in equation (4).

As previously analyzed, the key point of this soft switching technique is that the inductor current should be large enough to generate the zero voltage condition during the switching transition periods. As illustrated in Fig. 4, t_4 - t_5 has a smaller inductor current than t_1 - t_2 . As a result, t_D for this period is longer. Therefore, $t_{deadtime}$ should be selected so that it is larger than t_D , and can be expressed as:

$$t_{deadtime} > \frac{(C_1 + C_2)V_{in}}{\Delta I} \geq t_D \quad (5)$$

To ensure that the average output current of every switching cycle is equal to $I_{o,peak} \sin \omega t$, (as illustrated in Fig. 2) the inductor peak-to-peak current increment during every switching cycle has to satisfy the following equation:

$$\frac{V_{in} - |u_o|}{L_s} t_{on} = 2(I_{o,peak} |\sin \omega t| + \Delta I) \quad (6)$$

By combining (4) and (6), the turn-on and turn-off time can be calculated by:

$$\begin{cases} t_{on} = \frac{2L_s(I_{o,peak} |\sin \omega t| + \Delta I)}{V_{in} - V_{o,peak} |\sin \omega t|} \\ t_{off} = \frac{2L_s(I_{o,peak} |\sin \omega t| + \Delta I)}{V_{o,peak} |\sin \omega t|} \end{cases} \quad (7)$$

Based on (7), a digital controller can be built to calculate the turn-on and turn-off times based on the sensing of V_{in} and V_o . The control block is shown in Fig. 5.

In Fig. 5, I_{ref} is the desired sinusoid waveform $I_{o,peak} |\sin \omega t|$ of the output current. I_{ref} can be generated by the output power

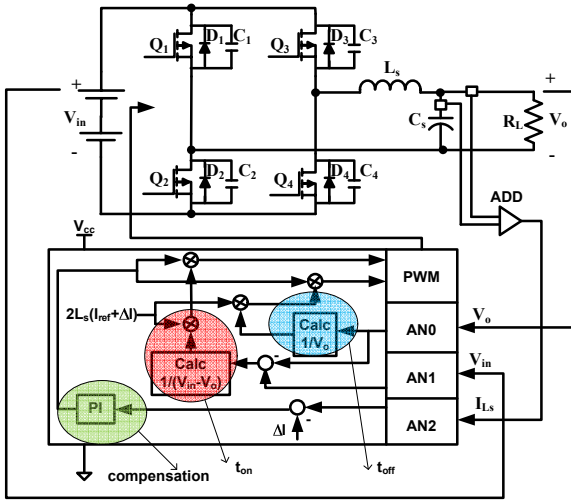


Fig. 5. Control block of BCM inverter.

and a PI regulator for V_o . This can make the system operate as a voltage source inverter. I_{ref} can also be pre-decided and pre-saved in the DSP. In this case the inverter can operate as an AC current source. Fig. 5 illustrates I_{ref} as a pre-saved parameter.

When the required output voltage is changed to $V_o < 0$, the calculations of t_{on} and t_{off} are still the same, except that Q_3 and Q_4 , and Q_1 and Q_2 exchange their status.

To ensure that the reverse-current is at the desired value ΔI , as illustrated in Fig. 2, a compensation block can be provided to t_{on} and t_{off} . As illustrated in Fig. 5, a PI regulator generates the compensation value by comparing the sampling value I_{Ls} with the given ΔI . The sampling of I_{Ls} is triggered by the falling edge V_{g1} (V_{g2}), as illustrated in Fig. 4, for modes $V_o > 0$ ($V_o < 0$). ADC is repeated several times until the minimum value is measured, so that the real reverse-current can be sensed. The compensation operation frequency can be lower than the switching frequency.

Since the inductor current includes both the switching frequency and the line frequency it is difficult to measure with a single transformer. As illustrated in Fig. 5, the inductor current can be sensed with a high frequency current transformer and a low frequency current sensor chip, which operate separately and are added to the capacitor and the output side inductor.

III. DESIGN CONSIDERATIONS

By adding the turn-on and turn-off times in (7) together, the relationship between the switching frequency and the other system parameters can be derived as:

$$F_s = \frac{V_{o, peak} |\sin \omega t| (V_{in} - V_{o, peak} |\sin \omega t|)}{2L_s V_{in} (I_{o, peak} |\sin \omega t| + \Delta I)} \quad (8)$$

For the proper design of the BCM inverter, once the operation condition is decided, the main circuit parameters can be specified. To give a design example, suppose that the input

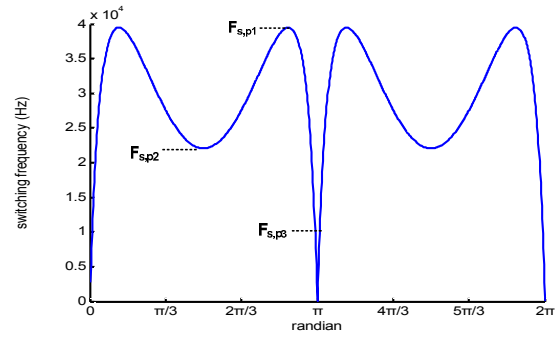


Fig. 6. Switching frequency waveform of BCM inverter.

DC voltage is 250V; the peak value of the output ac voltage is 170V with a line frequency of 60Hz; and the rated power is 150W. Considering the voltage and current stresses of the switches in this design example, the FCP20N60 MOSFET is selected to build the inverter system.

For the switching frequency design, Fig. 6 shows the waveform of the switching frequency vs ωt calculated by (8) in a full line cycle ($\omega t \in (0, 2\pi)$). Regardless of the vertical-axis value, the waveform shape is the same for different system parameters. It can be clearly seen in Fig. 6 that the switching frequency increases/decreases rapidly near $k\pi$ (k is integer 0,1,2...) and achieves zero at the points of $k\pi$. For practical considerations, usually the switching frequency is not increased from zero to the maximum value, as shown in Fig. 6. Therefore, when the switching frequency drops close to zero, all four switches can be turned off at the same time until the switching frequency rises away from zero again. This period is identified as the all-off period in this paper. When the all-off period is small enough, the output voltage distortion caused by this period can be neglected. (When the all-off period is less than $\pi/36$, the THD caused by this period is less than 1%.)

The maximum and minimum values of the switching frequency can be calculated by differentiating (8), as shown in (9) and (10). In addition, the all-off period restriction is considered to get the switching frequency range, as shown in (11).

$$F_{s, p1} = \frac{\beta(V_{in} - \beta)}{2L_s V_{in}(\alpha + \Delta I)} \quad (9)$$

$$F_{s, p2} = \frac{V_{o, peak}(V_{in} - V_{o, peak})}{2L_s V_{in}(I_{o, peak} + \Delta I)} \quad (10)$$

Where:

$$\alpha = \frac{-V_{o, peak}\Delta I + \sqrt{V_{o, peak}\Delta I(V_{o, peak}\Delta I + 3I_{o, peak}V_{in})}}{3V_{o, peak}}$$

$$\beta = \frac{-V_{o, peak}\Delta I + \sqrt{V_{o, peak}\Delta I(V_{o, peak}\Delta I + 3I_{o, peak}V_{in})}}{3I_{o, peak}}$$

$$F_{s, p3} = F_s \Big|_{\omega t = \frac{\pi}{2}} \quad (11)$$

Fig. 7 shows the boundary switching frequencies varying with the reverse current ΔI . (as the inductance of L_s has not

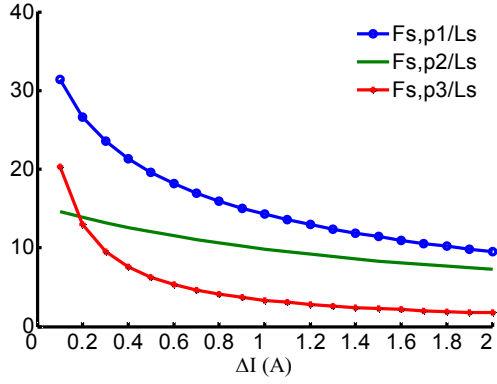
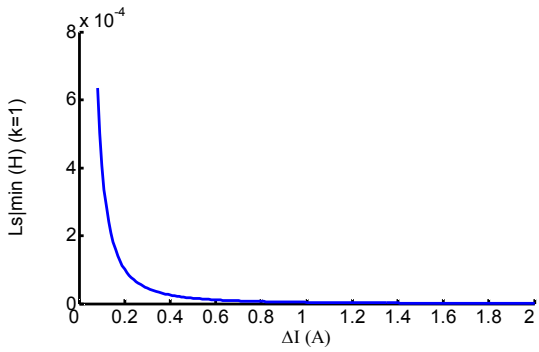


Fig. 7. Switching frequency range waveform.


 Fig. 8. Minimum L_s waveform with $k=1$.

been specified, the vertical-axis switching frequency is divided by L_s in Fig. 7) When I is larger than 0.2A, the boundary frequencies are decided by $F_{s,p1}$ and $F_{s,p3}$. Moreover, with an increase of I , the boundary switching frequencies and the frequency range decrease together.

According to (6), the minimum value of t_{on} (achieves at $V_o=0$) could be derived to get the restriction of L_s :

$$t_{on, \min} = \frac{2L_s \Delta I}{V_{in}} \quad (12)$$

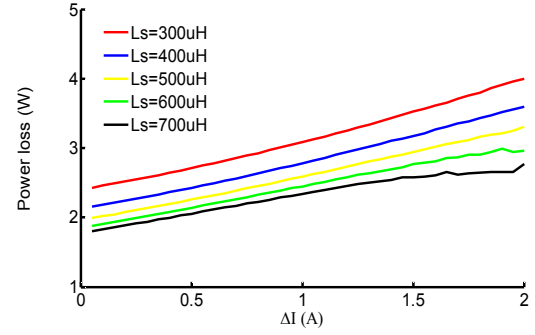
The calculations of t_{on} and t_{off} are based on (4), which neglects the dead time. To guarantee the accuracy of the calculations, the minimum value of t_{on} should be much larger than the dead time. Thus, (5) and (12) are combined to get a restriction for the L_s design.

$$L_s \geq \frac{k(C_1 + C_2)V_{in}^2}{2\Delta I^2} \quad (13)$$

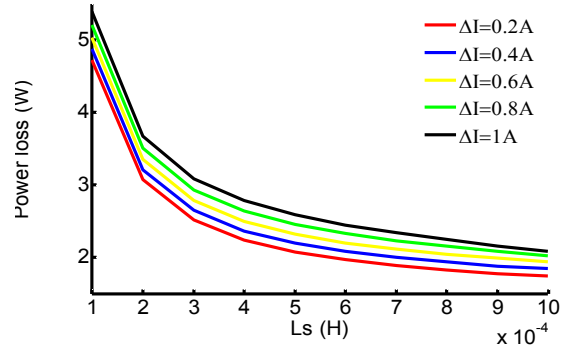
The larger the value of k , the less distortion is caused by neglecting the dead time, thus the more accurate the calculations of t_{on} and t_{off} become.

Fig. 8 is drawn from (13) to show the minimum value of inductor L_s when $k=1$. The output capacitance can be obtained from the datasheet of a FCP20N60.

Fig. 8 illustrates that with an increase of ΔI , the minimum



(a)



(b)

Fig. 9. Power loss waveforms.

requirement of L_s decreases.

Thus, based on Fig. 7 and Fig. 8, it is preferable for ΔI be larger to have a smaller inductance and a narrower switching frequency range. This results in a smaller size and a higher power density.

Although the proposed BCM control method realizes zero voltage switching during the turn-on period, there are still various losses for the inverter system such as the inductor and MOSFETs conduction losses, antiparallel diode loss, MOSFETs turn-off switching losses, inductor core losses, etc. To optimize the parameter section for the inverter system efficiency consideration, the power losses are calculated with Mathcad. (As inductor core losses is very difficult to calculate under various frequencies with various duty cycles. Thus, it is not included here.) The power loss waveforms are illustrated in Fig. 9.

Fig. 9.(a) shows the power loss vs. the ΔI waveforms under various L_s , while Fig. 9.(b) shows the power loss vs. the L_s waveforms under various ΔI .

Fig. 9.(a) illustrates that the power loss increases approximate linearly with a decreasing of ΔI ; while Fig. 9 (b) illustrates that the power loss increases more and more rapidly with a decreasing of L_s . Thus, from Fig. 9, it can be seen that L_s has to be larger than 400uH and ΔI should be as small as possible.

To balance the efficiency requirements with the size and

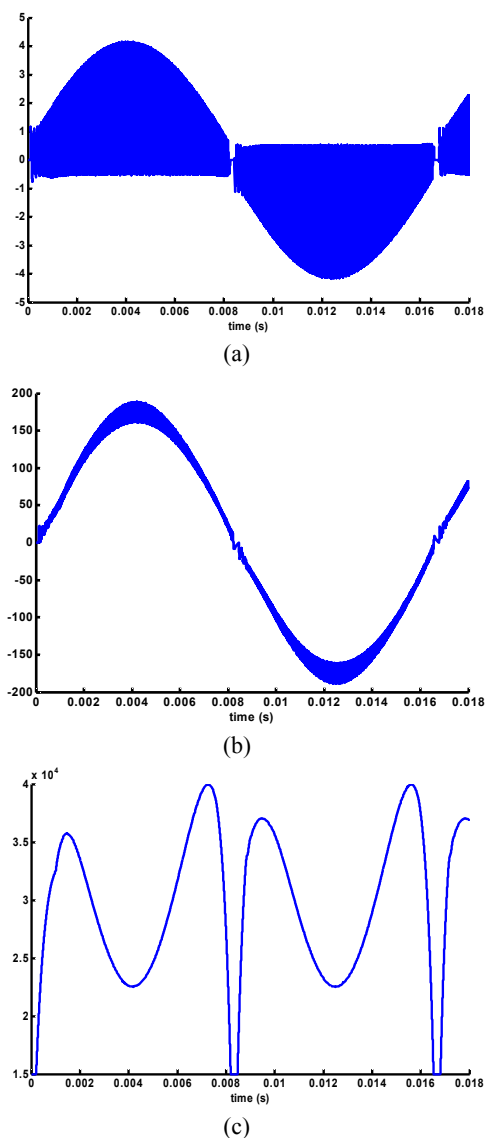


Fig. 10. BCM inverter simulation waveforms: (a) inductor current waveform, (b) output voltage waveform, (c) switching frequency waveform.

switching frequency range requirements, a trade-off decision has to be carefully made.

For the nonlinear relationship of the boundary frequencies vs. ΔI , as illustrated in Fig. 7, ΔI should be larger than 0.3A to have smaller boundary frequencies. From Fig. 8, assume that $k=10$ (The minimum L_s can be calculated by multiplying the vertical-axis value of Fig. 8 with 10.) is large enough to ignore the dead-time-distortion. For $\Delta I=0.2A$ $L_{s|min}$ is about 1000uH, and for $\Delta I=0.4A$ $L_{s|min}$ is about 270uH.

Considering all of the above restrictions, the parameters are selected to be $\Delta I=0.4A$ and $L_s=500uH$, and the relevant boundary switching frequencies are 15kHz and 42.6kHz. The overall calculated efficiency is 98.7%.

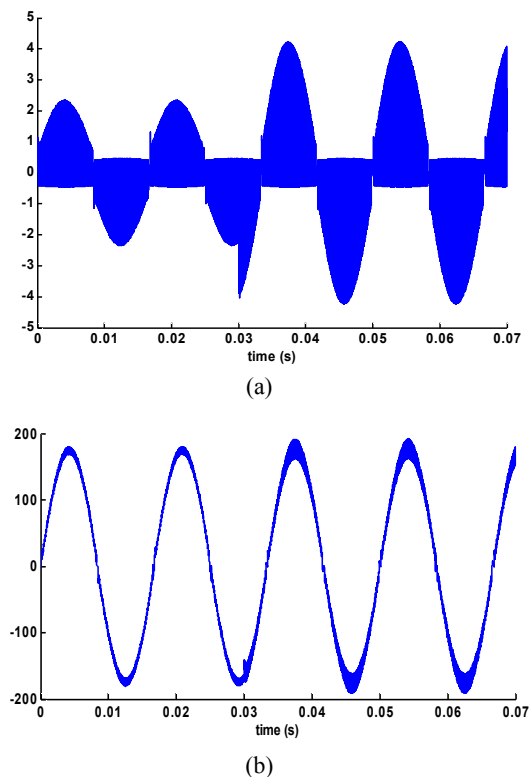


Fig. 11. BCM inverter simulation waveforms with sudden changing at $t=0.03s$ from half load to full load: (a) inductor current waveform, (b) output voltage waveform

IV. SIMULATION RESULTS

MATLAB Simulink was used to simulate the proposed control algorithm. The parameters of the single-phase inverter simulation system are set as: Input: 250V_{dc}; output: 170V_{ac,pk}; rated power: 150W, 60Hz; switching frequency: 15kHz~40kHz; $L_s=540uH$; $C_s=1uF$; and $\Delta I=0.5A$.

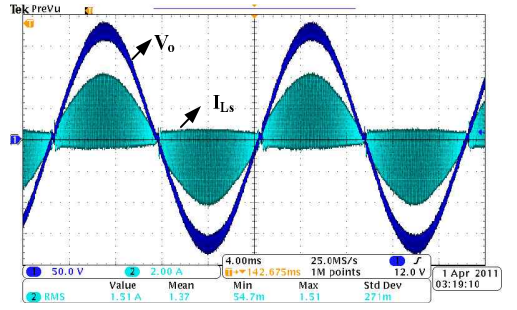
Fig. 10.(a) shows the inductor current waveform, which indicates that the inverter operates under the BCM mode as expected. Fig. 10.(b) shows the waveform of the output voltage; and Fig. 10.(c) shows the switching frequency waveform.

The waveform in Fig. 10.(c) is similar to the waveform in Fig.6. The only difference is caused by the compensation of ΔI mentioned in the control design section.

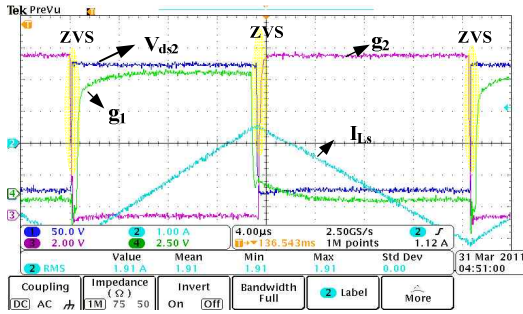
The simulation results verify that the proposed control algorithm operates as theoretically analyzed in section II.

To illustrate the transient operation of the proposed digital controller (when the BCM inverter operates as a voltage source), a simulation is carried out with the output power changing suddenly from half load to full load. The inductor current and output voltage waveforms are shown as in Fig. 11.

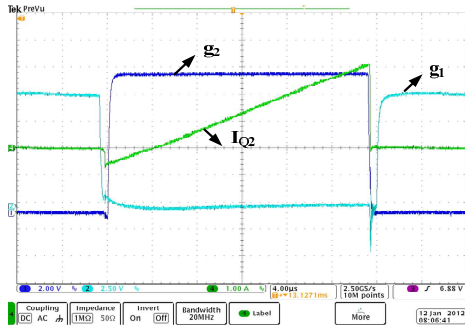
As illustrated in Fig. 11, the load change happens at $t=0.03s$. The inductor current (as shown in Fig. 11(a)) and



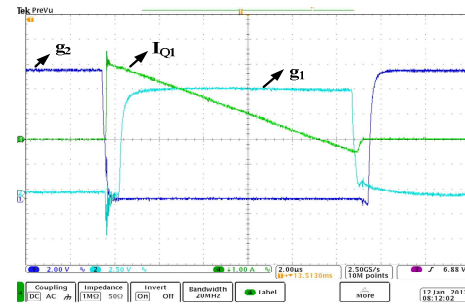
(a)



(b)



(c)



(d)

Fig. 12. BCM inverter waveforms: (a) output voltage & inductor current (b) zero voltage switching waveforms (c) current through MOSFET Q_2 and driver signals for MOSFETs Q_1 & Q_2 (d) current through MOSFET Q_1 and driver signals for MOSFETs Q_1 & Q_2 .

output voltage maintain the desired waveform (as shown in Fig. 11(b)).

V. EXPERIMENTAL RESULTS

A 150W full-bridge inverter prototype was built to implement the proposed control scheme. The digital

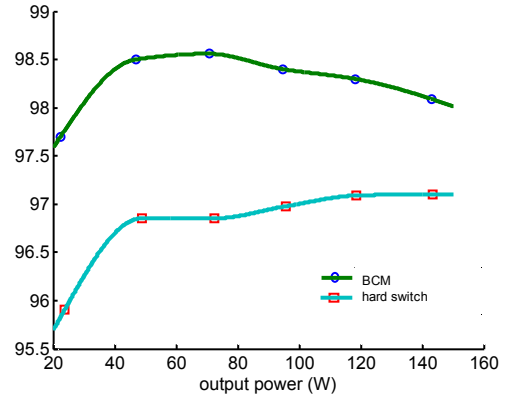


Fig. 13. Efficiency waveform of BCM inverter.

controller is implemented by a dspic30f2023 microchip. The parameters of the circuit system are set as below:

Input: $250V_{dc}$; output: $170V_{ac,pk}$; rated power: 150W, 60Hz; switching frequency: 15kHz~41kHz; $L_s=561\mu H$; $R_s=0.2\Omega$; $C_s=1\mu F$; and $\Delta I=0.4A$.

Fig. 12(a) shows the output voltage and inductor current. Both are similar to the simulation results in section IV. Fig. 12(b) shows the two complementary driving signals of the high frequency leg, the drain source voltage across one of the MOSFETs, and the current through the inductor. It can be clearly seen from Fig. 12(b) that before the arrival of g_2 , V_{ds2} across MOSFET Q_2 has already decreased to zero. Before the arrival of g_1 , V_{ds2} has already increased to its maximum. Thus, the ZVS is successfully realized during the switches transitions. Fig. 12(c) and (d) show key the waveforms for Q_1 and Q_2 individually. They operate exactly the same as in Fig. 4. They also confirm that although power MOSFETs operating in the third quadrant is not common, they are practicable.

To give a comparison of the proposed soft switching technique, continuous conduction mode (CCM) hard switching control is implemented on the same prototype. The detailed parameters are as follows:

Input voltage: $250V_{dc}$; output: $170V_{ac,pk}@150W$, 60Hz; switching frequency: 20kHz; $L_s=2.61mH$; $R_s=0.6\Omega$; and $C_s=1\mu F$.

Fig. 13 shows an efficiency comparison between the BCM and the hard-switching techniques. The peak efficiency of the BCM technique can reach up to 98.5%, which is 1.5% higher than the peak efficiency of the hard switching technique. All of the efficiency measurements were implemented by a PZ4000 power analyzer. The measured efficiency does not include the driving power loss.

VI. CONCLUSIONS

This paper proposes a novel soft switching technique for conventional full-bridge single phase DC/AC inverters. The

ZVS can be realized on all of the switches by operating the inductor current under the BCM control scheme. When compared with the hard switching inverter, it improves the efficiency without introducing additional components.

The operation principle of the proposed ZVS technology was analyzed in detail by dividing the operation progress into six stages. The equivalent circuits and key waveforms of each stage were discussed carefully to reveal the soft-switching characteristics. The digital control strategy was analyzed carefully to implement the proposed BCM technique. An example was given to introduce the design considerations and to aid in the inverter system parameter selections. A 150W inverter prototype was built under the design guideline to carry out the experiments. The experimental results verify the operation principle and the control analysis.

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