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A Novel Control Technique for a Multi-Output Switched-Resonant Converter

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Abstract

This paper proposes a novel control method for a multi-output switched-resonant converter. Output voltage can be regulated against variations in the supply voltage and load by controlling the voltage of the resonant capacitor (pulse amplitude control). Precise control is possible when pulse amplitude control is combined with pulse number control. The converter is analyzed, and design considerations are explained by using examples. Control implementation is described and load regulation and ripples are analyzed by simulation and hardware results. The topology is modified to obtain an additional negative output without any additional hardware other than a diode. The analysis of such a triple output converter with two positive outputs and one negative output is conducted and confirmed. The topology and control scheme are scalable to any number of outputs.

Keywords: Multi-Output, SIMO, Switched-Resonant Converter, SwRC

I. INTRODUCTION

Multiple-output converters are a category of converters wherein many different output voltages are obtained from a single converter. However, some parts of the converters are common for all outputs. This setup minimizes the total hardware count. If a forward or fly back converter is used, the primary winding of the transformer is common, but separate secondary windings are used for each output. This common primary winding reduces the reactive component in the converter, thus minimizing size, weight, and cost. Non-isolated versions have several types of single inductor and multiple-output converters (SIMO), wherein the source side inductor is common for all outputs.

Such multiple-output converters are required in a wide variety of applications. For example, a typical personal computer requires several different power supplies for the motherboard, hard disk, CD drive, cooling fan, and so on. Choosing the correct supply voltage for a specific load enhances the performance and improves the efficiency of the device by minimizing losses.

The key issue regarding multiple-output converters is the regulation of various outputs against varying supply voltages and loads with minimal hardware and minimal stress on the components. Any variation in the load of one output, apart from influencing its own output voltage, also influences the voltages of other outputs. This cross regulation is another important consideration.

Previous literature describes numerous possible configurations for multiple-output converters, which can be broadly divided into isolated and non-isolated converters [1]–[15]. For non-isolated converters, many configurations of SIMO converters have been proposed. A new family of switched-resonant converters has been proposed in [14], [15]. A resonant tank is repeatedly charged from the supply and is successively discharged into each output in a cyclic manner. Switches are turned OFF at zero current to minimize switching losses. Virtually no cross regulation exists between the outputs because of the discontinuous nature of the inductor current after the power discharge into each output. However, by the nature of this topology, power is transferred to the load in discrete units only, thus making the precise and continuous regulation of load voltage difficult.

In this study, a new control scheme is proposed to regulate the output voltage against load or supply variations. The voltage of the resonant capacitor is varied as needed to regulate the output voltage. This process can be performed in a continuous manner, thus enabling precise regulation. The modified topology has the additional advantage of obtaining

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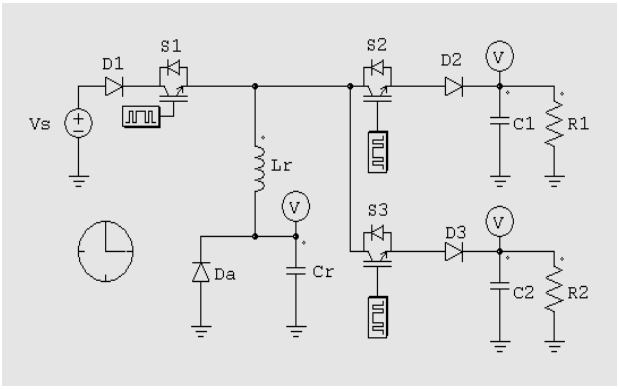


Fig. 1. Dual-output switched-resonant converter.

an additional negative output without the need for an additional switch. Hence, any positive or negative output voltage can be obtained and tightly regulated. The converter is analyzed, and the simulation and hardware results confirm the concept and analysis.

This paper is organized as follows. Chapter 2 explains the principle of operation of the converter and different existing methods of control. Chapter 3 discusses the proposed control method and the steady state analysis. Chapter 4 explains the design considerations. The control implementation strategy is discussed in Chapter 5. Chapter 6 presents the simulation and hardware results for the chosen converter. Chapter 7 discusses a converter modification that can generate an additional negative output with only an extra diode. Chapter 8 concludes.

II. PRINCIPLE OF OPERATION

Before explaining the proposed control method, the existing topology is briefly described and the control mechanism by frequency and pulse number variations is examined in this chapter. The switching devices are assumed ideal. Fig. 1 shows a dual-output switched-resonant converter with switches S1, S2, and S3. The switches turn ON and OFF at zero current. D1, D2, and D3 prevent conduction in the opposite direction through the body diodes of the switches.

When S1 is initially OFF, the supply *Vs*, *Lr*, and *Cr* form an oscillatory circuit. A half cycle later, the current returns to zero and S1 is turned OFF at ZCS. The voltage across the capacitor is approximately twice the supply voltage. After a small dead time, S2 is turned ON and the stored energy in the capacitor discharges into the load through the oscillatory circuit *Cr*, *Lr*, S2, and load *R*1 (parallel with the filter capacitor *C*1). A quarter cycle later, the voltage across the resonant capacitor becomes V1 (the voltage of the first output) and inductor current is at negative maximum. When the capacitor voltage becomes zero, the diode Da becomes forward biased. The capacitor *Cr* is now bypassed and the inductor current discharges into the load linearly since the load voltage is almost constant. S2 is turned OFF at ZCS after the discharge is complete. The above cyclic process repeats for the second output with the charging of the resonant capacitor *Cr* and discharging into the second output *R*2 (parallel with the filter capacitor C2).

A. Frequency (or dead time) Control

The energy stored in the capacitor at the end of the charging period is as follows:

$$0.5 * C_r (2V_s)^2 = 2C_r V_s^2 , \quad (1)$$

where $2V_s$ corresponds to the voltage of the resonant capacitor at the end of the charging period. The energy transferred to the first output during a complete switching cycle of T_s seconds is given by $(V_1^2 T_s / R1)$, where V_1 is the voltage of the first output and *R1* is the corresponding load resistance.

By equating the energies, we obtain the following:

$$C_r = (V_1^2 . T_s) / (2R_1 V_s^2) , \quad (2)$$

which indicates that C_r is proportional to the required output power $V_1^2 / R1$ and switching time T_s for a particular supply voltage. If the supply voltage V_s or load resistance *R1* changes, V_1 can be maintained constant by controlling T_s via frequency control (or dead time control). However, in frequency control, if *R1* changes and *R2* does not change, a variation in T_s to maintain V_1 constant will affect the other output voltage, thus leading to cross regulation. Hence, pure frequency control will not be suitable if more than one output exists.

B. Pulse Number Control

For a converter with two outputs, given that C_r is common for both the outputs and T_s encompasses both outputs, $C_r = (V_1^2 . T_s) / (2R_1 V_s^2) = (V_2^2 . T_s) / (2R_2 V_s^2)$, which implies that both outputs should have the same power. This constraint can be overcome by pulse number control, that is, a two-output converter should have $n1$ power pulses for the first output and $n2$ power pulses for the second output within each switching cycle. The equation for the capacitor is modified as follows:

$$C_r = (V_1^2 T_s / 2.R1.V_s^2 .n1) = (V_2^2 T_s / 2.R2.V_s^2 .n2) ,$$

and the ratio of the output powers is the same as $n1/n2$. The times allocated for each output within a switching cycle are also in the same ratio. The values of $n1$ and $n2$ can be varied independently within the overall T_s, thus preventing cross regulation. For example, if a dual-output converter has two outputs of 30 and 40 W, three and four power pulses will exist in the first and second outputs, respectively. The power of each pulse will be 10 W. The disadvantage of this method is that power and voltage can only be controlled in discrete values and intermittently. A supply of 8 and 15 pulses to the first and second outputs, respectively, may not be practical in every switching cycle at a power pulse of 5 W if the powers to the two outputs are 40 and 75 W. The proposed control

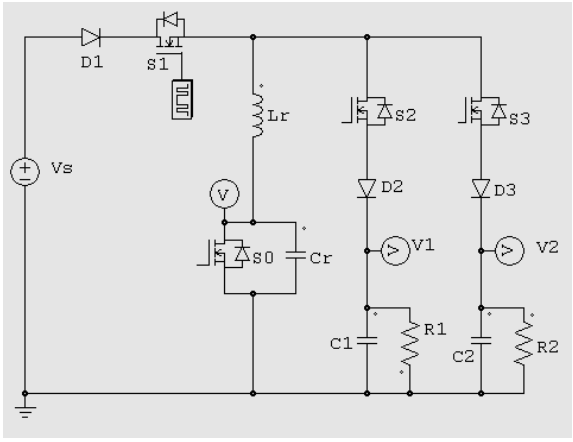


Fig. 2. Proposed converter with control of resonant capacitor voltage.

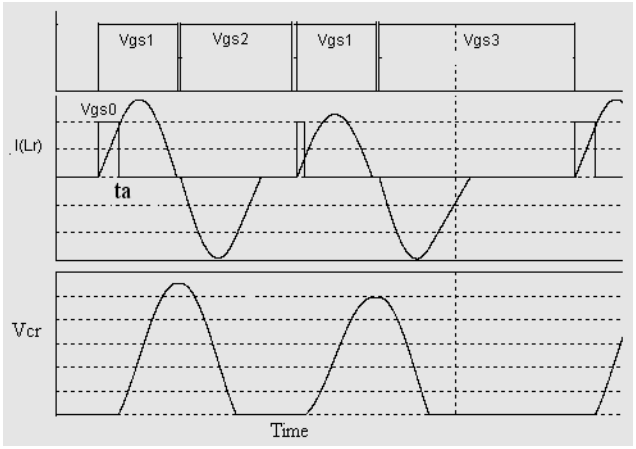


Fig. 3. Waveforms of the proposed converter.

method overcomes this problem by varying the voltage of the resonant capacitor. Hence, continuous variation in output is possible.

III. Proposed Control Method

In Equation (1.1), ($2V_s$) corresponds to the voltage of the resonant capacitor (V_{cr}) at the end of the resonant charging period. The proposed method varies the voltage of the resonant capacitor, thus controlling the output voltage. By expressing (2) in a general form, we obtain the following:

$$V_{cr}^2 = 2V_1^2 T_s / C_r R1 . \quad (3)$$

Hence, for a particular T_s and load resistance $R1$, the resonant capacitor voltage can be controlled to regulate V_1. The modified topology that enables this variation is shown in Fig. 2. The diode D_a is replaced with a switch S0(typically a MOSFET because ZVS is possible during turning ON and OFF). When S1 and S0 are turned ON, the current through the resonant inductor L_r increases linearly. When S0 is opened, the stored energy in the inductor completely discharges into the resonant capacitor *Cr*. The voltage across the resonant capacitor at the end of this discharge depends on the initial 'ON' duration of switches S1 and S0. Hence, by controlling this duration, the voltages of the resonant capacitor and the output can be continuously controlled.

The different modes of operation and the steady state analysis are described below. Fig. 3 shows the waveforms of the gate voltages, inductor current *I(Lr)*, and resonant capacitor voltage (*Vcr*). Fig. 4 shows the circuit during each operating mode.

Mode 1: All switches are initially in OFF states. At $t = 0$, S0 and S1 are turned ON. S0 is turned ON with both ZVS and ZCS, and S1 is turned ON with ZCS. The supply voltage V_s appears across the resonant inductor *Lr*, and the inductor current rises linearly. At $t = t_a$, the current becomes the following:

$$i(t_a) = V_s t_a / L_r = I_1 , \quad (4)$$

Mode 2: At $t = t_a$, S0 is switched OFF with ZVS. The parasitic capacitance of the switch is included in *Cr*. The voltage across Cr starts to rise. By considering this instant as t = 0 for this mode, we obtain the following:

$$V_s = L_r \frac{di}{dt} + \frac{1}{C_r}\int i dt . \quad (5)$$

The initial current is $i(t = 0) = I_1$. By solving the above equation, we obtain the following:

$$i(t) = (V_s / \omega L_r) Sin\omega t + I_1 Cos\omega t , \quad (6)$$

$$\omega = 1/\sqrt{L_r C_r} . \quad (7)$$

$i(t)$ can be rewritten as follows:

$$i(t) = \sqrt{I_1^2 + (V_s / \omega L_r)^2}\, Sin(\omega t + \alpha) , \quad (8)$$

where

$$\alpha = \tan^{-1}\left(\frac{I_1}{V_s / \omega L_r}\right) . \quad (9)$$

By substituting I_1 from Eq.(4), we obtain the following:

$$i(t) = \frac{V_s}{\omega L_r}\sqrt{1 + (\omega t_a)^2}\, Sin(\omega t + \alpha) \quad (10)$$

$$\alpha = \tan^{-1}(\omega t_a) \quad (11)$$

or $\omega t_a = \tan\alpha$.

The voltage across the capacitor can be written as follows:

$$V_{cr} = V_s - L_r \frac{di}{dt} . \quad (12)$$

From Eq. (10), the following expression is obtained:

$$V_{cr} = V_s\left(1 - \sqrt{1 + (\omega t_a)^2}\, Cos(\omega t + \alpha)\right) \quad (13)$$

For zero current switching, the current should be allowed to reach zero. From Eq. (10), the current becomes zero at $\omega t = \pi - \alpha$. The corresponding capacitor voltage becomes the following:

$$V_{cr0} = V_s\left(1 + \sqrt{1 + (\omega t_a)^2}\right) \quad (14)$$

Given that $\omega t_a = \tan\alpha$,

$$V_{cr0} = V_s(1+1/Cos\alpha)\,. \quad (15)$$

The variations in gain, V_{cr0} / V_s, and $\omega t = \tan\alpha$ with "t" is shown in Fig. 5. If the inductor is not initially charged, $I_1 = 0$ and Mode 1 does not exist; $t_a = 0$, $\alpha = 0$, and $V_{cr0} = 2V_s$. If the inductor is initially charged for a duration of t_1 such that $\alpha = \tan^{-1}(\omega t_1) = \pi/3$, the voltage across the capacitor becomes $3V_s$; that is, the capacitor voltage varies from $2V_s$ to $3V_s$ as α varies from zero to $\pi/3$.

Hence, the control action consists of varying t_a in Mode 1 such that the capacitor voltage is adjusted to the correct value corresponding to the load.

In Eq. (3), substituting $V_{cr} = V_s(1+1/Cos\alpha)$, the first output voltage becomes the following:

$$V_1 = V_s(1+1/Cos\alpha_1)\sqrt{C_r R1/2T_s}\,. \quad (16)$$

For different V_s and $R1$, α_1 is regulated to maintain V_1.

A similar equation is obtained for the second output:

$$V_2 = V_s(1+1/Cos\alpha_2)\sqrt{C_r R2/2T_s}\,. \quad (17)$$

α_2 is regulated to maintain V_2.

Given that α_1 and α_2 are independently controllable variables, no cross regulation occurs.

To constrain the maximum voltage and stresses across the capacitor and devices, α is limited to 45° or 60°. This control can be used together with the pulse number control for fine adjustment. For example, if the powers of the two outputs are 40 and 100 W, the first and second outputs will have one power pulse and two power pulses in every cycle, respectively. The power pulse of the first output is 40 W, which corresponds to $\alpha_1 = 0$, and the power pulse of the second output is 50 W with α adjusted suitably. From Eqs. (16) and (17), the corresponding α is 36°.

Mode 3: A small dead time, wherein no changes occur in current or voltage, is allowed for the devices to turn OFF completely.

Mode 4: After a small dead time, switch S2, which corresponds to the first output, is turned ON and the stored energy in capacitor C_r is transferred to the load. The inductor current varies in a sinusoidal manner:

$$I_{Lr} = (-(V_{cr0} - V1)/\omega L_r)Sin\omega t\,, \quad (18)$$

where the negative sign indicates that the current is in the opposite direction, and $t = 0$ corresponds to the beginning of this mode. The corresponding voltage across the capacitor is

$$V_{cr} = (V_{cr0} - V1)Cos\omega t + V1\,. \quad (19)$$

After a quarter cycle, at $t = t_3$ and $\omega t_3 = \pi/2$ (Fig. 12b), the following is obtained:

$$I_{Lr} = (-(V_{cr0} - V1)/\omega L_r)\,, \quad (20)$$

and $V_{cr} = V1$.

Depending on the load, $V_{cr} = 0$ at $t = t_4$. The corresponding inductor current at $t = t_4$ can be obtained from Eqs. (18) and (22) as follows:

$$I_{Lr} = (\frac{V_{cr0}}{\omega L_r})\sqrt{1-(2V_1/V_{cr0})}\,. \quad (21)$$

Mode 5: At t_4, the voltage across the capacitor is zero and attempts to become negative. This is prevented by body diode of S0, which is now forward biased. The inductor current now discharges linearly, and the duration from (19) is given by :

$$\omega t_4 = \pi - \cos^{-1}(V1/(V_{cr0} - V1))\,, \quad (22)$$

$$t_5 - t_4 = dt_5 = L_r\, dI/V1\,. \quad (23)$$

Given that the inductor current at the end of Mode 5 at $t = t_5$ is zero, dI = the value of I_{Lr} at t_4. Hence, we obtain the following from Eq.(21):

$$dt_5 = \frac{V_{cr0}}{\omega V_1}\sqrt{1-(2V_1/V_{cr0})}\,. \quad (24)$$

The mode ends after the linear discharge when the current becomes zero at t_5. After a small dead time, Modes 6 to 10 are implemented as a repeat of Modes 1 to 5 and feed power to the second output. The switching cycle is completed at the end of Mode 10.

IV. DESIGN CONSIDERATIONS

By choosing the resonant half-cycle duration t_1 based on device considerations and given that $\omega t_1 = \pi$, ω can be found. The dead times in Mode 3 and at the end of Mode 5 are allowed to be 10% of the charging time $t1$. Let D be the duty ratio. Depending on the power levels of the two outputs, we decide on the power to be transferred in each output pulse. For example, if the power levels are 15 and 25 W, each output power pulse could be 10 W, corresponding to $\alpha = 0$. The first and second outputs have one power pulse and two power pulses, respectively. "α" should be adjusted for the two outputs such that 10 and 20 W becomes 15 and 25 W, respectively. When $\alpha = 0°$ and $V_{cr0} = 2V_s$ for a single output converter and given that $t_1 = \pi/\omega$, the total time duration from Modes 1 to 5 including the dead times is :

$$\pi + 0.1\pi + \{\pi - Cos^{-1}(\frac{V_1}{2V_s - V_1})\} + \frac{2V_s}{V_1}\sqrt{1-(V_1/V_s)} + 0.1\pi = \omega DT_s\,. \quad (25)$$

By knowing ω, T_s can be obtained. From Eq. (2), we obtain the following:

$$C_r = (V_1^2 T_s/2.R1.V_s^2)\,. \quad (26)$$

For a particular supply voltage, C_r is proportional to the required output power $V1^2/R1$ and the switching time T_s. By knowing T_s, C_r can be obtained. By knowing ω and C_r, L_r can be obtained as follows:

$$L_r = 1/(\omega^2 C_r)\,. \quad (27)$$

For a dual-output converter, if T_s is divided equally between the two outputs, the right-hand side of Eq. (25) becomes $\omega DT_s/2$. T_s is in general, divided between the outputs at the same ratio as their powers.

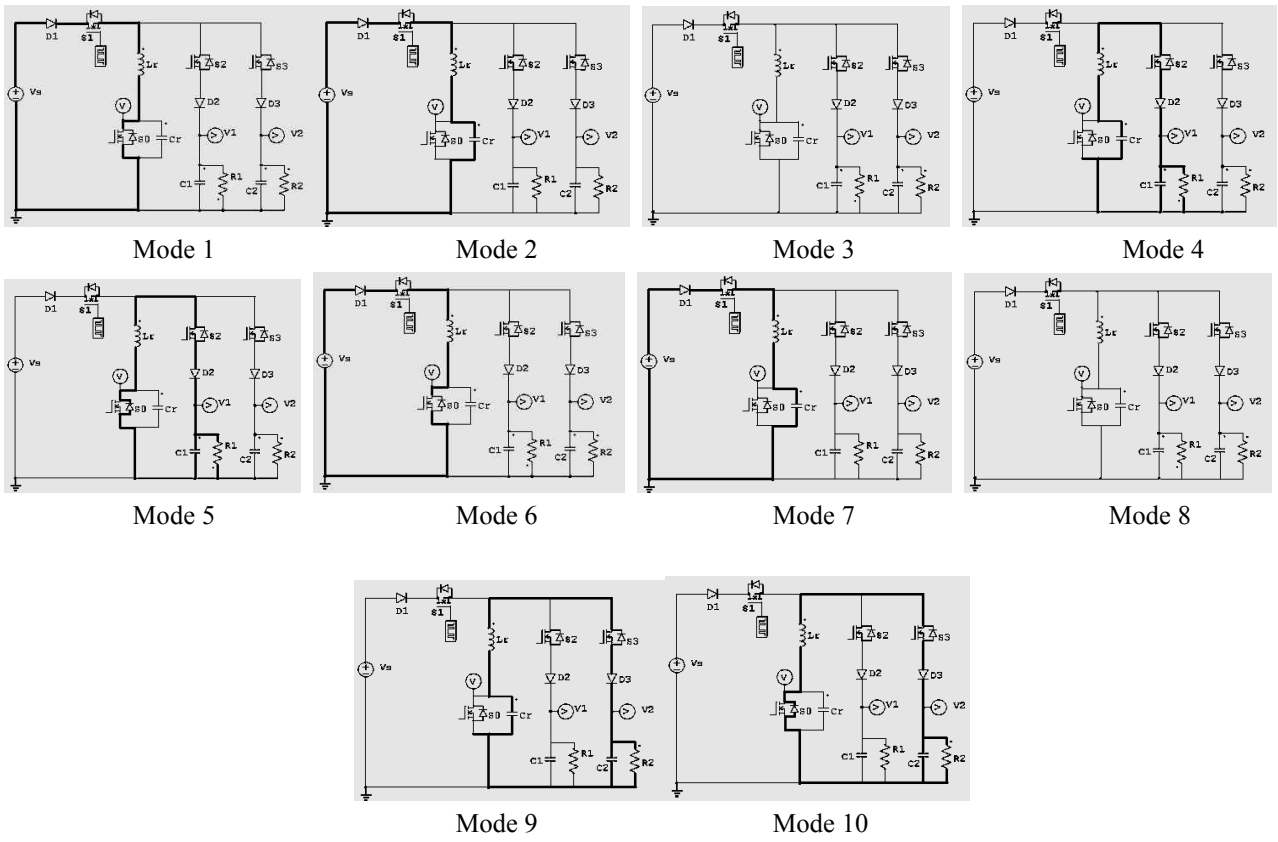


Fig. 4. Circuit diagram for different modes.

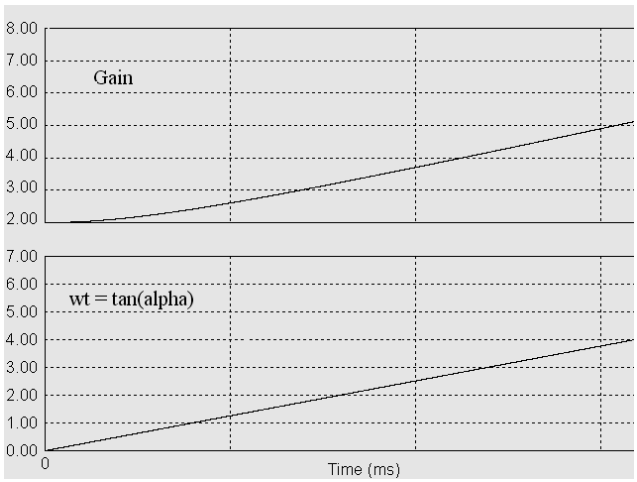


Fig. 5. Variation of gain and tanα with time.

The filter capacitor values are chosen based on ripple considerations. If each output is allocated at 50% of time T_s, the following is obtained:

$$Cf = (0.5T_s + 1.2\pi/\omega).100/R1.p\,, \qquad (28)$$

where p is the percentage of permitted ripple. The design considerations are explained by using the example shown below. The specifications of the chosen converter are shown in Table I.

TABLE I

CONVERTER SPECIFICATIONS

Rated supply	24 V
First output	12 V, 150 Ω
Second output	5 V, 22 Ω

The powers of the first and second outputs are less than 1 W and more than 1 W, respectively. By assuming a basic power pulse of 0.75 W for α = 0, the additional power for the two outputs can be obtained by varying α.

The resonant half-cycle time t_1 is chosen as 10 μs.

$\omega t_1 = \pi$, from which, $\omega = 0.3142*10^6$ rad/sec.

By using the second output as reference and the right side of Eq. (1.25) as $\omega DT_s/2$ for the dual-output case, we can obtain the following:

$$\pi + 0.1\pi + \{\pi - Cos^{-1}(\frac{V_2}{2V_s - V_2})\} + \frac{2V_s}{V_2}\sqrt{1-(V_2/V_s)} + 0.1\pi = \omega DT_s/2\,. \qquad (29)$$

T_s is obtained as 150 μs. From Eq.(26), C_r is obtained as 0.1 μF. From Eq.(27), the corresponding L_r is obtained as 101 μH.

V. CONTROL IMPLEMENTATION

The schematic for the control of the converter is shown in Fig. 6, and the corresponding power circuit is shown in Fig. 7.

Vg0, Vg1, Vg2, and Vg3 correspond to the gate signals of MOSFETs S0, S1, S2, and S3, respectively, and Vf1 and Vf2 are the feedback signals from the outputs.

The output voltage is continuously controlled by varying the resonant capacitor voltage. This resonant capacitor voltage is then controlled by the peak value of the inductor current in Mode 1 when S0 and S1 are ON. The setpoint of the required output is compared with the actual output and the error is passed through a PI controller and a limiter block. The output of this limiter block corresponds to the required value of the inductor currrent. Given that the current in the inductor charges linearly during Mode 1, "time" can be used as the controlling parameter instead of current, thereby making current sensing unnecessary. Similar to the "peak current mode control," a running clock generator sets a flip-flop periodically at the beginning of each clock cycle. The frequency of the clock generator corresponds to the required switching frequency of the converter. The output of the flip-flop drives the gate of S0. A time ramp is generated from the instant of the positive edge of the clock. When the output of the time ramp exceeds the output of the limiter block, the flip-flop is reset and S0 is turned OFF. Given that the same exercise has to be repeated for the second output, the outputs of the corresponding flip-flops are "OR"ed and given to the gate of S0. S1 is turned ON twice per cycle and once for each output to charge the resonant capacitor. S2 and S3 are turned ON once per cycle to discharge the energy from the resonant capacitor to the outputs. The ON durations of S1, S2, and S3 depend on the design parameters to ensure discontinuous conduction. A stabilizing ramp can be added if required.

VI. Simulation and Hardware Results

The simulation results for the converter with the specifications shown in Table I are discussed below. The output voltages, resonant inductor current, and resonant capacitor voltage at the specified supply of 24 V and load resistances of 150 and 22 Ω are shown in Fig. 8a. The corresponding waveforms when the supply voltage is changed to 15 V with the same load resistances is shown in Fig. 8b. Given the reduced supply voltage, the duration of initial charging in Mode 1 increases to supply the required energy. The waveforms for a supply of 24 V and the load resistances of the two outputs changed to 180 and 15 Ω are shown in Fig. 8c. The reduced power requirement of Output 1 and the increased power requirement of Output 2 are reflected in the current and voltage waveforms. In all cases, the output voltages are tightly regulated.

To achieve load regulation, the load resistance of the first output is changed from 30 Ω to 180 Ω in increments of 30 Ω. The corresponding output voltages and output currents are shown in Fig. 9(a). Table II shows the average, maximum, and minimum voltages for each load.

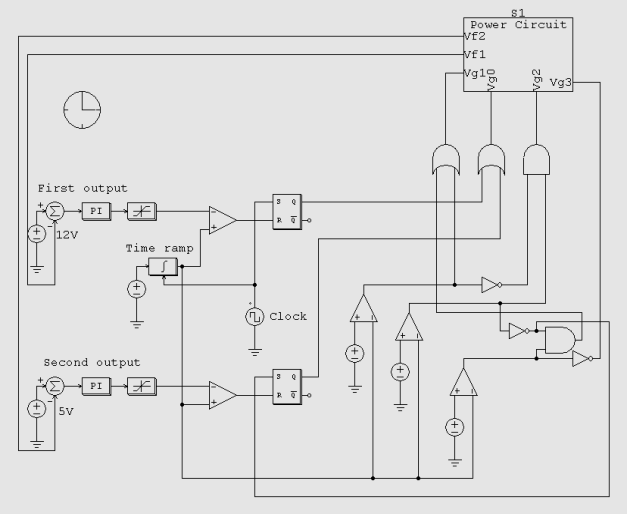


Fig. 6. Schematic of the controller.

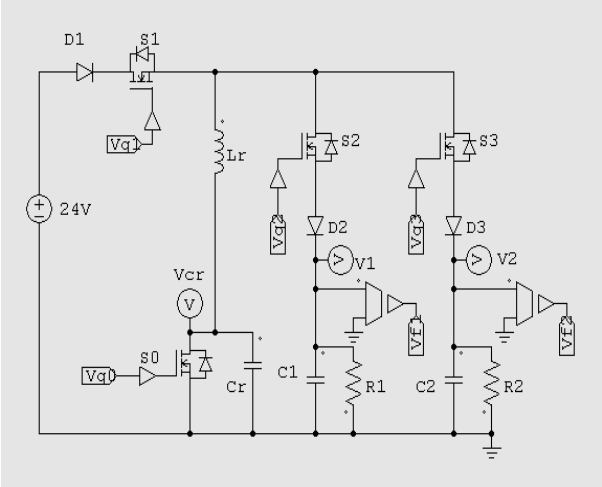


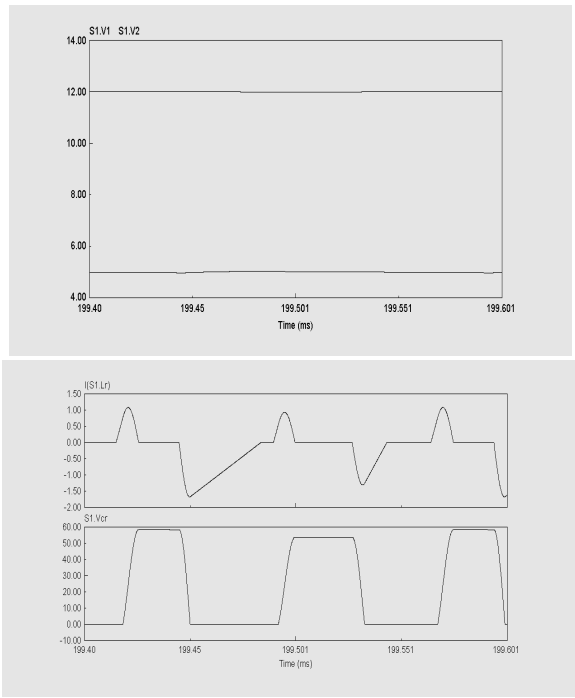
Fig. 7. Power circuit of the converter in Fig. 6.

TABLE II
Variation of First Output Voltage with Load

Sno	Load	Avg	Max	Min	Ripple
1	30 Ω	12.0004	12.0475	11.9462	0.84%
2	60 Ω	12.0003	12.0261	11.9719	0.45%
3	90 Ω	12.0002	12.0181	11.9809	0.31%
4	120 Ω	12.0001	12.0139	11.9854	0.24%
5	150 Ω	12.0000	12.0112	11.9881	0.19%
6	180 Ω	12.0003	12.0097	11.9903	0.16%

The load resistance of the second output is similarly changed from 10 Ω to 30 Ω in increments of 5 Ω. The corresponding output voltages and output currents are shown in Fig. 9(b). Table III shows the average, maximum, and minimum voltages for each load. The load voltages are tightly regulated for such a wide variation.

The ripple in the output (Tables II and III) is observed to be 2% or less.



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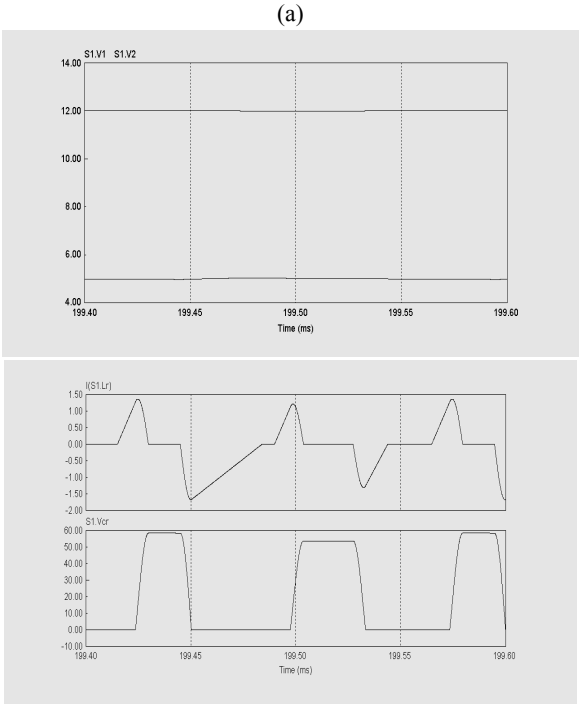

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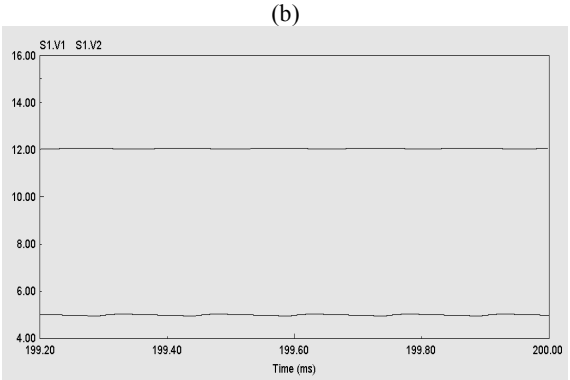
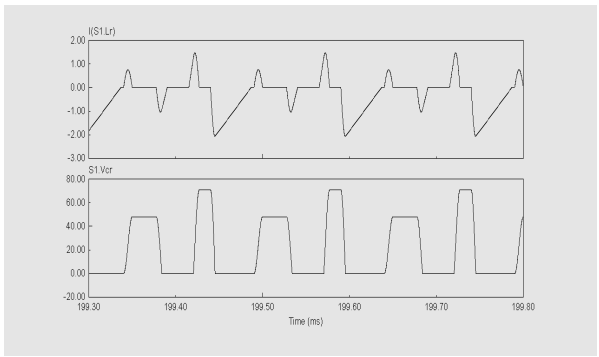
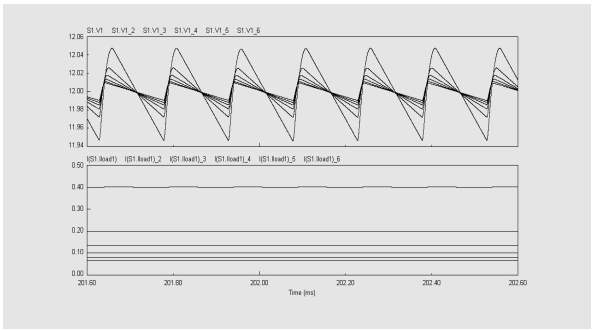




(c)

Fig. 8. (a) Output voltages, inductor current, and capacitor voltage (Vs = 24 V, R1 = 150 Ω, and R2 = 22 Ω). (b) Output voltages, inductor current, and capacitor voltage (Vs = 15 V, R1 = 150 Ω, and R2 = 22 Ω). (c) Output voltages, inductor current, and capacitor voltage (Vs = 24 V, R1 = 180 Ω, and R2 = 15 Ω).



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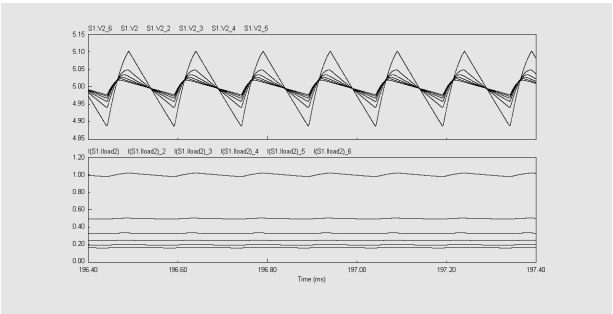
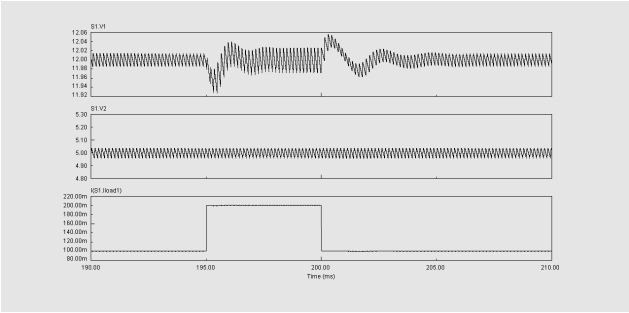


(b)

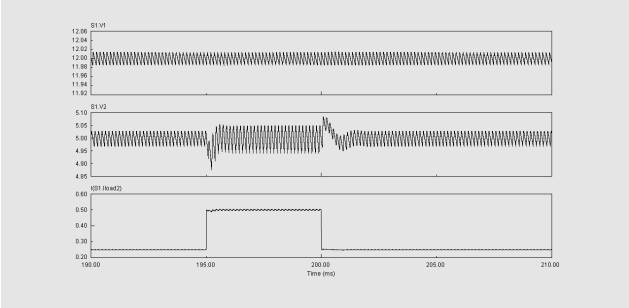
Fig. 9. (a) First output voltage and current (load varies from 30 Ω to 180 Ω in increments of 30 Ω). (b) Second output voltage and current (load varies from 10 Ω to 30 Ω in increments of 5 Ω).

TABLE III
VARIATION OF SECOND OUTPUT VOLTAGE WITH LOAD

Sno	Load	Avg	Max	Min	Ripple
1	10 Ω	4.99948	5.04814	4.94108	2.14%
2	15 Ω	4.99976	5.03440	4.95866	1.51%
3	20 Ω	4.99987	5.02748	4.96794	1.19%
4	25 Ω	4.99992	5.02293	4.97378	0.98%
5	30 Ω	4.99995	5.01970	4.97780	0.84%



(a)



(b)

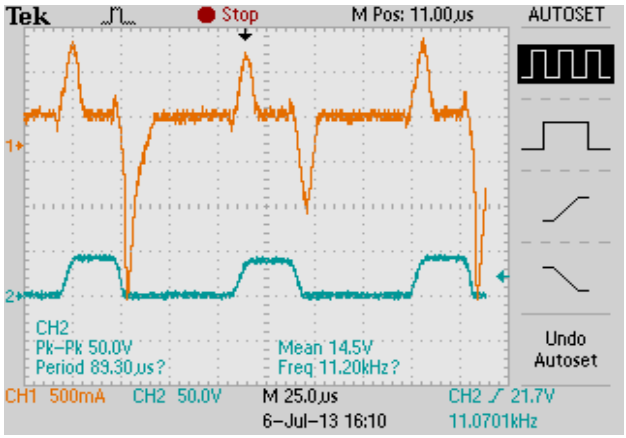
Fig. 10. (a) Output voltages and current (Load 1 changes from 120 Ω → 60 Ω →120 Ω). (b) Output voltages and current (Load 2 changes from 20 Ω → 10 Ω →20 Ω).

The effect of sudden load variation and the corresponding transients are illustrated in Figs. 10a and 10b. Fig. 10a shows the effect of a sudden change in the first output load from 120 Ω to 60 Ω and then back to 120 Ω. Fig. 10b shows the effect of a sudden change in the second output load from 20 Ω to 10 Ω and then back to 20 Ω again. In both cases, the transient variation in the output during the load change is minimal. Furthermore, cross regulation is virtually negligible because the other output is completely unaffected.

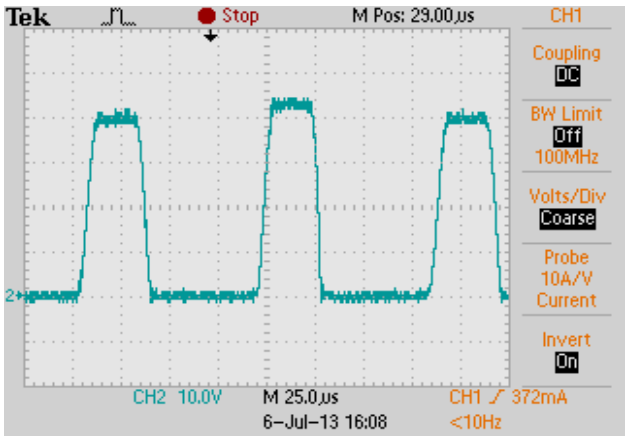
Control range: Control of the output voltage is only possible when $\alpha > 0°$. If either load resistance or supply voltage is high, the output may exceed the set value even at $\alpha = 0°$ and control is lost. If either supply voltage or load resistance is low, the charge and discharge times of the resonant inductor will increase and the current may not reach zero before the beginning of the next cycle. Hence, the design must consider the worst-case values of the load and supply voltage.

Hardware results: The hardware implementation is performed by using a Xilinx Spartan 3 FPGA kit operating at 20 MHz with a XC3S250E FPGA processor. The specifications for the hardware model are same as the specifications in Table I. One pulse is present in Outputs 1 and 2 per cycle. IRF 840 is the switching device, and BYQ28E is the blocking diode. A 20 MHz clock frequency corresponds to a clock time of 50 ns. The total time is 3000 clocks.

The inductor current, resonant capacitor voltage, and output voltage waveforms are shown in Figs. 11a to 11c. The



(a)



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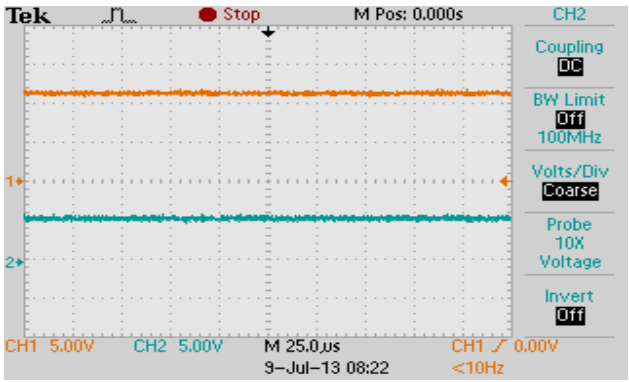
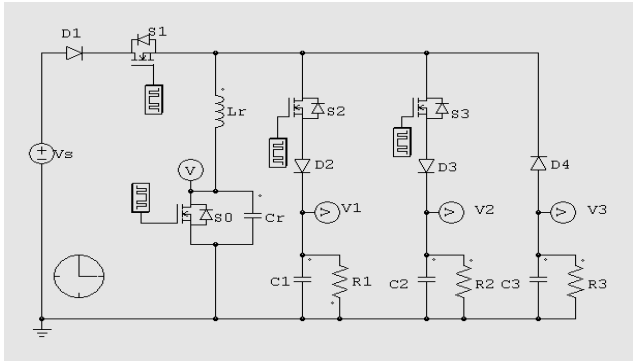


(c)

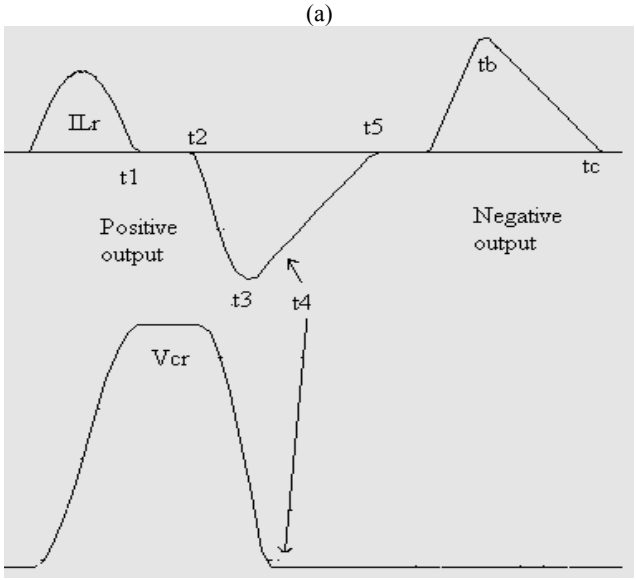
Fig. 11. (a) Inductor current and resonant capacitor voltage. (b) Resonant capacitor voltage. (c) First and second output voltages.

waveforms show that the level of resonant capacitor voltage and the peak charging current differ for each of the two outputs while satisfying the output requirements.

Given the ZCS operation of the switches, switching losses are largely minimized. However, efficiency is around 70% to 75% because of the presence of the reverse blocking diodes and because the converter has low power and voltage. If switches without body diodes are used, the reverse blocking diodes are not required and efficiency improves to 80% to 85%.



(a)



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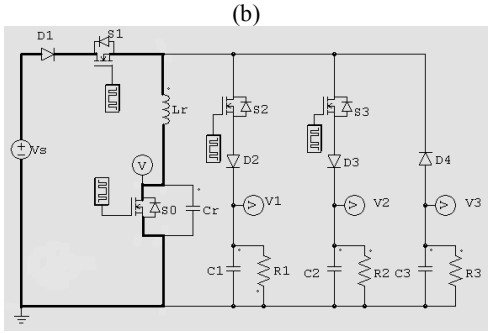

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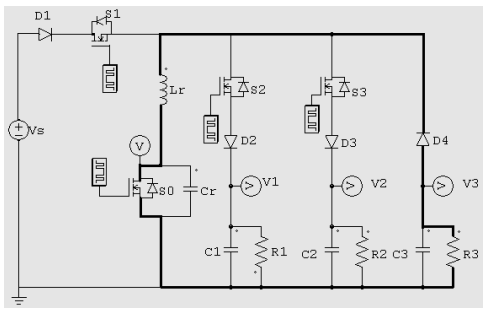

(d)

Fig. 12. (a) Converter with an additional negative output. (b) Inductor current and capacitor voltage waveforms. (c) Mode 11. (d) Mode 12.

VII. Obtaining an Additional Negative Output

The topology discussed above can be easily adapted to obtain an additional negative output without any additional switches. Only a decoupling diode is required additionally. A triple output converter with two positive outputs and an additional negative output is shown in Fig. 12a. The corresponding waveforms of the inductor current and the resonant capacitor voltage are shown in Fig. 12b. The additional modes of operation for the third negative output are shown in Figs. 12c and 12d.

Output voltages *V1* and *V2* are obtained in the manner mentioned above. The third output *V3* with a negative polarity works like a buck-boost converter in discontinuous conduction mode. When S0 and S1 are ON, the resonant inductor *Lr* is charged linearly because the voltage across the inductor is the supply voltage *Vs*. When S1 is turned OFF, the stored energy in the inductor is transferred to the third output through diode D4. The current decreases linearly because the voltage across the inductor is the third output voltage (which is negative).

The output voltage of this negative third output can be regulated by controlling the ON duration of S0 and S1 to charge the inductor *Lr*. A MOSFET is used as switch S0 since it has zero voltage switching both during ON and OFF switching. However, for the negative output, S1 does not have zero current switching when switched OFF. During power transfer in the linear discharge mode for the positive outputs, the body diode of S0 carries the current and performs the function of diode Da in Fig. 1.

The analysis of this converter shows that two additional modes exist for the negative output in addition to the ten modes of operation discussed for the positive outputs above. These two modes can be present anywhere in the switching cycle. In this study, these two modes are present at the end of the cycle.

Mode 11: Once S0 and S1 are turned ON, the resonant inductor *Lr* is charged linearly because the voltage across the inductor is the supply voltage Vs. The rate of increase in the current is given by the following:

$$dI_{Lr}/dt = V_s/L_r \ . \tag{30}$$

At $t = t_b$, the current reaches the following value:

$$I_p = V_s\, t_b/L_r \ . \tag{31}$$

Mode 12: S1 is turned OFF and the stored energy in the inductor is transferred to the third output through diode D4. The current decreases linearly because the voltage across the inductor is the third output voltage (which is negative). The rate of decrease in the current is given by the following:

$$dI_{Lr}/dt = -V3/L_r \ . \tag{32}$$

TABLE IV

CONVERTER SPECIFICATIONS

Rated supply	24 V
First output	5 V, 220 Ω
Second output	2.3 V, 50 Ω
Third output	−5 V, 72 Ω

By substituting I_p for dI_{Lr}, the time required for the current to become zero is expressed as follows:

$$t_c = V_s t_b / V3 . \quad (33)$$

The output voltage of this negative third output can be regulated by controlling the ON duration of S0 and S1 in Mode 11 to charge the inductor *Lr* (i.e., t_b). Given that the outputs are time multiplexed and the inductor is fully discharged into each output during its cycle, no cross regulation occurs.

The energy stored in the inductor at $t = t_b$ in Mode 11 is completely transferred to the filter capacitor of the third output in Mode 12. The filter capacitor supplies power to the load at other times. By considering energy balance, the following is obtained:

$$(1/2)L_r I_p^2 = V_3^2 T_s / R3 , \quad (34)$$

$$V3 = \sqrt{L_r I_p^2 R3 / 2T_s} . \quad (35)$$

By substituting for I_p from Eq. (31), we obtain the following:

$$V3 = \sqrt{V_s^2 t_b^2 R3 / 2T_s L_r} . \quad (36)$$

Given that *Lr* and T_s are fixed because of other positive outputs, t_b can be adjusted for each change in Vs and / or R3 to maintain V3 at the required value. t_b can be obtained as follows:

$$t_b = \sqrt{2V_3^2 T_s L_r / V_s^2 R3} . \quad (37)$$

Hence, the resonant inductor is charged for a duration of t_b seconds in Mode 11 in every switching cycle, and this power is discharged into the third output for a duration of t_c seconds in Mode 12 (Fig. 8(b)).

The specifications for hardware validation are shown in Table 4. A full switching cycle consists of a charge/discharge sequence for each of the positive outputs and an inductor charge/discharge sequence for the third negative output.

However, to achieve the required power for the third output, a single inductor charge/discharge sequence for the third negative output results in an inductor current that is greater than the corresponding positive output. Hence, to limit the peak value of the inductor current, the charge/discharge sequence for the third output is done twice per cycle.

The resonant inductor current and output voltage waveforms are shown in Fig. 13. The hardware setup is shown in Fig. 14.

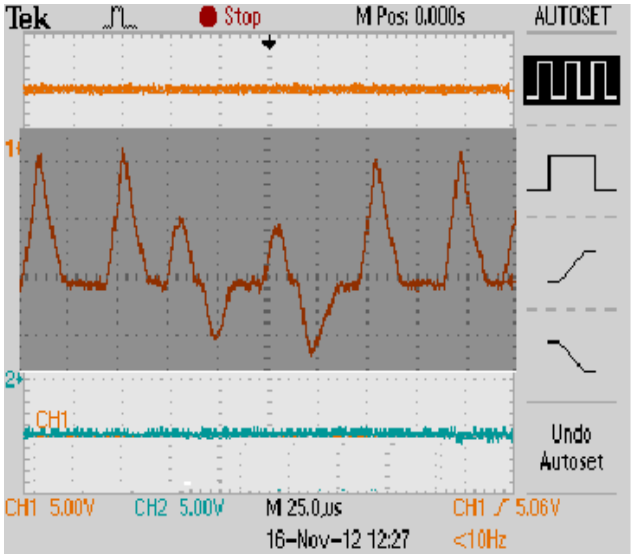

Fig. 13. Resonant inductor current and output voltages.

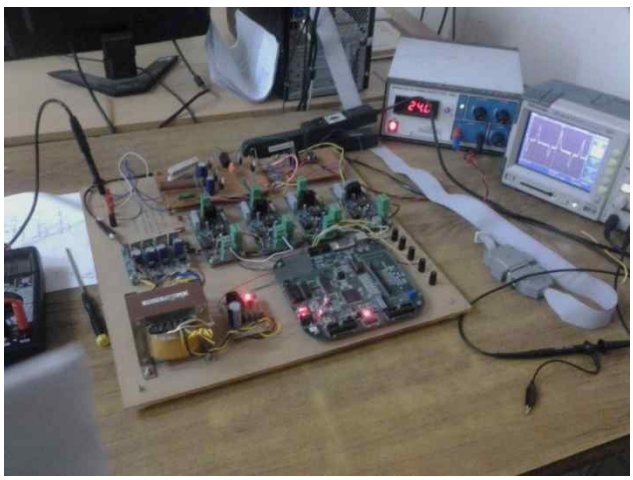

Fig. 14. Hardware setup.

VIII. CONCLUSIONS

This study proposes a novel control scheme for a switched-resonant converter that is capable of achieving and regulating any combination of output voltages (both positive and negative). An additional negative output is achieved with the addition of only one diode. The topology is scalable to any number of outputs by adding a switch to each additional output. Steady state analysis is performed for the proposed converter, and the design considerations are explained. The simulation results and hardware implementation are validated by using an FPGA system.

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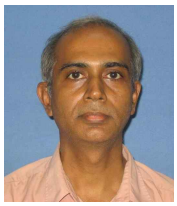

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