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High-Efficiency Supercapacitor Charger Using an Improved Two-Switch Forward Converter

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Abstract

This paper proposes a high-efficiency supercapacitor charger. Conventional two-switch forward converter can be used for charging supercapacitors. However, the efficiency of conventional converters is low because of their switching losses. This study presents a high-efficiency two-switch forward converter for supercapacitor chargers. The proposed converter improves power efficiency by 4 %, from 89 % to 93 %. The proposed converter has the advantages of reduced switch voltage stresses and minimized circulating current when compared to other converter topologies. The performance of the proposed converter is evaluated by experimental results using a 300 W prototype circuit for a 54-V, 35-F supercapacitor bank.

Key words: Forward converter, High-efficiency, Supercapacitor charger, Switching loss

I. INTRODUCTION

Supercapacitors have been widely used for automotive and energy conversion systems [1]-[3]. The life and capacity of supercapacitors depend on several factors such as charge mode, maintenance, temperature, and age [4]. Among these factors, the charge mode has the greatest impact on battery life and capacity. Supercapacitors are charged with current and voltage levels by a supercapacitor charger [5]. The supercapacitor charger is designed by using switched mode power supplies. The basic requirements for supercapacitor chargers are small size and high efficiency. A high switching frequency is necessary to achieve a small size. However, as the switching frequency is increased, the efficiency of the supercapacitor chargers is reduced because the switching losses increase. Thus, selecting an optimal converter topology is important for the design of high-efficiency supercapacitor chargers.

The forward converter is a popular DC-DC converter topology for low voltage and high current applications [6], [7]. In particular, the two-switch forward converter in Fig. 1 is a good candidate for supercapacitor chargers due to its simple structure and low switch voltage stress [8]-[11]. The two switches S_1 and S_2 are turned on and off simultaneously [10].

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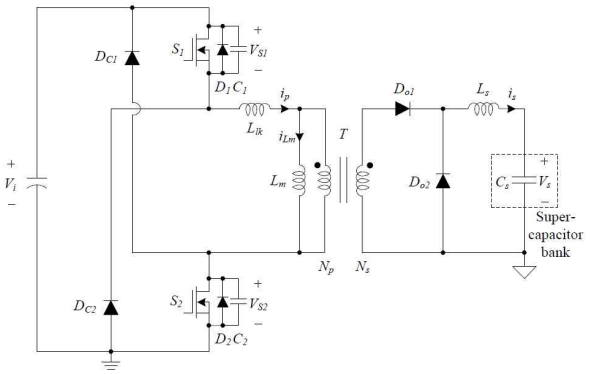


Fig. 1. Circuit diagram of the conventional two-switch forward converter.

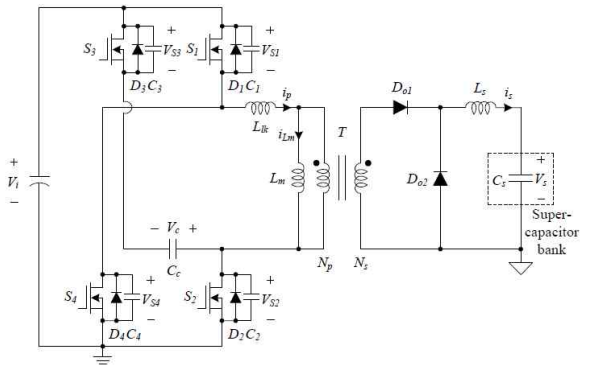


Fig. 2. Circuit diagram of the proposed two-switch forward converter.

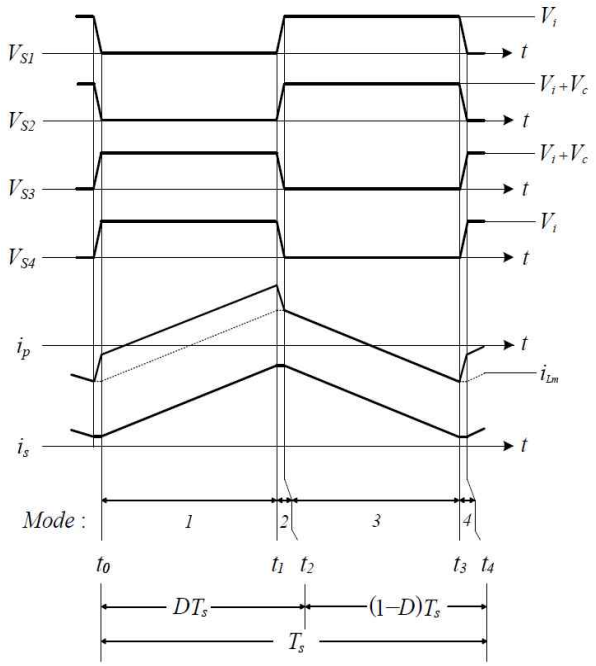


Fig. 3. Switching waveforms of the proposed converter.

The magnetizing current i_{Lm} flows into the input source V_i through the reset diodes D_{C1} and D_{C2}. Thus, the two-switch forward converter can eliminate the need for a separate demagnetizing winding, which is used in the conventional forward converter. However, when the switches are turned off, the energy stored in the leakage inductor L_{lk} causes high voltage spikes across the switches [11]. These voltage spikes increase the switching losses. Another drawback of the two-switch forward converter is a duty cycle limitation [12]. The maximum duty cycle is limited to 0.5 to guarantee the transformer reset. This small duty cycle operation increases the output filter size and current stress. To cope with these problems, the active-clamping method has recently been applied to the two-switch forward converter [13], [14]. By using one more power switches in the primary side, zero-voltage switching of the power switches is achieved. However, the voltage stress of the auxiliary switch for the active-clamping circuit is still high. As a result, high-cost switches are usually used.

To relieve the abovementioned drawbacks, a high-efficiency two-switch forward converter is proposed for supercapacitor chargers. The proposed converter in Fig. 2 can reduce switching losses. The two reset diodes are replaced by two auxiliary switches S_3 and S_4. As a result, all of the power switches operate without any voltage spikes. Switching losses can be reduced by zero-voltage switching of the power switches. The duty cycle range is also extended by using one clamping capacitor C_c. Thus, the proposed converter can be used for a high input voltage range of around 300 V ~ 400 V. In addition, the proposed converter has the advantages of reduced switch voltage stresses and minimized circulating current when compared to the other converter topologies. The supercapacitor charging strategy is presented by using a constant current and constant voltage charging control [15]. All of the control functions are implemented in software with a single-chip microcontroller. The proposed converter is realized with minimal hardware at a low-cost. The performance of the proposed converter is evaluated through experimental results by using a 300 W prototype circuit for a 54-V, 35-F supercapacitor bank. The proposed converter improves the converter efficiency by 4 %, from 89 % to 93 %.

II. PROPOSED CONVERTER

A. Converter Operation

Fig. 2 shows a circuit diagram of the proposed converter. V_i is the input voltage. V_s is the supercapacitor voltage. The primary part consists of power switches (S_1, S_2, S_3, S_4), a clamping capacitor (C_c), and a transformer (T). The power switches are considered to be ideal switches except body diodes $D_1 \sim D_4$ and output capacitors $C_1 \sim C_4$. The transformer T has a magnetizing inductor L_m and leakage inductor L_{lk} with a turns ratio of 1 : N where $N = N_s / N_p$. The secondary part consists of output diodes (D_{o1}, D_{o2}), an output filter inductor (L_s), and a supercapacitor bank (C_s).

Fig. 3 shows the switching waveforms of the proposed converter during one switching period T_s. The converter has four switching modes during T_s. S_1 and S_2 are turned on and off simultaneously. S_3 and S_4 are also turned on and off simultaneously. Then, S_1 (S_2) and S_3 (S_4) operate complementarily with a short dead time. When the duty cycle D is based on the on-time of S_1 and S_2, the duty cycle of S_3 and S_4 is $1 - D$. Before $t = t_0$, S_3 and S_4 are turned off. Voltages V_{S1} and V_{S2} are zero when the primary current i_p flows through body diodes D_1 and D_2.

Mode 1 [t_0, t_1]: At $t = t_0$, S_1 and S_2 are turned on at zero voltage. L_m and L_{lk} store energy from V_i. The magnetizing inductor current i_{Lm} increases linearly as

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_i}{L_m + L_{lk}}(t - t_0). \quad (1)$$

At the secondary side, output diode D_{o1} is turned on. The output inductor current i_s flows through output diode D_{o1}.

Mode 2 [t_1, t_2]: At $t = t_1$, S_1 and S_2 are turned off. The primary current i_p charges C_1 and C_2 and discharges C_3 and C_4. V_{S1} increases from zero to V_i while V_{S2} increases from zero to $V_i + V_c$. V_{S3} decreases from $V_i + V_c$ to zero while V_{S4} decreases from V_i to zero. Since the switch output capacitor C_s (= $C_1 = C_2 = C_3 = C_4$) is very small, the time interval during this mode is considered negligible when compared to T_s. The magnetizing current i_{Lm} is considered to be constant. Switch body diodes D_3 and D_4 conduct the primary current i_p at the end of this mode.

Mode 3 [t_2, t_3]: At $t = t_2$, S_3 and S_4 are turned on at zero voltage. The energy stored in L_{lk} is recycled to the clamping

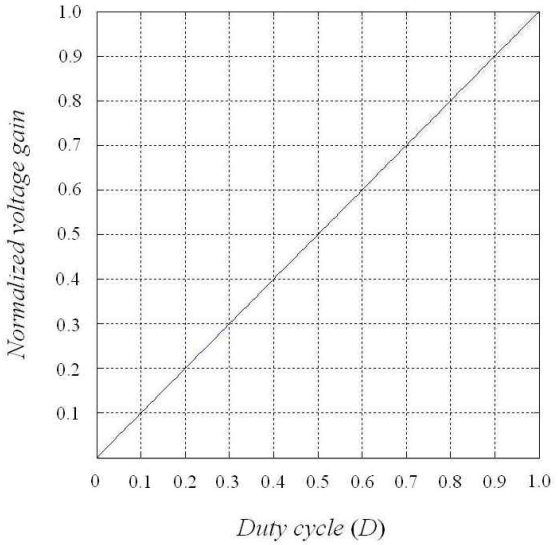


Fig. 4. Graph for the normalized voltage gain between the input voltage V_i and supercapacitor voltage V_s.

capacitor C_c. S_3 and S_4 are turned on without any voltage spikes. The magnetizing inductor current i_{Lm} decreases linearly as:

$$i_{Lm}(t) = i_{Lm}(t_2) - \frac{(V_i + V_c)}{L_m + L_{lk}}(t - t_2). \quad (2)$$

At the secondary side, output diode D_{o2} is turned on. The output inductor current i_s freewheels through output diode D_{o2}.

Mode 4 [t_3, t_4]: At $t = t_3$, S_3 and S_4 are turned off. The primary current i_p charges C_3 and C_4 and discharges C_1 and C_2. V_{S1} decreases from V_i to zero while V_{S2} decreases from $V_i + V_c$ to zero. V_{S3} increases from zero to $V_i + V_c$ while V_{S4} increases from zero to V_i. Switch body diodes D_1 and D_2 conduct the primary current i_p. The next switching cycle begins when S_1 and S_2 are turned on at zero voltage again.

B. Circuit Analysis

The voltage stress of S_1 and S_4 is clamped to the input voltage V_i. The voltage stress of S_2 and S_3 is clamped to the sum of V_i and V_c. For the volt-second balance relation on L_m during T_s, the following relation between V_i and V_c is obtained as:

$$V_i D T_s - (V_i + V_c)(1 - D)T_s = 0. \quad (3)$$

By rearranging (3), the clamp capacitor voltage V_c is derived as:

$$V_c = \frac{2D - 1}{1 - D} V_i. \quad (4)$$

For the volt-second balance relation on L_s during T_s, the following relation between V_i and V_s is obtained as:

$$\frac{V_s}{V_i} = ND. \quad (5)$$

Fig. 4 shows a graph of the normalized voltage gain between V_i and V_s. As the duty cycle D varies from zero to one, the normalized voltage gain increases linearly. When compared to the duty cycle of the previous two-switch forward converter [10], the proposed converter has a wide duty cycle range from zero to one. In particular, when the duty cycle D is below 0.5, the clamping capacitor voltage V_c can be lower than the input voltage V_i.

C. Zero-Voltage Switching Conditions

In order to achieve zero-voltage switching of S_3 and S_4, the energy stored in L_m and L_s should be larger than the energy stored in the switch output capacitors, as suggested in [16]. The zero-voltage switching condition of S_3 and S_4 is:

$$\frac{L_m i_{Lm}^2(t_2)}{2} + \frac{L_s i_{Do1}^2(t_2)}{2} > \frac{(C_1 + C_4)}{2} V_i^2 + \frac{(C_2 + C_3)}{2}(V_i + V_c)^2. \quad (6)$$

Similarly, in order to achieve zero-voltage switching of S_1 and S_2, the energy stored in L_m and L_s should be larger than the energy stored in the switch output capacitors. The zero-voltage switching condition of S_1 and S_2 is:

$$\frac{L_m i_{Lm}^2(t_4)}{2} + \frac{L_s i_{Do2}^2(t_4)}{2} > \frac{(C_1 + C_4)}{2} V_i^2 + \frac{(C_2 + C_3)}{2}(V_i + V_c)^2. \quad (7)$$

D. Voltage and Current Stresses

In the proposed converter, the voltage stress of S_1 and S_4 is clamped to the input voltage. On the other hand, the voltage stress of S_2 and S_3 is the sum of the input voltage and the clamping capacitor voltage. The voltage stress of S_2 and S_3 can be changed with the duty ratio D. When the duty cycle D is below 0.5, the voltage stress of S_2 and S_3 can be lower than the input voltage V_i. This is one of the advantages of the proposed converter when compared to the other full-bridge (FB) converter topologies. Table I summarizes the voltage and current stresses of the proposed converter.

E. Circulating Current

In the phase-shifted full-bridge (PSFB) converter [17], a circulating current is inevitable during the freewheeling period. It is especially large at a high input voltage, causing the large conduction losses associated with the transformer and primary switches. This is because there exists a non-powering period, as shown in Fig. 5(a), where a zero voltage is applied to the transformer winding. The power is not delivered to the secondary side even though the current is circulating at the primary side. On the other hand, in the proposed converter, there is no freewheeling period except for a small dead-time period, as shown in Fig. 5(b). The power can always be delivered to the secondary side. There is no zero voltage period across the transformer winding. This is another advantage of the proposed converter when compared to the FB converter topologies.

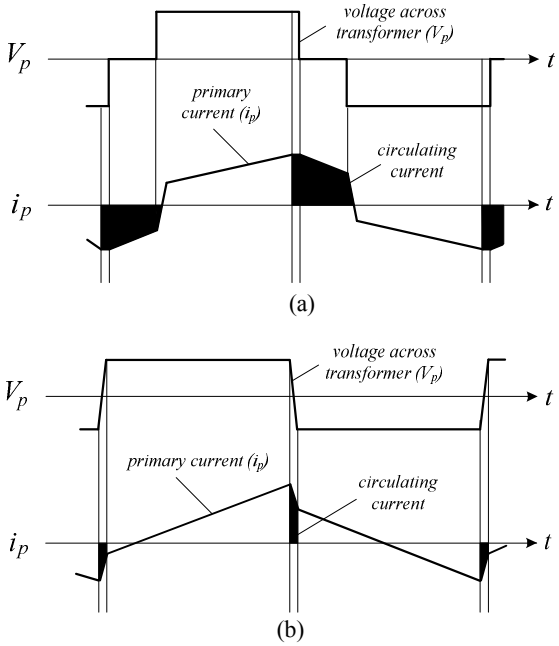


Fig. 5. Comparison of key waveforms between the PSFB converter and proposed converter: (a) PSFB converter and (b) proposed converter.

TABLE I

VOLTAGE AND CURRENT STRESSES OF THE RROPOSED CONVERTER

Switch	Voltage Stress	Current Stress
S_1	V_i	$Ni_o + \frac{V_i}{2L_m}DT_s$
S_2	$V_i + V_c = \frac{D}{1-D}V_i$	$Ni_o + \frac{V_i}{2L_m}DT_s$
S_3	$V_i + V_c = \frac{D}{1-D}V_i$	$Ni_o - \frac{V_i + V_c}{2L_m}(1-D)T_s$
S_4	V_i	$Ni_o - \frac{V_i + V_c}{2L_m}(1-D)T_s$

F. Averaged Model

In the proposed converter, the switch power stage, together with the transformers and rectifier, can be substituted with an equivalent pulse source V_g, as illustrated in Fig. 6. This pulsating source can be averaged to a constant dc voltage source V_d. Assume that the output filter inductor current is in the continuous-conduction mode. The average model can then be derived as an equivalent buck converter topology, with an equivalent switching frequency. By using the state-space averaging method [18], the state-space averaged dc model is expressed as:

$$0 = A \cdot \begin{bmatrix} I_s \\ V_s \end{bmatrix} + B \cdot V_d \tag{8}$$

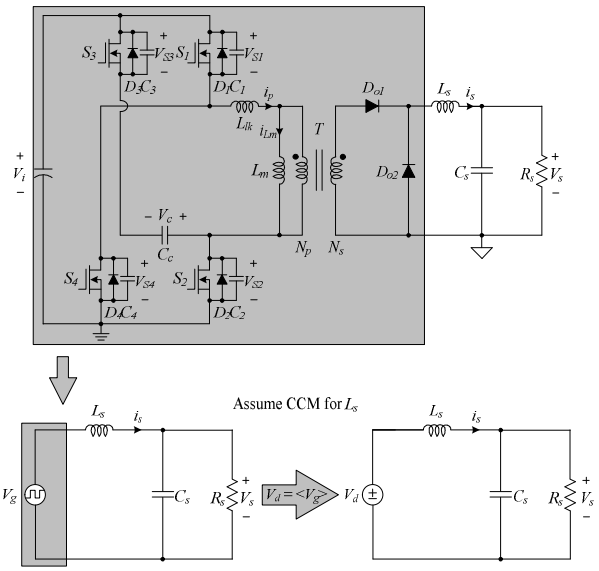


Fig. 6. Derivation of the average model.

where:

$$A = \begin{bmatrix} 0 & -\frac{1}{L_s} \\ \frac{1}{C_s} & -\frac{1}{C_s R_s} \end{bmatrix} \quad B = \begin{bmatrix} \frac{D}{L_s} \\ 0 \end{bmatrix}$$

where R_s is the equivalent resistance of the supercapacitor bank. Solving (8), the following equations can be obtained as:

$$I_s = \frac{D}{R_s} \cdot V_d \tag{9}$$

$$V_s = DV_d \tag{10}$$

The state-space averaged ac model is expressed as:

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_s \\ \hat{v}_s \end{bmatrix} = C \cdot \begin{bmatrix} \hat{i}_s \\ \hat{v}_s \end{bmatrix} + D \cdot V_d \cdot \hat{d} \tag{11}$$

where:

$$C = \begin{bmatrix} 0 & -\frac{1}{L_s} \\ \frac{1}{C_s} & -\frac{1}{C_s R_s} \end{bmatrix} \quad D = \begin{bmatrix} \frac{1}{L_s} \\ 0 \end{bmatrix}$$

where $\hat{d}$ is the small-signal duty ratio. Solving (11), the following equations can be obtained as:

$$\frac{\hat{v}_s}{\hat{d}} = \frac{\frac{\hat{i}_s}{C_s}}{s + \frac{1}{C_s R_s}} \cdot \frac{1}{\hat{d}} \tag{12}$$

$$\frac{\hat{i}_s}{\hat{d}} = \frac{V_d}{sL_s + \frac{1}{\frac{1}{R_s} + sC_s}} \tag{13}$$

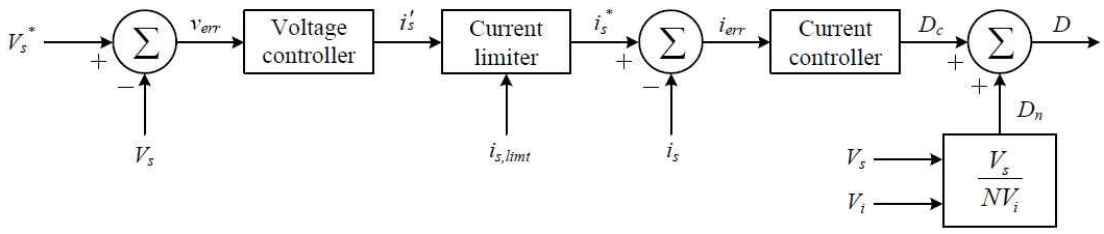


Fig. 7. Control block diagram of the supercapacitor charging controller.

III. CONTROL STRATEGY

Fig. 7 shows a control block diagram of the proposed converter. It is assumed that the output filter inductor current i_s flows continuously. When S_1 and S_2 are turned on, the inductor current i_s increases. The following voltage equation is obtained as:

$$NV_i - L_s \frac{di_s}{dt} - V_s = 0 . \tag{14}$$

On the other hand, when S_3 and S_4 are turned on, the inductor current i_s freewheels through diode D_{o2}. Then, the following voltage equation is obtained as:

$$V_s - L_s \frac{di_s}{dt} = 0 . \tag{15}$$

Depending on the duty cycle D of S_1 and S_2, the average inductor voltage for T_s gives the supercapacitor current variation Δi_s as:

$$(NV_i - V_s)DT_s - V_s(1-D)T_s = L_s \Delta i_s . \tag{16}$$

By rearranging (14):

$$NV_i D = V_s + L_s \frac{\Delta i_s}{T_s} . \tag{17}$$

Here, the duty cycle D is represented as:

$$D = D_n + D_c . \tag{18}$$

D_n is a nominal duty cycle. D_c is a controlled duty cycle. The nominal duty cycle D_n and the controlled duty cycle D_c can be represented as:

$$D_n = \frac{V_s}{NV_i} \tag{19}$$

$$D_c = L_s \frac{\Delta i_s}{NV_i T_s} . \tag{20}$$

Then, the duty cycle D becomes

$$D = D_n + D_c = \frac{V_s}{NV_i} + L_s \frac{\Delta i_s}{NV_i T_s} . \tag{21}$$

To force the supercapacitor current i_s to track its current command i_s^*, a proportional-integral (PI)-type current controller is used for the controlled duty cycle D_c as:

$$D_c = k_p i_{err} + k_i \int i_{err} dt \tag{22}$$

$$i_{err} = i_s^* - i_s . \tag{23}$$

The current error i_{err} is calculated by comparing the current command i_s^* to the measured current i_s. k_p and k_i are the proportional and integral control gains, respectively. To regulate the supercapacitor voltage V_s, a PI-type voltage controller is used. The voltage error v_{err} is calculated by comparing the reference supercapacitor voltage V_s^* to the measured supercapacitor voltage V_s. The voltage controller generates the current command i_s'. $i_{s.limit}$ is the maximum charging current of the supercapacitor. If i_s' is higher than $i_{s.limit}$, the supercapacitor is charged with a constant current. On the other hand, if i_s' is lower than $i_{s.limit}$, the supercapacitor is charged with a constant voltage.

IV. EXPERIMENTAL RESULTS

A 300 W prototype circuit has been built and tested to verify the operation principles and performance of the proposed converter. The input voltage ranges from 300 V to 400 V. The supercapacitor voltage ranges from 30 V to 48 V. Table II shows the values of the major circuit parameters. For the power switching devices, $S_1 = S_2 = S_3 = S_4$ = FQA24N50C3 (Fairchild) and $D_{o1} = D_{o2}$ = DSEK6002A (IXYS) are used. The current stresses of the switching devices are different, as shown in Table I. The proposed converter adopts FQA24N50C3s for all of the four switches by considering the maximum current stresses of the switches. The FQA24N50C3 (24 A, 500 V) can withstand the maximum allowable current stresses of all of the power switches. The power switches operate at a constant switching period of 20 μsec with a dead time of 330 nsec. The transformer has a primary winding turns of N_p = 20 and a secondary winding turns of N_s = 10. The controller is digitally implemented by using a single-chip microcontroller dsPIC30F3011 (Mircochip).

The input voltage V_i, supercapacitor voltage V_s, and supercapacitor current i_s are measured by voltage and current sensing amplifiers. They are sensed through the 10-bit A/D converter in the microcontroller. After the voltage and current signals are read, the duty cycle D is obtained by calculating D_n and D_c. Fig. 8 shows a picture of the hardware prototype including the proposed converter. The designed prototype system includes a power-factor correction circuit and the proposed dc-dc converter.

In order to verify the proposed converter operation and its

TABLE II

MAIN CIRCUIT PARAMETERS

Circuit parameter	Value
input voltage V_i	300 V ~ 400 V
supercapacitor voltage V_s	30 V ~ 48 V
switch output capacitor C_s	500 pF
clamping capacitor C_c	1 μF
transformer turns ratio N	0.36
magnetizing inductor L_m	250 μH
leakage inductor L_{lk}	4 μH
output filter inductor L_s	360 μH

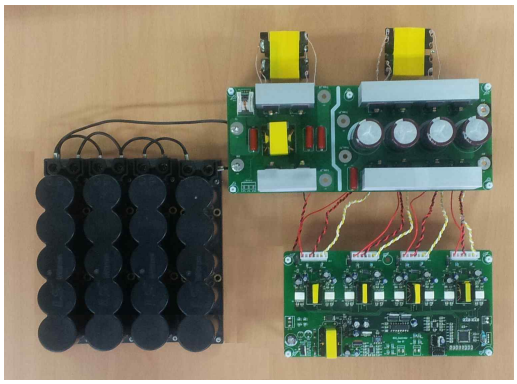


Fig. 8. Picture of the hardware prototype including the proposed converter.

control method, simulation results are presented in Fig. 9 through Fig. 11 by using PSIM 9.0 software. In the simulation, the control block is implemented by C-language-based DLL blocks. Fig. 9 shows the simulation waveforms when D is 0.4. Fig. 9(a) shows the primary current i_p and switch voltages V_{S1} and V_{S4}. Fig. 9(b) shows the primary current i_p and switch voltages V_{S2} and V_{S3}. Fig. 10 shows the simulation waveforms when D is 0.6. It is shown that the proposed converter can operate when the duty cycle is over 0.5. It is also shown that all of the power switches are turned on at zero-voltage without any voltage spikes. Fig. 11 shows the simulation waveforms of the proposed converter for charging the supercapacitor banks. C_s = 35-F and R_s = 4.5 mΩ are used for the supercapacitor bank parameters. As shown in Fig. 11, as the proposed converter supplies a constant current of 15 A, the supercapacitor bank increases linearly. When the supercapacitor voltage reaches the maximum allowable voltage at 48 V, the supercapacitor voltage is regulated constantly and the current decreases.

The conventional two-switch forward converter in [11] has been designed and tested for a performance comparison with the proposed converter. Fig. 12 shows the experimental waveforms of the conventional two-switch forward converter. It shows the primary current i_p and switch voltages V_{S1} and V_{S2}

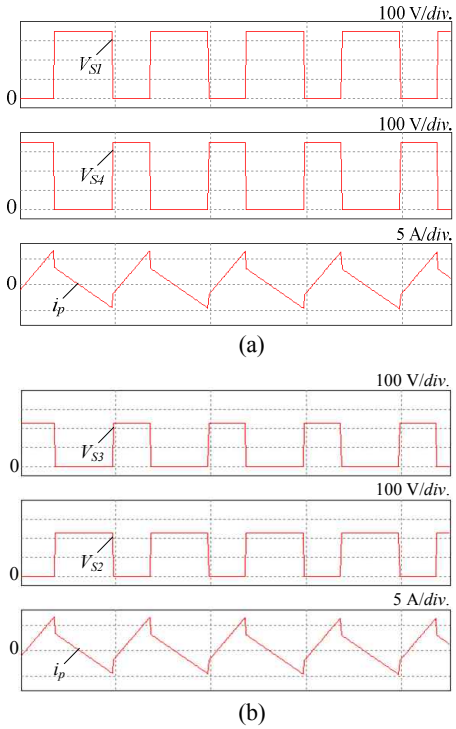


Fig. 9. Simulation results of the proposed converter when D is 0.4: (a) primary current i_p and switch voltages V_{S1} and V_{S4} and (b) primary current i_p and switch voltages V_{S2} and V_{S3}.

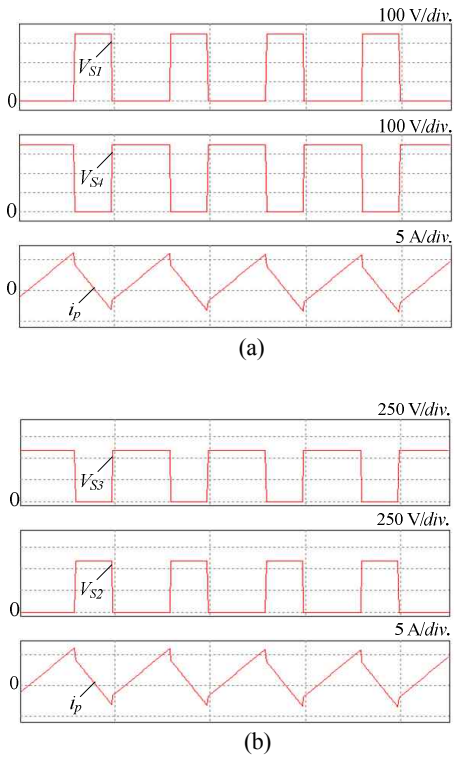


Fig. 10. Simulation results of the proposed converter when D is 0.6: (a) primary current i_p and switch voltages V_{S1} and V_{S4} and (b) primary current i_p and switch voltages V_{S2} and V_{S3}.

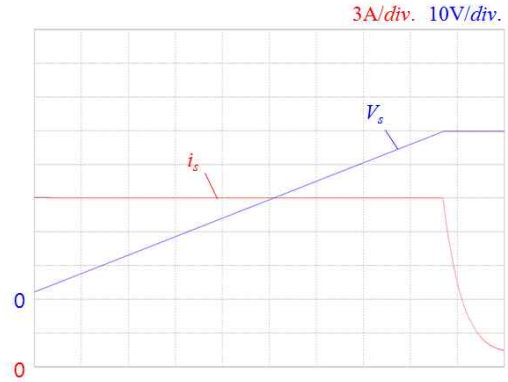


Fig. 11. Simulation waveforms of the proposed converter for charging the supercapacitor banks.

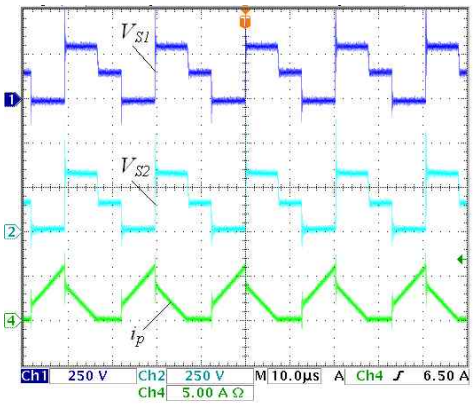


Fig. 12. Experimental waveforms of the conventional converter: primary current i_p and switch voltages V_{S1} and V_{S2}.

of the conventional two-switch forward converter. When the switches are turned off, high voltage spikes are observed in Fig. 12. These voltage spikes increase the switching losses. Fig. 13 shows the experimental waveforms of the proposed converter when the duty cycle D is 0.4. Fig. 13(a) shows the primary current i_p and switch voltages V_{S1} and V_{S4}. Fig. 13(b) shows the primary current i_p and switch voltages V_{S2} and V_{S3}. As shown in Fig. 13(a) and (b), when the switches are turned off, voltage spikes are not observed across the switches. Fig. 13(c) shows switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2}. Fig. 13(d) shows switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4}. As shown in Fig. 13(c) and (d), before the primary current i_p changes its direction, the switch voltage is zero. Zero-voltage switching of the power switches is achieved, which significantly reduces the switching power losses.

Fig. 14 shows the experimental waveforms of the proposed converter when the duty cycle D is 0.6. Fig. 14(a) shows the primary current i_p and switch voltages V_{S1} and V_{S4}. Fig. 14(b) shows the primary current i_p and switch voltages V_{S2} and V_{S3}. As shown in Fig. 14(a) and (b), zero-voltage switching of the power switches is achieved when the duty cycle D is 0.6. It can also be seen that the proposed converter can operate when the duty cycle is over 0.5. Fig. 15 shows the experimental waveforms when the proposed converter charges the

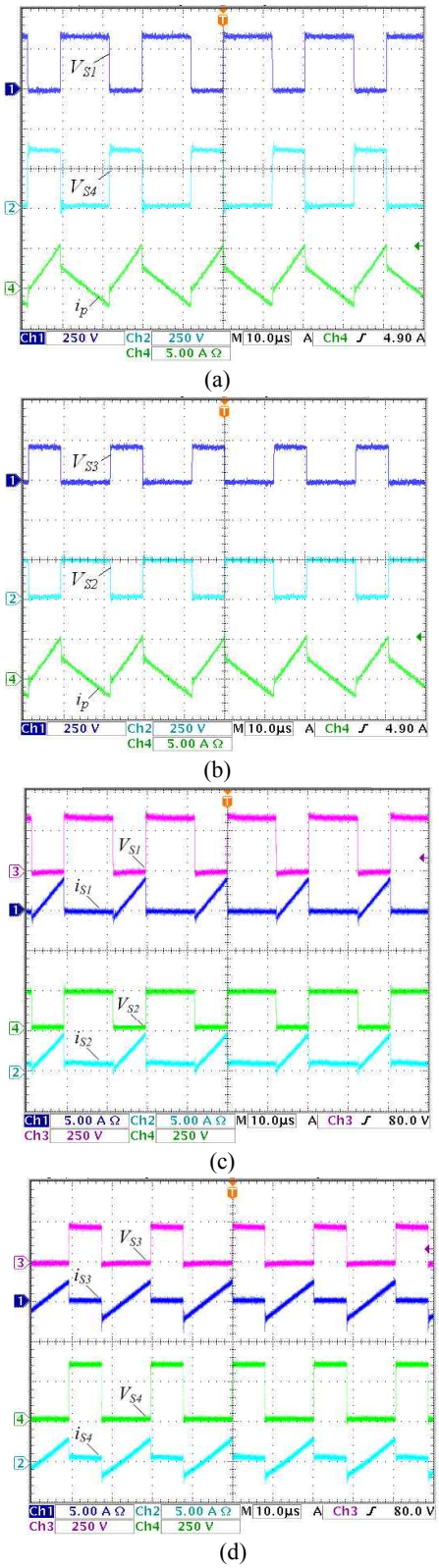
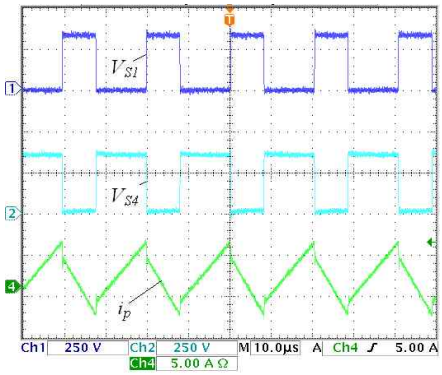
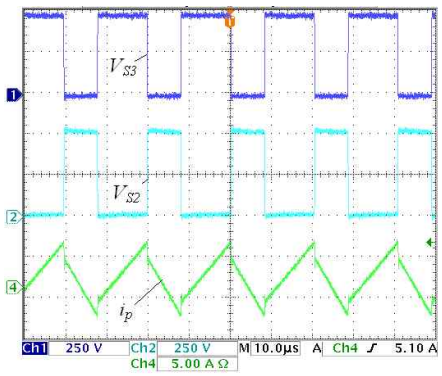


Fig. 13. Experimental waveforms of the proposed converter when D is 0.4: (a) primary current i_p and switch voltages V_{S1} and V_{S4}, (b) primary current i_p and switch voltages V_{S2} and V_{S3}, (c) switch voltages V_{S1} and V_{S2} and switch currents i_{S1} and i_{S2} and (d) switch voltages V_{S3} and V_{S4} and switch currents i_{S3} and i_{S4}.



(a)



(b)

Fig. 14. Experimental waveforms of the proposed converter when D is 0.6: (a) primary current i_p and switch voltages V_{S1} and V_{S4} and (b) primary current i_p and switch voltages V_{S2} and V_{S3}.

supercapacitor bank. A supercapacitor bank is used, which consists of 20 supercapacitors connected in series. The rated capacitance per capacitor is 700 F. Its rated voltage is 2.7 V. Its equivalent resistance is 4.5 mΩ. The total equivalent resistance of the supercapacitor bank is 90 mΩ. As shown in Fig. 15, the proposed converter charges the supercapacitor bank by controlling the output filter inductor current i_s. The supercapacitor voltage increases from 35 V to 40 V linearly when the current command i_s^* is 3 A.

Fig. 16 shows the experimental waveforms when the supercapacitor voltage V_s reaches a maximum voltage of 48 V. It also shows the supercapacitor voltage V_s and the output filter inductor current i_s. The output filter inductor current i_s flows continuously. Fig. 17 shows the dynamic response of the proposed converter when it charges the supercapacitor bank with a constant current of 15 A. As the proposed converter supplies a constant current of 15 A, the supercapacitor bank increases linearly. At the moment that the supercapacitor voltage reaches the maximum allowable voltage at 48 V, the supercapacitor voltage is regulated constantly and the current decreases. In order to evaluate the efficiency, the conventional two-switch forward converter [11] and the proposed converter have been tested for the same power level. Fig. 18 shows the measured efficiencies of the converters for different power

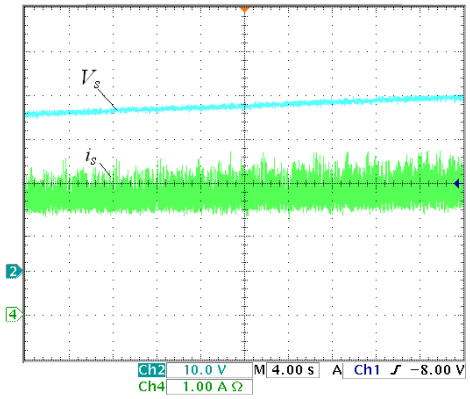


Fig. 15. Experimental waveforms of the proposed converter for charging the supercapacitor bank: supercapacitor voltage V_s and output filter inductor current i_s.

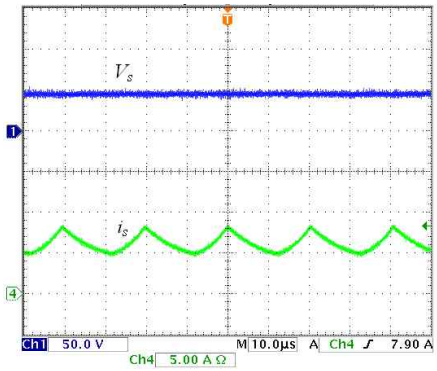


Fig. 16. Experimental waveforms of the proposed converter for charging the supercapacitor bank: supercapacitor voltage V_s and output filter inductor current i_s.

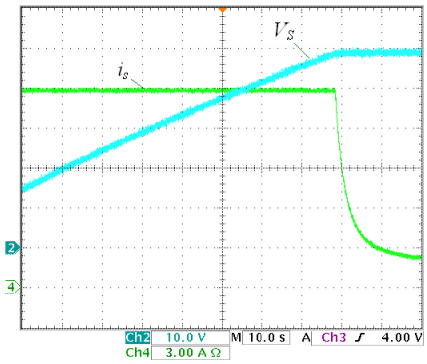


Fig. 17. Experimental waveforms of the proposed converter for charging the supercapacitor bank: supercapacitor voltage V_s and output filter inductor current i_s.

levels. The conventional two-switch forward converter achieves an efficiency of 89 % for 300 W. On the other hand, the proposed converter achieves an efficiency of 93 % for 300 W. The proposed converter improves the converter efficiency by 4 % by achieving zero-voltage switching of the power switches. The duty cycle range is also extended for the use of the proposed converter at a high input voltage range of around 300 V to 400 V. In order to compare the efficiency of the

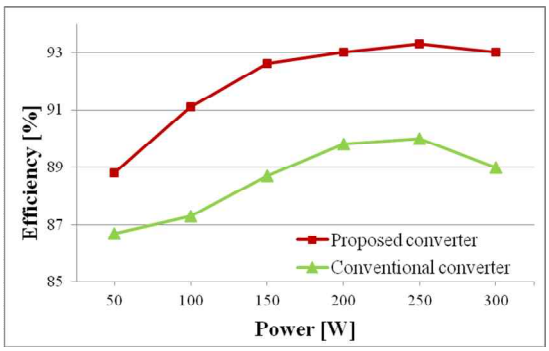


Fig. 18. Measured efficiencies for different power levels.

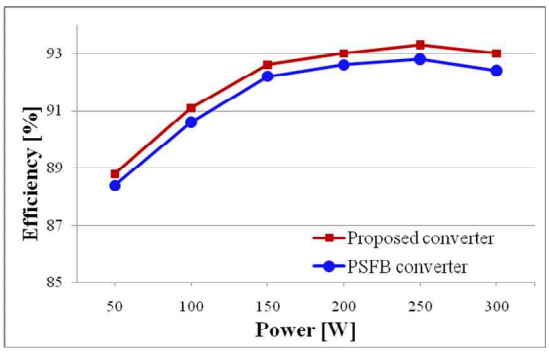


Fig. 19. Measured efficiencies for different power levels.

proposed converter with that of the PSFB converter [17], Fig. 19 shows the measured efficiencies of the converters for different power levels. The PSFB converter achieves an efficiency of 92.5 % while the proposed converter achieves an efficiency of 93 % for 300 W. The proposed converter improves the converter efficiency by 0.5 % by reducing the voltage stresses and by minimizing the circulating currents.

V. CONCLUSIONS

This paper proposed a high-efficiency two-switch forward converter for supercapacitor chargers. The proposed converter reduces switching losses with an extended duty cycle. The power switches are turned on at zero voltage without any voltage spikes. Zero-voltage switching of the power switches is achieved. The power efficiency is increased by reducing the switching losses. The proposed converter has the advantages of reduced switch voltage stresses and a minimized circulating current when compared to the other converter topologies. The supercapacitor charging strategy has been also presented by using a constant current and constant voltage charging control. All of the control functions are implemented in software with a single-chip microcontroller. The performance of the proposed converter has been verified through experimental results using a 300 W prototype circuit for a 54-V, 35-F supercapacitor bank. The proposed converter improves power efficiency by 4 %, from 89 % to 93 % at the rated power.

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