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Parameter Optimization of the LC filters Based on Multiple Impact Factors for Cascaded H-bridge Dynamic Voltage Restorers

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Abstract

The cascaded H-Bridge Dynamic Voltage Restorer (DVR) is used for protecting high voltage and large capacity loads from voltage sags. The LC filter in the DVR is needed to eliminate switching ripples, which also provides an accurate tracking feature in a certain frequency range. Therefore, the parameter optimization of the LC filter is especially important. In this paper, the value range functions for the inductance and capacitance in LC filters are discussed. Then, parameter variations under different conditions of voltage sags and power factors are analyzed. In addition, an optimized design method is also proposed with the consideration of multiple impact factors. A detailed optimization procedure is presented, and its validity is demonstrated by simulation and experimental results. Both results show that the proposed method can improve the LC filter design for a cascaded H-Bridge DVR and enhance the performance of the whole system.

Key words: Dynamic Voltage Restorer, Multiple Impact Factors, Parameter Optimization, Value Range Function

I. INTRODUCTION

In recent decades, due to an increase in sensitive loads, economic loss events caused by voltage sags are a frequent occurrence. In order to minimize the adverse impact of voltage sags, the load side must be equipped with an appropriate compensation facility. A Dynamic Voltage Restorer (DVR) is connected between the grid and a sensitive load in series for suppressing voltage sags [1], [2]. When grid voltage sag occurs, the DVR resumes the load voltage to the rated value in a millisecond, thus ensuring the normal operation of the sensitive load. Many studies on DVRs have been carried out and a variety of topologies of the DVR have been discussed by scholars. In order to resolve the energy problem during compensation, some experts are committed to introducing energy storage devices to the structure of the DVR, such as chemical battery energy storage [3], superconducting energy storage [4] and flywheel energy storage [5]. Other experts have done research on topologies and control strategies utilizing low-voltage DVRs with a three-phase three-wire [6] or a three-phase four-wire [7]. High-voltage DVRs with the neutral-point clamped type [8], flying capacitor type [9] or cascaded type [10] have also been studied. Currently, the industrial application of DVRs is mainly in low-voltage. This is due to the extensive application of renewable energy, especially the grid integration of large-scale wind power and solar power. Power systems are becoming more and more complex, and the requirement for the low voltage ride through capability of wind farms and photovoltaic power plants has become more stringent. Because the DVR can effectively suppress voltage sags, the promotion and assembly of high voltage and large capacity DVRs is particularly urgent [11], [12]. Therefore, the study of high voltage and large capacity DVRs has become a new research focus [13], [14].

A reasonable LC filter design is the key to the development of a DVR. However, the design emphasis of LC filters for different DVR topologies is usually different. In [15] the characteristics of multi-level PWM waveform harmonics are summed up on basis of a large number of simulation datum.

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Then the design of the output filter is founded on a harmonic analysis, but it lacks a theoretical derivation. In [16] the high order harmonic contents and Total Harmonic Distribution (THD) values of two cascaded H-bridge inverters are accurately calculated. This provides a theoretical basis for the filter design. However, there is no further analysis on the filter parameters of the cascaded H-bridge topology. In [17] the LC parameters are designed by a transfer function analysis of the low-voltage DVR system based on the characteristic of the control strategy. This method guarantees that the LC filter can satisfy the system performance. However, it does not optimize the LC parameters to ensure the minimization of cost and volume. In [18] the LC filter parameters are designed for the two-level topology of a low-voltage DVR. However, the load harmonic current, the output power factor and the voltage sag depth are not taken into account during the design process. In the paper, the output LC filter parameter optimization of the H-bridge cascaded DVR is studied. In consideration of the load harmonic current, different output power factors and different voltage sag depths, a systematic analysis of the LC filter parameters' upper and lower limits is presented. The optimization of an LC filter based on multiple impact factors for a cascaded H-bridge dynamic voltage restorer is proposed. The theoretical derivation is discussed in detail, and the optimization method is validated by simulation and experimental results. The results show that the optimization method of the LC filter design is able to fully meet the system performance requirements, and reduce the cost and volume of the DVR system. It provides a reference for the design of the filter parameters in high voltage and large capacity power electronic equipment.

II. System Description of the Cascaded H-Bridge DVR

As shown in Fig.1, a cascaded H-bridge DVR is mainly comprised of a phase-shifting step-down transformer, power units and a LC filter. The system voltage u_e is connected to each power unit by the phase-shifting step-down transformer *TR*. In each power unit, the AC voltage is converted into DC voltage V_{dc} by the diode rectifier bridge which is composed of D1, D2, D3, D4, D5 and D6. After smoothing by the capacitor C, the DC voltage is used as the input of the H-bridge inverter which is made up of Q1, Q2, Q3 and Q4.

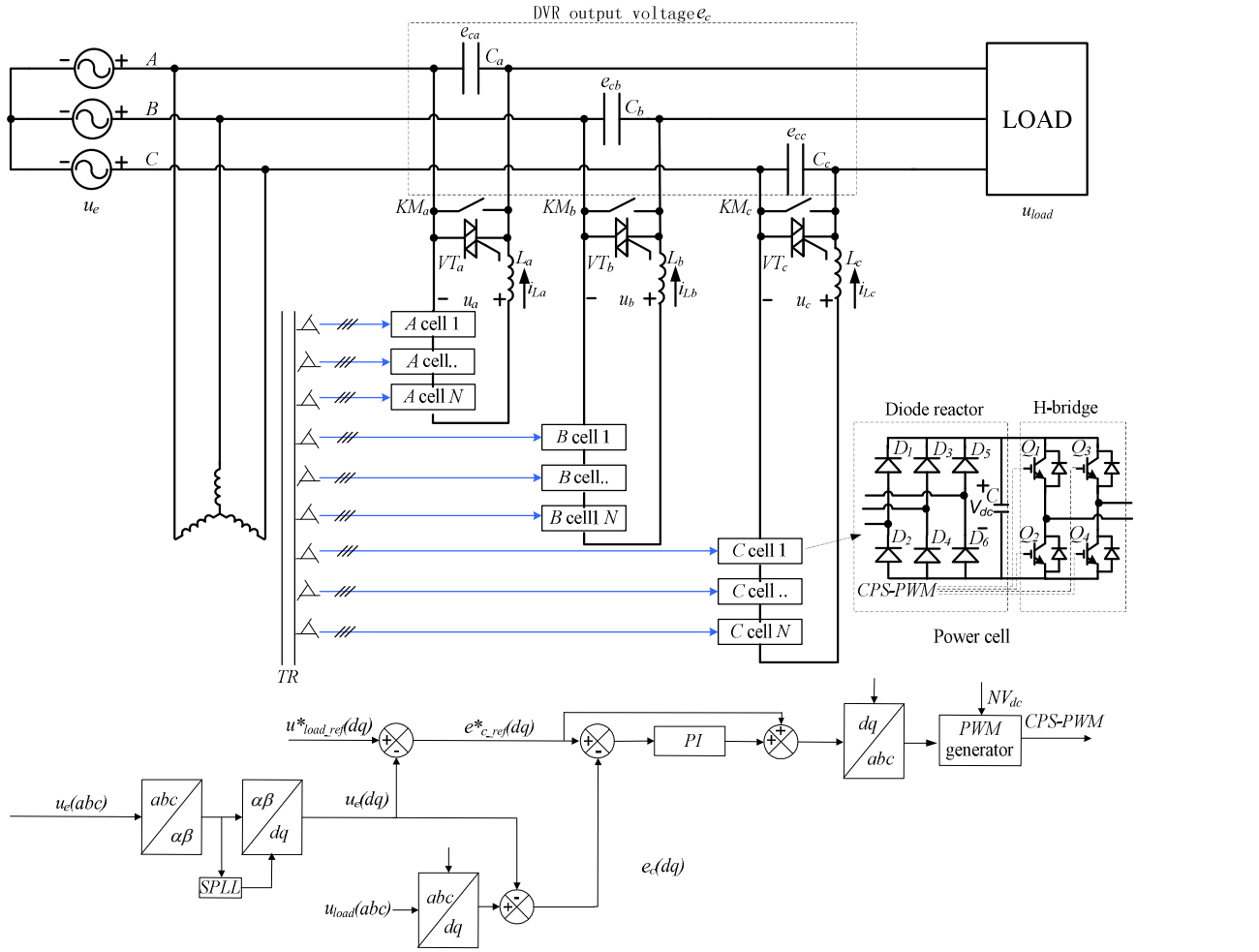

Fig. 1. System diagram of Cascaded H-bridge DVR

Take phase A for example, after filtering by the inductor L_a and the capacitor C_a, the output transient voltage u_a formed by N cascaded power units is turned into the instantaneous capacitor voltage e_{ca}. The capacitor C_a is connected in series between the grid and the load. Therefore, e_{ca} can be used to implement the dynamic voltage compensation. As shown in Fig.1, after the system voltage phase locking and voltage sag detection, the DVR control system generates a CPS-SPWM (Carrier Phase Shifting SPWM) signal to achieve control of the switching devices in each power unit by using a voltage feed-forward and feedback control.

An LC filter is the main part of a cascaded H-bridge DVR. It has a direct impact on the waveform quality of the output compensation voltage, the speed of the dynamic response and the performance of the control system. In addition, it affects the cost and volume of the DVR system. Because the DVR is series connected to the grid, the load characteristic determines the design requirements of the LC filter. In practical industrial situations, the load current contains large harmonic contents which lead to grid voltage distortion. Therefore, higher requirements for the LC filter are put forward.

There are multiple compensation strategies in the actual running of a DVR, such as the pre-sag compensation strategy, the in-phase compensation strategy and the minimum energy compensation strategy [19][20]. As a result, the output power factor of a DVR cannot be uniquely determined. Different output power factors will have different impacts on the LC filter design. Meanwhile, the DC voltage of each power unit V_{dc} is influenced by the voltage sag depth. Therefore, different V_{dc} values also influence the LC filter design. Therefore, an optimized design strategy for the LC filter needs to take full account of multiple impact factors such as load current harmonics, different output power factors and different voltage sag depths.

During the LC filter design, changes in the capacitance have a smaller impact on cost and size. In addition, inductance changes bring relatively large variations in cost and size. Therefore, the upper and lower limits of the inductance are a key aspect in design. Inductance design is necessary to achieve both fast current tracking and current ripple suppression. The inductor current mainly consists of load current. However, it also contains a certain amount of capacitor current. Since the capacitor current is much less than the load current, in the design, it can be approximated that the inductor current is equal to the load current.

Take phase A for example. Assume that the inductor current i_{La} is sinusoidal and that the DVR output power factor equals 1. When the inductor current is crossing zero, its change rate is at its largest. The inductance should be designed to be small enough to meet the requirements for the fast current tracking. Therefore, there is an upper limit to the inductance. When the inductor current reaches its peak, the current ripples are at its most serious. The inductance should be designed to be large enough to suppress the current ripples. Therefore, there is a lower limit to the inductance. By a transient analysis under the condition of multiple impact factors for these two moments, the upper limit L_{max} and the lower limit L_{min} of the inductance can be obtained. After determining the inductance range, the upper limit C_{max} and the lower limit C_{min} of the capacitance can be derived according to the LC filter requirements of the DVR. Finally, reasonable LC filter parameters can be determined.

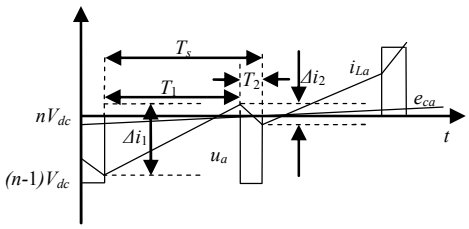

Fig. 2. The tracking wave of zero-crossing current under CPS-SPWM(partial enlarged view).

III. The Derivation of L_{max} Based on Multiple Impact Factors

Taking phase A for example, the transient state process of the zero-crossing current tracking wave is analyzed, as shown in Fig.2. When using CPS-SPWM, the output voltage presents a stepped waveform. The cascaded H-bridge output voltage u_a gradually increases by a step of each unit of DC voltage V_{dc}. In each step, u_a is switched between nV_{dc} and $(n\text{-}1)V_{dc}$. Meanwhile, n is an integer and the corresponding ceiling of the number for the instantaneous voltage e_{ca}. Assume that the output factor of the DVR is $\cos\varphi$. Then the voltage value at the zero-crossing current time is $e_{ca}=e_{cm}\sin\varphi$. As Fig.2 shows, T_1 is the high pulse time, and Δi_1 is the amplitude variation of the inductor current at time T_1. T_2 is the low pulse time, and Δi_2 is the amplitude variation of the inductor current at time T_2. L is the inductance, and i_{La} is the inductor current. Meanwhile, I_{Lm} is the peak value of the inductor current, and e_{cm} is the peak value of e_{ca}.

According to the steady-state formula, at the zero-crossing current, when $0<t<T_1$:

$$u_a - e_{ca} = nV_{dc} - e_{cm}\sin\varphi \approx L\frac{\Delta i_1}{T_1} \tag{1}$$

When $T_1<t<T_s$:

$$L\frac{\Delta i_2}{T_2} \approx (n-1)V_{dc} - e_{cm}\sin\varphi \tag{2}$$

In order to meet the requirements of the rapid current tracking:

$$\frac{|\Delta i_1| - |\Delta i_2|}{T_s} \geq \frac{I_{Lm}\sin\omega T_s}{T_s} \approx \omega I_{L\mathrm{m}} \tag{3}$$

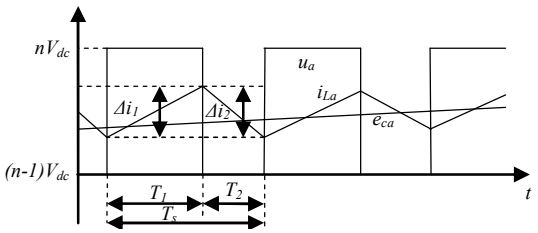

Fig. 3. The tracking wave of peak current under CPS-SPWM(partial enlarged view).

Where ω is the angular frequency of the inductor current i_{La}. From formula (1), (2) and (3):

$$L \le \frac{[nV_{dc} - e_{cm}\sin\varphi]T_1 - [e_{cm}\sin\varphi - (n-1)V_{dc}]T_2}{\omega I_{L\mathrm{m}} T_s} = \frac{nV_{dc}T_s - e_{cm}T_s\sin\varphi - V_{dc}T_2}{\omega I_{L\mathrm{m}} T_s} \quad (4)$$

When $T_2=0$, the current tracking response should be the fastest. At this time, the inductance is sufficiently small and satisfied the following formula:

$$L \le \frac{nV_{dc} - e_{cm}\sin\varphi}{\omega I_{L\mathrm{m}}} \quad (5)$$

L is determined by the value of nV_{dc}-$e_{cm}sin\varphi$, and n is an integer and the corresponding ceiling of the number for $e_{cm}sin\varphi$. Therefore, $e_{cm}sin\varphi$ is always between $(n\text{-}1)V_{dc}$ and nV_{dc}. Then V_{dc} is at its maximum. Therefore:

$$L \le \frac{V_{dc}}{\omega I_{Lm}} \quad (6)$$

In practical applications, considering the case where a nonlinear load current distortion occurs, the formula of the current should be:

$$i_{La} = \sum_{n=1}^{\infty} I_{Lmn}\sin n\omega_0 t \quad . \quad (7)$$

$\omega_0=2\pi f_0$ is the fundamental angular frequency. Assuming that the load current is constituted by the nth harmonic, in order to meet the tracking requirements of the nth harmonic change rate, the upper limit of the inductance should be:

$$L \le \frac{V_{dc}}{n\omega_0 I_{Lmn}} = L_{\max} \quad . \quad (8)$$

From the above analysis, it is clear that the upper limit of the inductance is unrelated to the voltage sag depth and the output power factor but is determined by the load harmonic current.

IV. The Derivation of L_{min} Based on Multiple Impact Factors

As shown in Fig.3, the transient state process of the peak current is analyzed. In order to facilitate the analysis and derivation, assume that the DVR output power factor is $cos\varphi$. Then the corresponding voltage instantaneous value at the peak current time is $e_{cm}cos\varphi$. Meanwhile, n is an integer and is determined by $e_{cm}cos\varphi$. u_e is the grid phase voltage rating. U_m is the reference peak value of u_e, and u_{1m} is the instantaneous peak value of u_e. Δu_m is the peak fluctuation of the grid phase voltage, which is the value of the DVR for compensation. Thus, $u_{1m}=U_m-\Delta u_m$. As a result, the voltage sag depth is $\Delta u_m/U_m$.

According to the steady-state formula at the peak current, when $0<t<T_1$:

$$u_a - e_{ca} = nV_{dc} - e_{cm}\cos\varphi \approx L\frac{\Delta i_1}{T_1} \quad (9)$$

When $T_1<t<T_s$:

$$u_a - e_{ca} = (n-1)V_{dc} - e_{cm}\cos\varphi \approx L\frac{\Delta i_2}{T_2} \quad (10)$$

When the current is on the top of the sine wave, $|\Delta i_1| = |\Delta i_2|$. Because of $T_1+T_2=T_s$:

$$T_1 = \frac{e_{cm}\cos\varphi - (n-1)V_{dc}}{V_{dc}}T_s \quad (11)$$

This can be solved from formula (9) and (10).And:

$$\Delta i_1 = \frac{(nV_{dc} - e_{cm}\cos\varphi)[e_{cm}\cos\varphi - (n-1)V_{dc}]}{LV_{dc}}T_s \quad (12)$$

$$L = \frac{(nV_{dc} - e_{cm}\cos\varphi)[e_{cm}\cos\varphi - (n-1)V_{dc}]}{|\Delta i_1|V_{dc}}T_s \quad (13)$$

Obviously, when using CPS-SPWM modulation, in order to reduce the current ripples effectively, $|\Delta i_1|$ should be the maximum pulsation of the current, which is $\Delta I_{max.}$. Formula (13) changes to:

$$L \ge \frac{(nV_{dc} - e_{cm}\cos\varphi)[e_{cm}\cos\varphi - (n-1)V_{dc}]}{\Delta I_{\max} V_{dc}}T_s \quad (14)$$

Set the phase shift step-down transformer turns ratio k, and the phase voltage utilization factor of the three-phase full-wave bridge rectifier k_1 so that the relationship between the DC voltage V_{dc} and u_{1m} is $V_{dc}=kk_1u_{1m}$. In the range of satisfying the compensation requirement, formula (14) changes to:

$$L \ge \frac{(nkk_1u_{1m} - e_{cm}\cos\varphi)[e_{cm}\cos\varphi - (n-1)kk_1u_{1m}]}{\Delta I_{\mathrm{m}ax}\, kk_1u_{1m}}T_s \quad (15)$$

Since $e_{cm}=\Delta u_m$, the expression $f(\Delta u_m,cos\varphi)$ of the relationship between the lower limit of the inductance, the output power factor and the voltage sag depth can be obtained.

$$f(\Delta u_m,\cos\varphi) = \frac{(nkk_1U_m - nkk_1\Delta u_m - \Delta u_m\cos\varphi)}{\Delta I_{\mathrm{m}ax}\, kk_1(U_m - \Delta u_m)} \times \frac{}{[\Delta u_m\cos\varphi - (n-1)kk_1U_m + (n-1)kk_1\Delta u_m]T_s} \quad (16)$$

Formula (16) is a bivariate distribution function. To analyze the relationship among $f(\Delta u_m,cos\varphi)$, Δu_m and $cos\varphi$, the derivation is presented below in detail.

Firstly, by solving $df(\Delta u_m,cos\varphi)/dcos\varphi=0$, the distribution

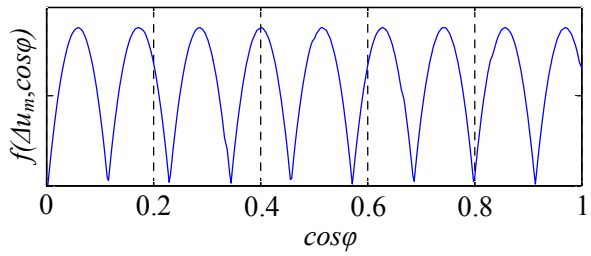

Fig. 4. Lower inductance limit versus output power factor.

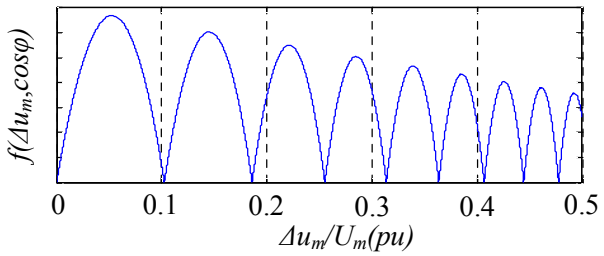

Fig. 5. Lower inductance limit versus voltage sag.

of the extreme point changes with the output power factor under the condition of a certain voltage sag depth can be obtained when:

$$\cos\varphi = \frac{(2n-1)kk_1(U_m - \Delta u_m)}{2\Delta u_m} \tag{17}$$

There are extreme points of $f(\Delta u_m,cos\varphi)$. The ceiling of the number n is determined mainly by the value of $\Delta u_m cos\varphi$. Therefore, there are n extreme points of formula (17).

For example, if the voltage sag depth is 0.5pu, when the output power factor changes from 0 to 1, there are plenty of extreme points.

When n=1, $\cos\varphi = \frac{kk_1(U_m - \Delta u_m)}{2\Delta u_m}$, an extreme point exists.

When n=2, $\cos\varphi = \frac{3kk_1(U_m - \Delta u_m)}{2\Delta u_m}$, an extreme point exists. Other extreme points are similar. It can been seen from Fig.4, that when the output power factor changes from 0 to 1, the extreme points of the lower limit present a regional distribution.

Secondly, by solving $df(\Delta u_m,cos\varphi)/d\Delta u_m$=0, the distribution of the extreme point changes with the voltage sag depth variation in the case of a certain output power factor can be obtained when:

$$\Delta u_m = \frac{nkk_1[\cos\varphi + (n-1)kk_1]}{2(nkk_1 + \cos\varphi)[(n-1)kk_1 + \cos\varphi]}U_m + \frac{(n-1)kk_1(nkk_1 + \cos\varphi)}{2(nkk_1 + \cos\varphi)[(n-1)kk_1 + \cos\varphi]}U_m \tag{18}$$

There are many extreme points. The ceiling of the number n is determined by $\Delta u_m cos\varphi$. Therefore, there are n extreme points in formula (18).

For example, if the output power factor is 1, when the voltage sag depth changes from 0pu to 0.5pu, plenty of extreme points exist.

When n=1, $\Delta u_m = \frac{kk_1}{2(kk_1+1)}U_m$, an extreme point exists.

When n=2, $\Delta u_m = \frac{kk_1}{(2kk_1+1)}U_m + \frac{kk_1}{2(kk_1+1)}U_m$, an extreme point exists, and so on.

As shown in Fig.5, when the sag depth changes from 0pu to 0.5pu, extreme points of the lower limit present a regional distribution.

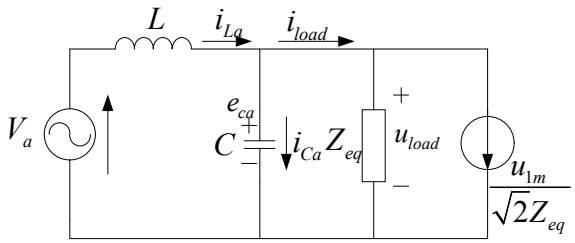

Fig. 6. The equivalent circuit of DVR.

To sum up, the lower limit of the inductance is determined by both the output power factor and the voltage sag depth. Therefore:

$$L_{\min} = \max[f(\Delta u_m, \cos\varphi)] \tag{19}$$

V. The Derivation of C_{min} and C_{max} Based on Multiple Impact Factors

After determining the range of the inductance, the capacitance can be designed. Firstly, due to the current limit of the power electronic switching device, the filter capacitor current cannot be too large, otherwise it will increase the cost of the design and lead to a rise in the power loss. Secondly, the major role of the capacitor C is to filter the voltage ripples in the CPS-SPWM and to smooth the DVR output voltage waveform for reducing the distortion. This also guarantees that the LC filter bandwidth can meet the requirements of the output voltage tracking feature. When considering the design of the capacitance, there are two important points:

1. The capacitor current needs to be far less than the load current.

2. The natural frequency of the LC filter should satisfy the condition of $10f_n<f_r<0.5f_{psw}$. f_n is the maximum pass-band frequency of the system, f_{psw} is the system equivalent switching frequency, and f_s is the LC filter natural frequency.

Firstly, according to Fig.1, the DVR equivalent diagram in Fig.6 is derived. i_{load} is the load current, and Z_{eq} is the equivalent impedance per phase. Meanwhile, i_{Ca} is the capacitor current, and Z_{Cf} is the capacitive reactance.

$$Z_{eq} = \frac{U_e^2}{S} \tag{20}$$

$$i_{La} = i_{Ca} + i_{Load} \tag{21}$$

To meet the requirements of point 1, i_C should be far less than i_{load}, according to [18]. Therefore:

$$\frac{1}{100}\frac{u_{load}}{Z_{eq}} \le i_{Ca} = \frac{e_{ca}}{Z_{Cf}} \le \frac{1}{10}\frac{u_{load}}{Z_{eq}} \tag{22}$$

After the voltage compensation of the DVR, the load voltage recovers to the rated level. Therefore, $u_{load}=U_m$, $e_{ca}=\Delta u_m$. At this time:

$$\frac{1}{100}\frac{U_m}{\Delta u_m \omega_0 Z_{eq}} \le C \le \frac{1}{10}\frac{U_m}{\Delta u_m \omega_0 Z_{eq}} \tag{23}$$

It can be seen from formula (23) that the capacitance design should be inversely proportional to the voltage sag depth. As Δu_m becomes larger, the upper and lower limits of the capacitance become smaller. The capacitance should be designed according to the maximum voltage sag depth.

At the same time, in order to meet the requirements of point 2, the LC filter natural frequency should be:

$$10 f_n \le f_r = \frac{1}{2\pi\sqrt{LC}} \le 0.5 f_{psw} \tag{24}$$

$$\frac{4}{L(2\pi f_{psw})^2} \le C \le \frac{0.01}{L(2\pi f_n)^2} \tag{25}$$

For reducing the cost and volume of the whole DVR system, the inductance should be as smaller as possible under the premise of meeting the performance requirement. The inductance in formula (25) is usually selected as the lower limit L_{min}. Set C_{min} and C_{max} as the minimum and maximum capacitances. The range of the capacitances should be:

$$C_{\min} \le C \le C_{\max} \tag{26}$$

$$C_{\min} = \max\left\{\frac{0.01U_m}{\Delta u_m \omega_0 Z_{eq}}, \quad \frac{4}{(2\pi f_{psw})^2 L_{\min}}\right\},$$

$$C_{\max} = \min\left\{\frac{0.1U_m}{\Delta u_m \omega_0 Z_{eq}}, \quad \frac{0.01}{(2\pi f_n)^2 L_{\min}}\right\}。$$

VI. The Design Optimization and Simulation Analysis

According to the system parameters in Table 1, since i_C is far less than i_{load}, i_{La} is equal to i_{load}. Taking these parameters to the formula (8), the upper limit value of the inductance is:

$$L_{\max} \le 1.2989\text{mH} \tag{27}$$

Through the description in chapter 4, on the condition of different output power factors and voltage sag depths, the lower inductance limit has a different extreme value distribution, and it is hard to determine the maximum extreme value. Therefore, a further analysis of the three-dimensional coordinate is needed. According to system parameters and the simulation results, the relationship between the voltage sag depth, the output power factor and the lower inductance limit is an extreme value surface, as shown in Fig.7.

With the voltage sag depth changing, the relationship between the output power factor and the lower inductance

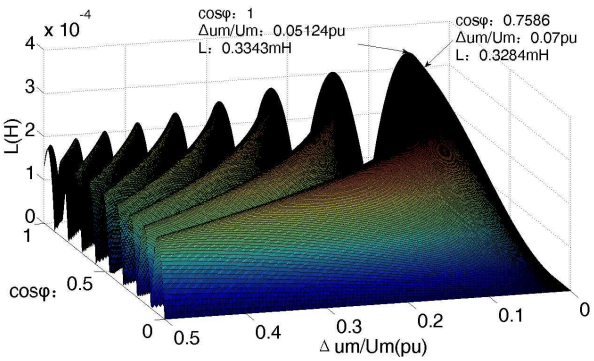

Fig. 7. Distribution curves of inductance versus double impact factors.

TABLE I

System Parameters

Rated voltage (U_e)	10kV	Rated current (I_e)	115.5A
Load power(S)	2 MVA	Turns ratio (k)	10000/690
Maximum cascaded number（n_{max})	9	Modulation mode	CPS-SPWM
Voltage sag depth ($\Delta u_m/u_m$)	0.07pu-0.5pu	Maximum current ripples(ΔI_{max})	23A
Equivalent switching frequency (f_{psw})	20kHz	Maximum pass-band frequency (f_0)	350Hz

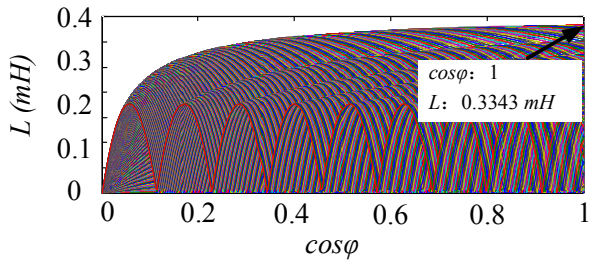

Fig. 8. Multi-curves of output power factor and inductance.

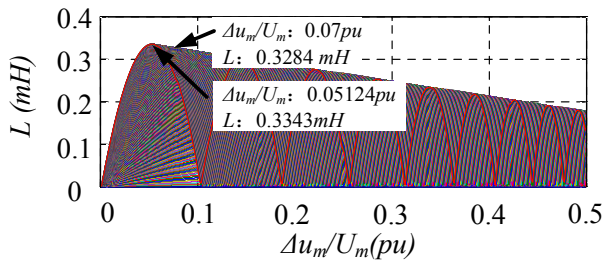

Fig. 9. Multi-curves of voltage sag and inductance

limit is shown in Fig. 8. The extreme value distribution is monotonically growing.

With the output power factor changing, the relationship between the voltage sag depth and the lower inductance limit is shown in Fig.9. The extreme value distribution is a parabola and has a peak point.

According to the extreme value surface shown in Fig.7, the distribution of the inductance has nine extremal curves. According to the relationship of Fig.8, the higher the output power factor, the larger the corresponding lower inductance limit value. Based on the analysis from Chapter 4, when the output power factor is 1, there is a maximum value for the inductance. Taking the system parameters into formula (18), when Δu_m=0.05124u_m, it has the maximum value of the function $f(\Delta u_m,cos\varphi)$:

$$f(\Delta u_m,\cos\varphi)|_{\Delta u_m=0.05124u_m,\cos\varphi=1}=0.3343mH \quad (28)$$

Therefore, the maximum value of the lower inductance limit is 0.3343mH.

According to the system design requirements, a voltage deviation among ±0.07pu of the normal voltage is allowed. Therefore, the 10kV H-bridge cascaded DVR does not need compensation when the voltage sag depth is in this range. Because the corresponding voltage sag depth of the maximum point is 0.05124pu, which is less than 0.07pu and not in the DVR design requirement, the lower inductance limit can be further optimized.

According to Fig.9, the relationship curve presents a monotonously rising trend within the range of the abscissa (0, 0.05124pu), and within the range of the abscissa (0.05124pu, 0.5pu) it is a monotonic downdard trend. Therefore, within the scope of the grid voltage sag depth 0.07pu-0.5pu, when Δu_m=0.07u_m, there is a maximum of $f(\Delta u_m,cos\varphi)$. According to formula (17), an extreme point exists when $cos\varphi$=0.7586. At this moment:

$$f(\Delta u_m,\cos\varphi)|_{\Delta u_m=0.07u_m,\cos\varphi=0.7586}=0.3284mH \quad (29)$$

In summary, within the scope of the grid voltage sag depth 0.07pu-0.5pu:

$$L_{\min}=\max[f(\Delta u_m,\cos\varphi)|_{\Delta u_m\in(0.07u_m\sim0.5u_m),\cos\varphi\in(0,1)}]=0.3284mH \quad (30)$$

According to formulas (27) and (30), the range of the inductance upper and lower limits can be obtained:

$$0.3284mH\le L\le1.2989mH \quad (31)$$

According to formulas (23) and (25), the capacitance range is:

$$1.27uF\le C\le6.3uF \quad (32)$$

The LC filter natural frequency distribution surface can be obtained according to the range of the upper and lower limit of the inductance and capacitance which are shown in Fig.10. Because the value of the inductance has a direct relationship on the cost and volume of the system, the inductance should be as small as possible under the condition of satisfying the

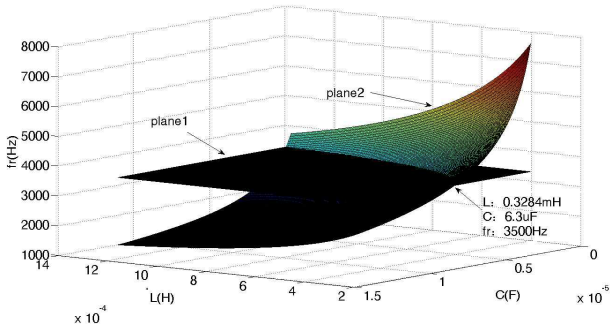

Fig. 10. Planes of cut-off frequency, inductance and capacitance.

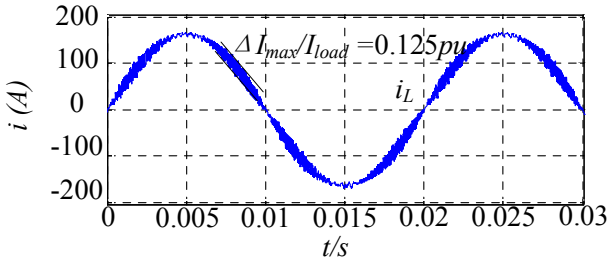

Fig. 11. The inductor current under the condition of output power factor 1.

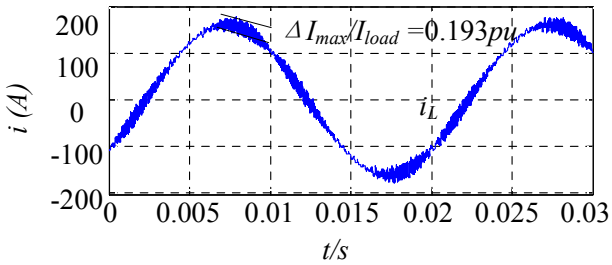

Fig. 12. The inductor current under the condition of output power factor 0.75.

DVR output performance.

It is shown in Fig.10 that plane 1 is a 3500Hz natural frequency plane, and plane 2 is a natural frequency plane with different LC parameters. The point at the intersection of the two planes is the LC parameters satisfying the system requirements. On the premise of minimizing the inductance, the optimized parameters of the LC filter are:

$$L=0.3284mH,C=6.3uF,f_{res}=3500Hz \quad (33)$$

According to the calculated inductance and capacitance, a 10kV medium voltage grid H-bridge cascaded DVR simulation model is built and the optimized design of the LC filter is validated in Matlab/Simulink.

Fig.11 shows that the inductor current waveform under the output power factor equals 1 when the voltage sag depth is 0.1pu. Fig.12 is the inductor current waveform when the output power factor equals 0.75 and the voltage sag depth equals 0.1pu. It can be seen from the comparison that the maximum current ripples in Fig.11 are smaller than those in Fig.12. Thus, under the condition of different output power factors, the maximum values of the inductor current ripples

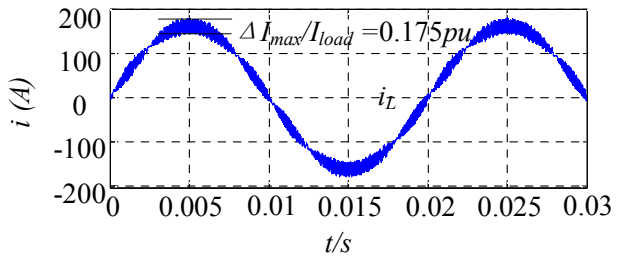

Fig. 13. The inductor current under the condition of voltage sag 0.15pu.

will be different, and a variation in the output power factor directly affects the design of the inductance.

Fig.13 is the inductor current waveform when the output power factor equals 1 and the voltage sag depth equals 0.15pu. It can be seen from a comparison with Fig.11 that the maximum current ripples under the voltage sag equals 0.1pu, which is smaller than the one in Fig.13 where the voltage sag equals 0.15pu. Thus, different voltage sag depths cause different inductor current ripple maximum values, and the variation in the voltage sag depth directly affects the design of the inductance.

VII. Experimental Results

According to the theoretical derivation and the simulation, a 10kV/2MW DVR prototype has been built as shown Fig. 14. A dual-DSP-TMS320F28335 is used as an algorithm processor. The CPS-SPWM is realized by an EP3C25-EQFP144 of Altera. The H-bridge consists of a FF300R17ME3 of Infineon. All of the tests have been carried out on the platform with the voltage sag composed by different inductors, as shown in Fig. 15. Fig. 16 shows the experimental result under the condition of 0.4pu voltage sag. Fig. 17 shows that the inductor current under the voltage sag equals 0.1pu and the output power factor equals 1. Fig. 18 shows that the inductor current under the output power factor equals 0.75 and the voltage sag depth equals 0.1pu. Fig. 19 is the inductor current when the output power factor equals 1 and the voltage sag depth equals 0.15pu. It can be seen that when the voltage sag depth is 0.1pu, the maximum current ripples in Fig. 17 are a little smaller than those in Fig. 18. When the output power factor is 1, the maximum current ripples in Fig. 17 are a little smaller than that in Fig. 19.

By analyzing and comparing the inductor current waveforms under different output power factors and different voltage sag depths, it can be seen that the optimized design method of the LC filter based on the load current harmonic, the output power factor and the voltage sag depth is able to satisfy the system performance. Meanwhile, due to the inductance optimization, the cost and volume of a DVR system can be effectively reduced. The optimized design is correct and effective, and it provides a theoretical guide for engineering design.

Fig. 14. The 10kV DVR principle prototype.

Fig. 15. Voltage sag generation system.

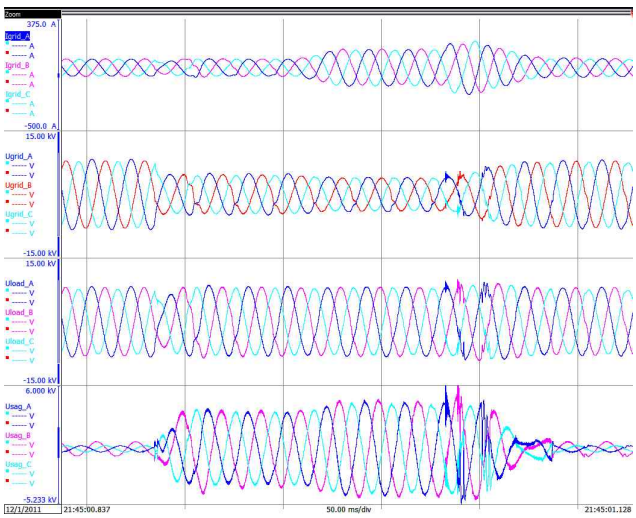

Fig. 16. Waveform under the condition of voltage sag 0.4pu（up to down: Grid current, Grid voltage, Load voltage, DVR voltage.

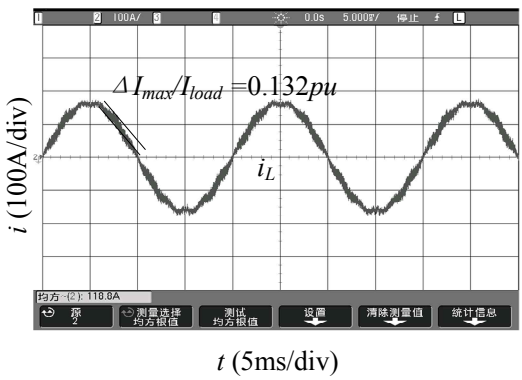

Fig. 17. The inductor current under the condition of output power factor 1.

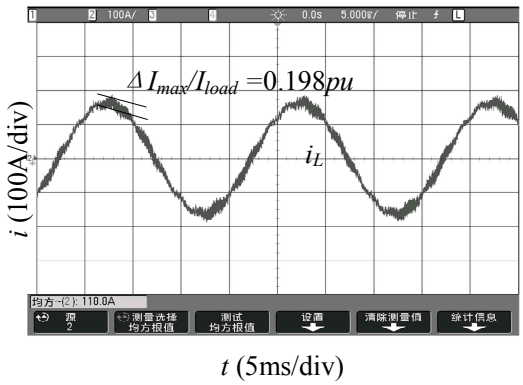

Fig. 18. The inductor current under the condition of output power factor 0.75.

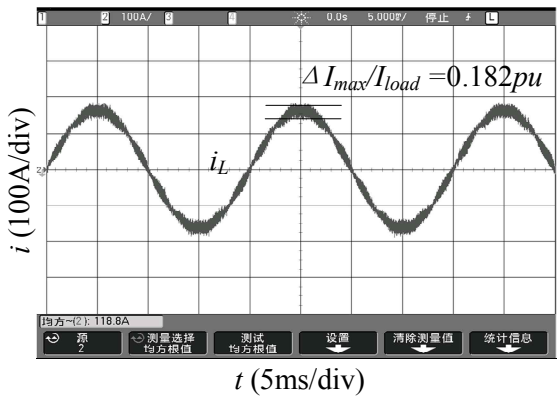

Fig. 19. The inductor current under the condition of voltage sag 0.15pu.

VIII. CONCLUSION

The paper presents an optimized design for the LC filter used in the H-bridge cascaded DVR topology based on multiple impact factors. By building and analyzing the upper and lower limit functions of the inductance and capacitance, it can be obtained that the load harmonic current affects the inductance upper limit design, while the output power factor and the voltage sag depth affect the lower inductance limit design. At the same time the upper and lower limit of the inductance also determines the range of the capacitance. Finally, LC filter parameters based on the multiple impact factors are worked out. The simulation and experimental results show that the filter parameters using the optimized design fully meet the system performance requirements. In addition, the cost and volume of the DVR system are minimized. The optimized design provides a reference for the filter design of high voltage and large capacity power electronic equipment, and has a tremendous engineering application prospect.

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REFERENCES

[1] J. C. Gomez and M. M. Morcos, “Voltage sag and recovery time in repetitive events,” *IEEE Trans. Power Del.*, Vol. 17, No. 4, pp. 1037-1043, Oct. 2002.

[2] S. Subramanian and M. K. Mishra, “Interphase AC-AC topology for voltage sag supporter,” *IEEE Trans. Power Electron.*, Vol. 25, No. 2, pp. 514-518, Feb. 2010.

[3] I. Papic, “300 kW battery energy storage system using an IGBT converter,” *IEEE Power Engineering Society Summer Meeting*, Vol. 2, pp.1214-1218, 1999.

[4] J. Shi, “SMES based dynamic voltage restorer for voltage fluctuations compensation,” *IEEE Trans. Appl. Supercon.*, Vol. 20, No. 3, pp. 1360-1364, Jun. 2010.

[5] B. Wang and G. Venkataramanan, “Dynamic voltage restorer utilizing a matrix converter and flywheel energy storage,” *IEEE Trans. Ind. Appl.*, Vol.45, No.1, pp.222-231, Jan./Feb. 2009.

[6] J. G. Nielsen and F. Blaabjerg, “A detailed comparison of system topologies for dynamic voltage restorers,” *IEEE Trans. on Ind. Appl.*, Vol. 41, No.5, pp. 1272-1280, Sep./Oct. 2005

[7] D. A. Fernandes, S. R. Naidu, A. M. N. Lima, “Closed-loop control of a dynamic voltage restorer based on a 4-leg voltage source converter,” *IEEE Int. Symposium on Ind. Electron.*, pp. 80-85, 2008.

[8] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaén, M. Corbalán, “Voltage-balance compensator for a carrier-based modulation in the neutral-point-clamped converter,” *IEEE Trans. Ind. Electron.*, Vol. 56 , No. 2, pp.305-314, Feb. 2009.

[9] P. Roncero-S´anchez and E. Acha, “Dynamic voltage restorer based on flying capacitor multilevel converters operated by repetitive control,” *IEEE Trans. on Power Del.*, Vol. 24, No. 2, pp.951-960, Apr. 2009.

[10] B. Wang and M. Illindala, “Operation and control of a dynamic voltage restorer using transformer coupled H-bridge converters,” *IEEE Trans. Power Electron.*, Vol. 21, No. 4, pp1053-1061, Jul. 2006.

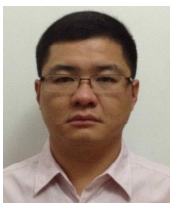
[11] M. Farsadi, A. G. shahrak, F. S. Oskouyi, “Photovoltaic based DVR for improving the operation of wind farm,” *7th Int. Con. on Electrical and Electron. Engineering (ELECO)*, Vol. 1, pp. 298-301, 2011.

[12] C. Wessels, F. Gebhardt, F. W. Fuchs, “Fault ride-through of a dfig wind turbine using a dynamic voltage restorer during symmetrical and asymmetrical grid faults,” *IEEE Trans. on Power Electron.*, Vol. 26, No. 3, pp. 807-815, Mar. 2011.

[13] C. Meyer, R. W. De Doncker, Y. W. Li, and F. Blaabjerg, “Optimized control strategy for a medium-voltage DVR—Theoretical investigations and experimental results,” *IEEE Trans. Power Electron.*, Vol. 23, No. 6, pp. 2746-2754, Nov. 2008.

[14] D. Li, P. C. Loh, M. Zhu, F. Gao, and F. Blaabjerg, “Cascaded multicell trans-z-source inverters,” *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp.826-836, Feb. 2013.

[15] W. Yi, L. Heming, and S. Xinchun, "Harmonic analysis and output filter design for multilevel PWM inverter," *Proceedings of the CSEE*, Vol. 23, No. 10, pp. 78-82, 2003.
[16] L. Chunxi, M. Weiming, and S. Chi, "Design of output lc filter and low order harmonics suppression in high power 400Hz inverter," *Trans. of China Electro. Society*, Vol. 26, No. 6, pp.129-136, 2011.
[17] H. Kim, J.-H. Kim, S.-K. Sul, "A design consideration of output filters for dynamic voltage restorers," *IEEE 35th Annu. Power Electron. Specialists Con.*, Vol.6, pp.4268-4272, 2004.
[18] S. Guo and D. Liu, "Analysis and Design of Output LC Filter System for Dynamic Voltage Restorer," *Twenty-Sixth Ann. IEEE Applied Power Electron. Con. and Expo. (APEC)*, pp.1599-1605, 2011.
[19] S. Wang, K. Yu, and G. Tang, "Performance analysis and improvement of digital vector control algorithm for dynamic voltage restorer," *Proceedings of the CSEE*, Vol. 28, No. 7, pp. 64-71, 2008.
[20] Z. Yin, L. Zhou, and K. Yu, "System design and simulation of 2MVA cascaded multilevel dynamic voltage restorer without series transformer," *Power system technology*, Vol. 30, No. 1, pp.80-84, 2006.



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