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A Driving Scheme Using a Single Control Signal for a ZVT Voltage Driven Synchronous Buck Converter

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Abstract

This paper deals with the optimization of the driving techniques for the ZVT synchronous buck converter proposed in [1]. Two new gate drive circuits are proposed to allow this converter to operate by only one control signal as a 12V voltage regulator module (VRM). Voltage-driven method is applied for the synchronous rectifier. In addition, the control signal drives the main and auxiliary switches by one driving circuit. Both of the circuits are supplied by the input voltage. As a result, no supply voltage is required. This approach decreases both the complexity and cost in converter hardware implementation and is suitable for practical applications. In addition, the proposed SR driving scheme can also be used for many high frequency resonant converters and some high frequency discontinuous current mode PWM circuits. The ZVT synchronous buck converter with new gate drive circuits is analyzed and the presented experimental results confirm the theoretical analysis.

Key words: Synchronous buck converter, Voltage-driven synchronous rectifier (VDSR), Voltage regulator module (VRM), Zero-voltage switching (ZVS)

I. INTRODUCTION

Due to the improvements in semiconductor technology, more transistors are being placed on integrated circuits (ICs). To decrease the power consumption of an IC, its operating voltage must be reduced. The voltages of today ICs are 5, 3.3, and 1.2 V or lower. On the other hand, increasing the bus voltage reduces the conduction losses. For this reason, the bus voltage has been changed from 5 V to 12 V in several applications such as portable equipment, telecommunication equipment, data processing units, etc. Therefore, efficiently converting the 12 V input to the IC voltages by high quality voltage regulator modules (VRMs) is very challenging.

A synchronous buck converter is usually the first choice for such a VRM. In this topology, the synchronous rectifier (SR) decreases the conduction losses of the main diode. However, the reverse recovery time of the SR body diode considerably increases both the switching losses and the electro-magnetic interference (EMI). By applying zero-voltage transition (ZVT) techniques to a synchronous buck converter, a time gap would be created between the conduction time of the main switch and the diode. Thus, the losses related to the reverse recovery time of the SR body diode are significantly reduced [1]. In addition, like other Soft switching methods, ZVT techniques decrease the switching losses and EMI. Among the many ZVT techniques, the studies in [1]-[6] have applied the ZVT and synchronous rectification techniques simultaneously. The ZVT synchronous buck converter proposed in [1] is shown in Fig. 1(a). In this technique, the zero-voltage switching (ZVS) condition is provided for the main and SR switches without any additional current or voltage stress. In addition, it provides the zero-current-switching (ZCS) condition for the auxiliary switch. Another distinctive advantage of this technique is that when the auxiliary switch current reaches the output inductor current, the SR does not turn off and remains on for a short interval. Therefore, the direction of the SR current is reversed and additional energy is stored in the auxiliary inductor. This additional energy can completely discharge the snubber capacitor even if the output voltage is less than $V_{in}/2$. In addition, this would eliminate the reverse recovery loss of the SR body diode. These advantages are created by a simple auxiliary circuit. However, this converter needs a complicated circuit to generate 3 isolated gate pulses for the main switch, the auxiliary switch and the SR. This complicated circuit can decrease reliability and increase the converter cost. Therefore, the driving scheme for the switches is a technical challenge of this new approach. Ref. [1] applies the external driven method

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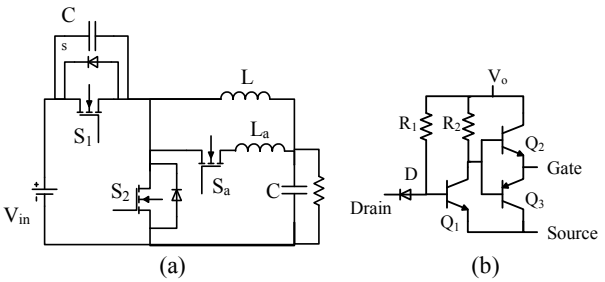

Fig. 1. (a) ZVT synchronous buck converter proposed in [1], (b) SR driving circuit proposed in [26](V_o is the converter output voltage).

to drive the SR. Besides this method, there are two other methods to control the synchronous rectifiers namely self-driven and control-driven methods. In the external-driven method, which is shown in Fig. 2(a), a control unit utilizes the switching signal to generate the SR driving signal. Thus, a more complicated circuit is required. In addition, in many applications, the SR driving signal needs to be isolated. Therefore, a transformer-isolated or an opt-isolated gate driver is required. As a result, this technique may adversely affect reliability while the system implementation is more complicated and costly.

The self-driven method, which is shown in Fig. 2(b), utilizes the voltage across the output inductor or the secondary side of the transformer to drive the SR [7]-[14]. This converter is non-isolated and does not have a transformer. In addition, when the SR is on, the voltage on the output inductor is clamped to V_O and cannot be utilized to turn off the SR. Thus, the implementation of a self-driven technique for this converter is very difficult.

The control-driven method develops the driving signal by monitoring the SR current [15]-[27]. This technique can be applied to this type of converter since the SR current is reversed before the SR is turned off. The control-driven method is divided into current-driven and voltage-driven methods. In the current-driven method, which is shown in Fig. 2(c), the current transformer (CT) is placed in series with the MOSFET to sense the SR current [15]-[24]. However, the CT has a large size and its winding adds resistance to the current path. Therefore, the current driven-method sacrifices power density and efficiency especially in low-voltage high-current applications.

The voltage-driven method, which is shown in Fig. 2(d), monitors the voltage developed across the SR drain-source and generates the driving signal according to the detected polarity [25]-[27]. This voltage is the result of the SR current flowing through its on resistance. In [26], a new circuit based on the voltage-driven method is proposed for a flyback converter as illustrated in Fig. 1(b).

This circuit detects the SR voltage polarity by a series combination of the diode and BJT base-emitter junction that

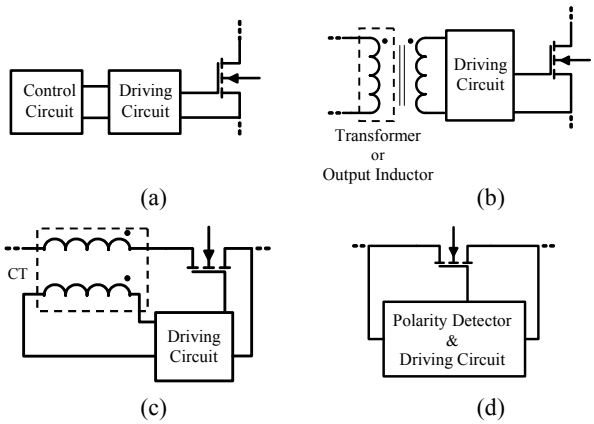

Fig. 2. Methods to control the synchronous rectifier. (a) External-driven method, (b) self-driven method, (c) current-driven method, (d) voltage-driven method.

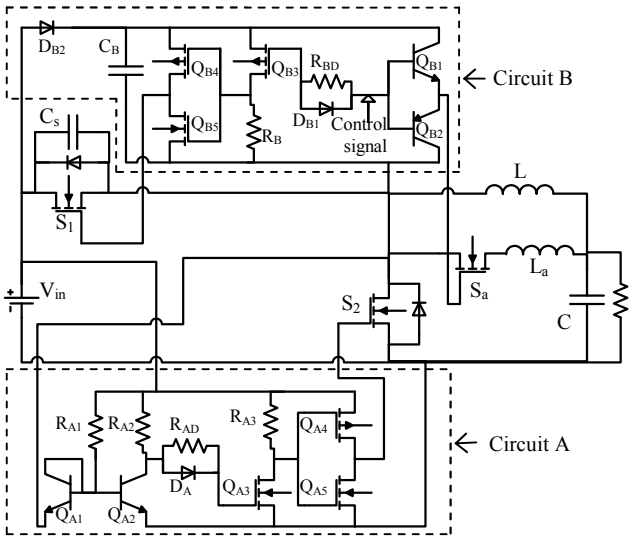

Fig. 3. ZVT synchronous buck converter with proposed driving circuits.

are placed across the SR drain-source terminals. Then, the generated signal is applied to the SR gate through a push-pull buffer. However, this circuit switches the SR as soon as the drain-source voltage polarity changes. In addition, the polarity of a voltage with such a low magnitude may not be detected.

As it can be observed from Fig. 1(a), the main and auxiliary switches of the Ref. [1] converter have a common source. Therefore, this paper proposes a driving circuit for these switches by using only one signal. In addition, this paper presents a new, improved voltage-driven synchronous rectification scheme for this converter. In addition, no extra DC voltage source is required to provide the supply voltage for the gate drivers. This is due to the fact that for low input voltage applications, especially 12V VRM applications, the variations of the input voltage are limited and thus, the input voltage can be used to supply the gate drive circuits. By incorporating these drivers, the converter driving scheme is

improved without any change in its main operational intervals or capabilities. Therefore, the converter driving complexity is reduced and the reliability is improved while the previously mentioned advantages of the converter in [1] are maintained. On the other hand, in the proposed synchronous rectification scheme, the SR can remain on when the drain-source voltage polarity changes. Consequently, it is very suitable for converters where the SR must not turn off as soon as its voltage polarity becomes positive, like some ZVT synchronous buck converters, some high-frequency resonant converters and some high-frequency discontinuous current mode PWM circuits.

This paper is composed of six sections. After this introduction, the ZVT synchronous buck converter with the proposed gate drive circuits is presented and analyzed in section II. Section III focuses on the design considerations. Other applications of the proposed voltage-driven synchronous rectifier are provided in section IV. In section V, experimental results from the implemented prototype are provided to confirm the validity of the theoretical analysis. Finally, some conclusions are presented in section VI.

II. CIRCUIT DESCRIPTION AND PRINCIPLE OF OPERATION

The ZVT synchronous buck converter together with its gate drive circuits is shown in Fig. 3. Circuit A which is based on the voltage-driven method, drives the SR. The main and auxiliary switches are driven by circuit B. The rest of the circuit is the converter which is composed of the main switch S_1, the SR switch S_2, and the output filter L & C. The snubber capacitor C_s, the unidirectional auxiliary switch S_a and the auxiliary inductor L_a are the auxiliary components to provide the ZVS condition. In circuit A, transistors Q_{A1} & Q_{A2} detect the SR voltage polarity. These transistors with resistors R_{A1} & R_{A2} generate proper signals with respect to the SR voltage polarity. Resistor R_{AD} provides the turn off signal to the SR with delay. Diode D_A bypasses R_{AD} when the turn on signal is generated. Finally, transistors Q_{A3}, Q_{A4}, and Q_{A5} along with resistor R_{A3} operate as a buffer to amplify and sharpen the edge of the gate signals. The reference voltage for this circuit is the input voltage. In circuit B, transistors Q_{B1} & Q_{B2} operate as a push–pull topology to drive the auxiliary switch. In addition, transistors Q_{B3}, Q_{B4}, and Q_{B5} along with resistor R_B operate as a buffer to drive the main switch. Resistor R_{BD} provides the main switch turn on with delay. Diode D_{B1} circumvents R_{BD} when the control signal becomes low. Finally, diode D_{B2} and capacitor C_B form the required bootstrap to make the supply voltage. Operation block diagrams of the proposed driving circuits are illustrated in Fig. 4. To simplify the converter analysis, the following assumptions are made: 1) all semiconductor devices are ideal; 2) the input voltage is constant and equal to V_{in} in a switching cycle; and 3) the inductor L current and capacitor C voltage are constant and equal to I_o & V_o, respectively. Fig. 5 and Fig. 6 illustrate the essential theoretical waveforms. Fig. 7 presents the equivalent circuit of each operating interval. The circuit operation is explained as follows.

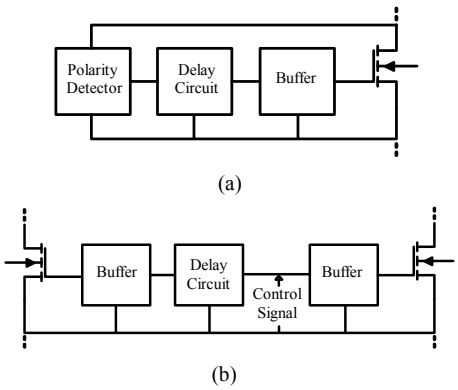

Fig. 4. Operation block diagrams. (a) circuit A, (b) circuit B.

Before the first interval [Before t_0]: It is assumed that the SR is on and all of the other semiconductor devices in the main circuit are off. In circuit A, transistors Q_{A1}, Q_{A3}, and Q_{A4} are on, while Q_{A2} and Q_{A5} are off. In addition, in circuit B, transistors Q_{B2}, Q_{B3}, and Q_{B5} are on, while Q_{B1} and Q_{B4} are off.

Interval 1 [$t_0 - t_1$]: This interval starts when the control signal becomes high and it turns on Q_{B1} and turns off Q_{B2}. Transistor Q_{B1} delivers current to the gate-source capacitor of S_a, and turns this switch on at t_0. At the same time, the gate-source capacitor of Q_{B3} begins to discharge through R_{BD} and thus, Q_{B3} turns off with a delay. When S_a turns on, the output voltage is placed across L_a. Accordingly, the L_a current increases from zero to I_o and the S_2 current decreases from I_o to zero linearly. Due to L_a, S_a is turned on under zero-current switching.

Interval 2 [$t_1 - t_2$]: At the beginning of this interval, the L_a current becomes more than I_o. Thus, the S_2 current is reversed and the drain-source voltage of S_2 becomes positive. In this condition, the base-emitter voltage of Q_{A2} is higher than Q_{A1}, and Q_{A2} is turned on by the current flowing through resistor R_{A1}. As a result, the input capacitor of Q_{A3} begins to discharge through R_{AD} and Q_{A2}. By proper design of R_{AD} (as discussed in the next section), Q_{A3} is turned off at the end of this interval. Therefore, S_2 is on and like the previous interval, the L_a current linearly increases from I_o. The maximum value of the L_a current at the end of this interval is defined as I_1. In this interval, additional energy is stored in L_a to make sure it would discharge the snubber capacitor.

Interval 3 [$t_2 - t_3$]: This interval starts by turning Q_{A3} off at t_2. The input capacitor of Q_{A4} is discharged through R_{A3}, and Q_{A4} is turned off. At the same time, the supply voltage charges the input capacitor of Q_{A5} through R_{A3} and turns on this

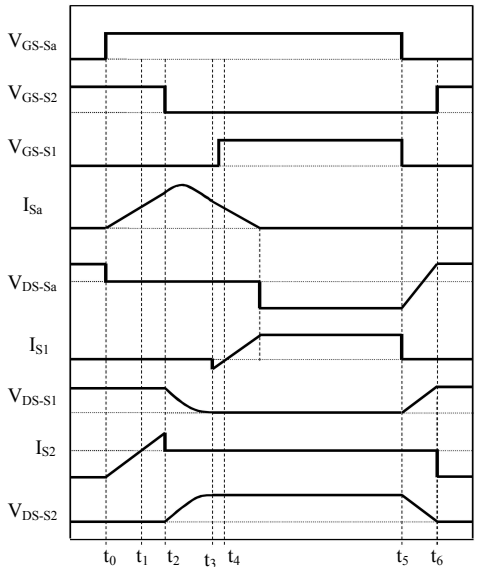

Fig. 5. Theoretical waveforms of the synchronous buck converter.

transistor. Finally, the input capacitor of the SR switch (S_2) is discharged trough Q_{A5}, and S_2 is turned off. By turning S_2 off, a resonance begins between L_a and C_s. By proper design of L_a, C_s and R_{AD} as discussed in the next section, C_s is completely discharged and the L_a current is slightly greater than I_o at the end of this interval. Due to C_s, S_2 is turned off under zero-voltage switching (ZVS).

Interval 4 [t_3 – t_4]: The body diode of S_1 turns on at t_3 and the voltage of C_s remains zero. The voltage difference between the input and output voltages is placed across L_a and its current decreases linearly to I_o. By proper design of R_{BD}, transistor Q_{B3} is turned off in this interval. Then, the input capacitor of Q_{B5} is discharged through R_B, and Q_{B5} is turned off. At the same time, the input capacitor of Q_{B4} is charged by the supply voltage through R_B, and Q_{B4} is turned on. Finally, the supply voltage charges the input capacitor of the main switch S_1 through Q_{B4}, and turns on this transistor. S_1 is turned on under ZVS because the L_a current is greater than I_o and thus, the body diode of S_1 is on during this interval.

Interval 5 [t_4 – t_5]: In this interval, the main switch S_1 is on. As a result, the L_a current continues to decrease from I_o to zero. Then, the unidirectional auxiliary switch S_a does not allow the L_a current to become negative, and it stops conduction. Thus, the converter behaves like a regular buck converter.

Interval 6 [t_5 – t_6]: This interval starts when the control signal becomes low. This signal turns off Q_{B1} and turns on Q_{B2}. Transistor Q_{B2} discharges the input capacitor of the auxiliary switch S_a, and turns off this switch. On the other hand, diode D_{B1} bypasses R_{BD}, and Q_{B3} is turned on immediately. As a result, Q_{B4} is turned off, Q_{B5} is turned on and consequently, the main switch S_1 is turned off. Then, I_o flows through C_s and charges it until the S_1 and S_2 voltages reach V_{in} and zero, respectively. Due to C_s, S_1 is turned off under the ZVS condition.

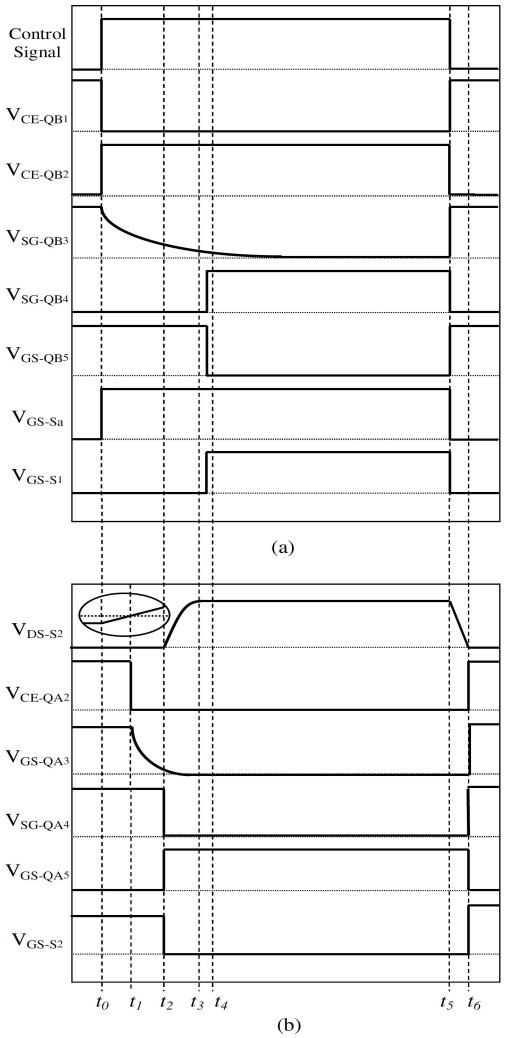

Fig. 6. Theoretical waveforms of the gate drive circuits. (a) circuit B waveforms and, (b) circuit A waveforms.

Interval 7 [t_6 – t_0+T]: The body diode of S_2 starts to conduct and the drain-source voltage of S_2 becomes negative. In this condition, the base-emitter voltage of Q_{A1} is higher than that of Q_{A2}, and Q_{A2} is turned off. Therefore, Q_{A3} is turned on immediately through D_A. Also, Q_{A4} is turned on, Q_{A5} is turned off and as a result, SR switch S_2 is turned on under ZVS.

III. DESIGN GUIDELINES

The design of the ZVT synchronous buck converter is discussed in [1]. In this converter, during the second interval, the L_a current increases from I_o to its maximum value at the end of this interval defined as I_1.

Therefore, additional energy proportional to (I_1–I_o) is stored in L_a. This additional energy is used to discharge C_s when the output voltage is less than $V_{in}/2$. The required value for I_1 to completely discharge C_s, and the durations of the various operating intervals are also discussed in [1]. Consequently,

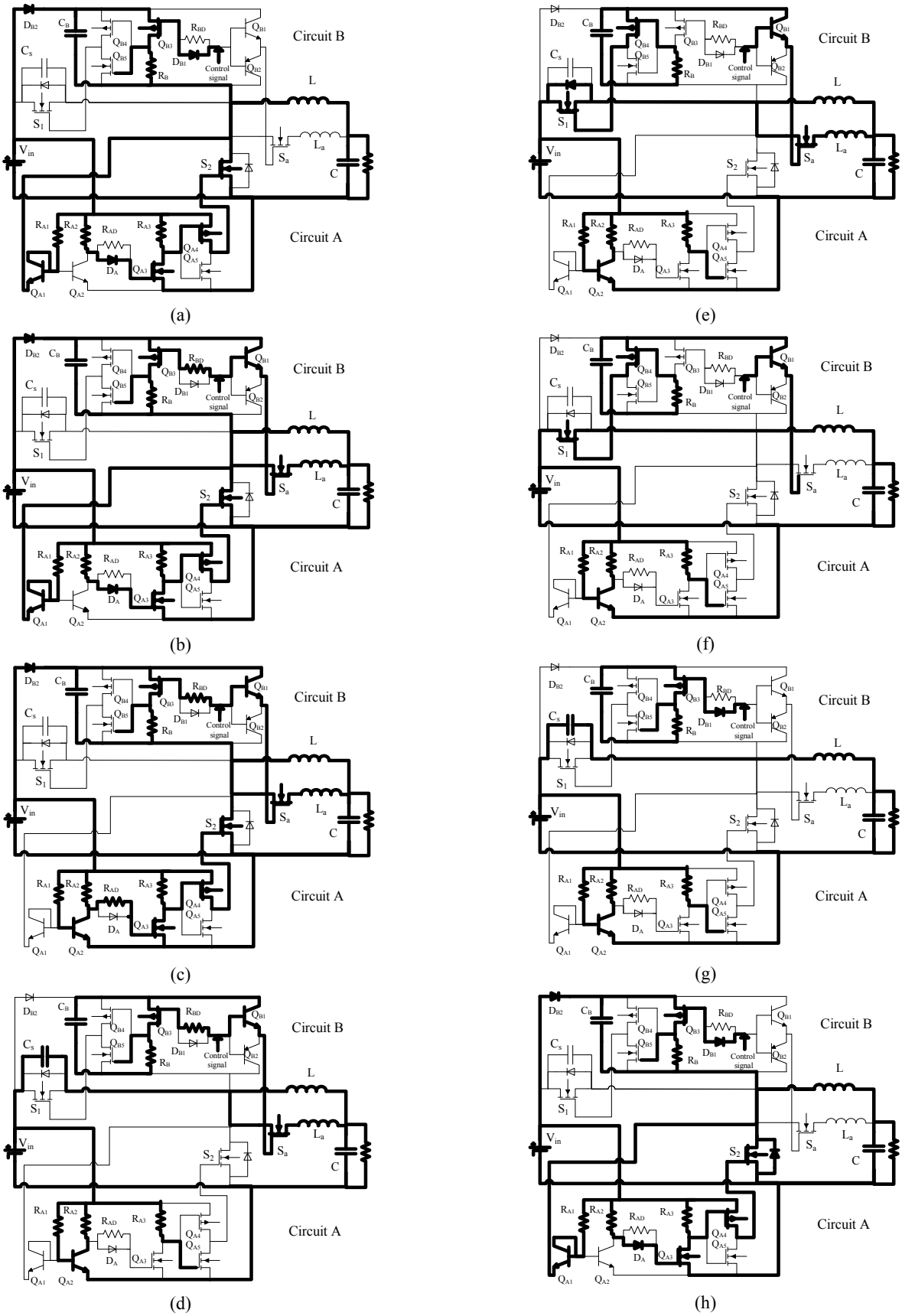

Fig. 7. Equivalent circuit for each operating interval. (a) before t_0, (b) $[t_0 - t_1]$, (c) $[t_1 - t_2]$, (d) $[t_2 - t_3]$, (e) $[t_3 - t_4]$, (f) $[t_4 - t_5]$, (g) $[t_5 - t_6]$ and (h) $[t_6 - t_0 + T]$.

only the gate drive circuits need to be designed. Resistor R_{AD} is used to reduce the gate-source voltage of Q_{A3} as follows:

$$V_{gs\_Q_{A3}} = V_{in} e^{-\frac{t-t_1}{\tau_A}}. \quad (1)$$

where

$$\tau_A = R_{AD} \times C_{gs\_Q_{A3}}. \quad (2)$$

Q_{A3} must be on during Interval 2 and it should turn off at the end of this interval. For this purpose, V_{gs_QA3} must be greater than its threshold voltage in Interval 2 and it must reach V_{th_QA3} at t_2. Thus, τ_A is obtained from (1) as:

$$\tau_A = -\frac{t_2 - t_1}{\ln \frac{V_{th\_Q_{A3}}}{V_{in}}}. \quad (3)$$

Finally, from (2) and (3), R_{AD} can be calculated as follows:

$$R_{AD} = -\frac{t_2 - t_1}{C_{gs\_Q_{A3}} \times \ln \frac{V_{th\_Q_{A3}}}{V_{in}}}. \quad (4)$$

R_{BD} discharges the input capacitor of Q_{B3} as follows:

$$V_{gs\_Q_{B3}} = -V_{in} e^{-\frac{t-t_0}{\tau_B}}. \quad (5)$$

where

$$\tau_B = R_{BD} \times C_{gs\_Q_{B3}}. \quad (6)$$

Therefore, Q_{B3} turns off with following delay:

$$t_D = -\tau_B \ln \frac{V_{th\_Q_{B3}}}{V_{in}}. \quad (7)$$

Q_{B3} must be turned off during Interval 4 when the body diode of S_1 conducts. Thus, t_D should be greater than t_3-t_0 and smaller than t_4-t_0. Finally, from (6) and (7), R_{BD} can be calculated as follows:

$$R_{BD} = -\frac{t_D}{C_{gs\_Q_{B3}} \times \ln \frac{V_{th\_Q_{B3}}}{V_{in}}}. \quad (8)$$

where

$$t_3 - t_0 < t_D < t_4 - t_0. \quad (9)$$

R_{AD} and R_{BD} are designed for the nominal load with t_D=t_3-t_0. By applying these resistors, at the nominal load, the main switch is turned on at the beginning of the fourth interval. At light loads, the duration of the first interval reduces and the fourth interval begins early. Thus, the main switch is turned on during the fourth interval. As a result, ZVS is guaranteed for the main switch at turn on and only the conduction time of its body diode is increased at light loads.

Power MOSFETs usually have large gate-source capacitances. In particular, Power MOSFETs with low on resistances have high die sizes. As a result, they have high gate-source capacitances. In addition, some MOSFETs may be paralleled to reduce the on resistance. Therefore, the gate drive circuits need buffers to drive these switches. The auxiliary switch S_a turns on/off as soon as the control signal becomes high/low. Therefore, a push-pull circuit is a proper buffer for the control signal. However, the main switch S_1 and the SR switch S_2, must be switched with a delay.

As discussed in the previous section, with the RC circuits, the initial signals rise/fall times increase and their values reach the threshold levels with desired delays. In this situation, if push-pull buffers are used, the drive signals have slow rise/fall times (they are soft). This can decrease efficiency because the on resistance of a power MOSFET has a reverse ratio with respect to its gate-source voltage. Thus, the on resistance is high during the interval that the gate-source voltage is between the threshold and maximum values.

Among the various buffers illustrated in Fig. 8, the theoretical analysis and simulation results show that the proper buffer for this situation is buffer IV. In buffer I, if the initial signal is soft, both of the transistors in the first stage would be on during the interval that the gate voltage is between V_{th} and (12-V_{th}). Buffer II drives the power switch through a resistor. Thus, the drive signal is soft in the rising edge. Buffer III, which is a push-pull with MOSFET, may incompletely charge or discharge the gate-source capacitor of the power switch. However, in buffer IV, when Q_1 turns off, the input capacitors of Q_2 and Q_3 discharge and charge through R at a high speed because of their low values. When Q_1 turns on, the input capacitors of Q_2 and Q_3 immediately charge and discharge through Q_1. In addition, the gate-source capacitor of the power switch, charges and discharges through the second stage transistors, immediately. Consequently, this buffer can almost generate a pulse from the initial soft signal.

In circuit B, the input voltage cannot be directly used as the supply voltage because the main switch source voltage is float. For this reason, as can be observed in Fig. 3, diode D_{B2} and capacitor C_B provide the supply voltage from the input voltage with the bootstrap technique. The first stage of circuit A must detect the polarity of a very small voltage. For this purpose, a BJT similar to Q_{A2} is used as a diode connected transistor in order to place two similar base-emitter junctions across each other.

Normally, control ICs have an under voltage lock out (UVLO) threshold. By using a control IC with an UVLO threshold of about 8 volts, the converter would not have problem in the transition time. During the transition time, until the input voltage is below the operational voltage of the control IC, it remains off. Thus, no control signal is generated. In this situation, the proposed driver circuit does not provide gate pulses for the main and auxiliary switches. Thus, the

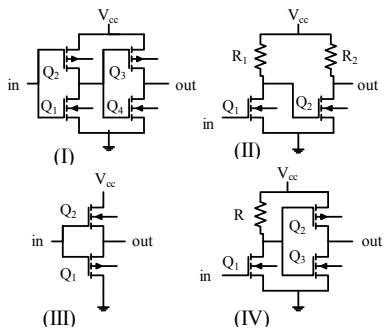

Fig. 8. Various buffers to drive a MOSFET.

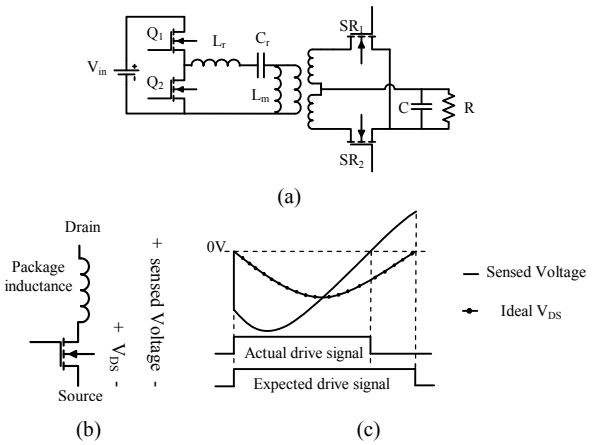

Fig. 9. (a) LLC resonant converter with SR, (b) simple schematic of the SR package, and (c) deviation in the sensed voltage due to SR package inductance.

converter stays off with no output voltage. In addition, by implementing the soft start technique, the overshoot problem is solved.

IV. Other Applications for the Proposed SR Driving Scheme

The proposed SR driver is also proper for many high-frequency resonant converters and some high-frequency discontinuous current mode PWM circuits such as LLC resonant converter and DCM synchronous buck converter. As it is mentioned in the introduction, in voltage-driven method, the drain-source voltage of the SR is used to drive it. The existence of parasitic inductances in MOSFET packages is inevitable. As it can be observed from Fig. 9(b), the developed voltage across the MOSFET drain-source terminals is actually the sum of the MOSFET resistive voltage (which is the ideal V_{DS}) and the package inductive voltage. Fig. 9(a) shows an LLC resonant converter with SR. In this converter, the SR current with a positive slope goes to zero and then the SR turns off. In this condition, as shown in Fig. 9(c), the sensed voltage of the SR terminals deviates greatly from the ideal V_{DS} and it goes to zero early (due to the positive voltage of the package inductor). As it can be observed, if this sensed voltage is directly used to drive the SR, the drive signal would be much shorter than the expected signal. As a result, the SR would be turned off much earlier than the expected time and its body diode would start conducting [27]. This phenomenon becomes noticeable at high frequencies. A similar condition exists for DCM synchronous buck converter. However, the proposed SR driver can produce a delay in the SR turn off signal. Thus, with the proposed driver, the SR used in any of these converters remains on after the sensed voltage becomes positive and is driven at almost ideal condition.

V. Experimental Results

A 12V input and 3.3V/15A output laboratory prototype is designed and implemented to operate at 100kHz switching frequency. In the main circuit of the converter, IRF1404 with $R_{ds(on)}$=4mΩ is used for the main and SR switches. In addition, an IRF1404 with a S30SC4M diode create the unidirectional auxiliary switch S_a. Finally, the values of L, L_a and C_s are 8.2μH, 0.12μH and 15nF, respectively. In the gate drive circuits, BS170 and BS250 are used for all of the N-Channel and P-Channel MOSFETs, respectively. All of the NPN BJTs are BC107 and the PNP BJT is a BC177. 1N4148 is used for all of the diodes. Based on the design procedure explained in the previous section, the values of R_{AD} and R_{BD} are calculated as 17kΩ and 7.2kΩ, respectively. A 1μF capacitor is used for C_B. In addition, 1kΩ resistors are used for R_{A1}, R_{A2}, R_{A3} and R_B. The experimental waveforms of the main circuit are presented in Fig. 10. These waveforms show that the synchronous buck converter operates properly when the proposed drivers are incorporated. Fig. 10(a) shows that the main switch is turned on under the ZVS condition while the duty cycle is equal to 0.3 (<0.5). Therefore, it can be concluded that the drivers have provided proper delays to turn off and turn on the SR and the main switches, respectively. The experimental signals of circuit B are illustrated in Fig. 11. In this figure, the signals are shown with respect to the main switch source. When the control signal becomes high, the gate signal of Q_{B3} begins to increase with slow rise time. In this condition, the source-gate voltage of Q_{B3} decreases slowly, and Q_{B3} turns off with a delay. Therefore, R_{BD} has provided the required delay. In addition, as it can be observed, the gate-source voltage of the main switch becomes high with a delay in comparison to the control signal. Note that this signal has an acceptable rise time. The experimental waveforms of circuit A are shown in Fig. 12. As it can be seen, the gate-source voltage of Q_{A3} has a slow fall time and reaches the threshold voltage with a delay. After this delay, the gate-source voltage of Q_{A5} becomes high and the gate-source voltage of the SR becomes low with a sharp fall time. As a result, the proposed SR driver has provided a gate signal with the desired delay and fall time. Experimental results under light load (20% of the nominal load) are provided in Fig. 13. In addition, the converter efficiency curve is shown in Fig. 14.

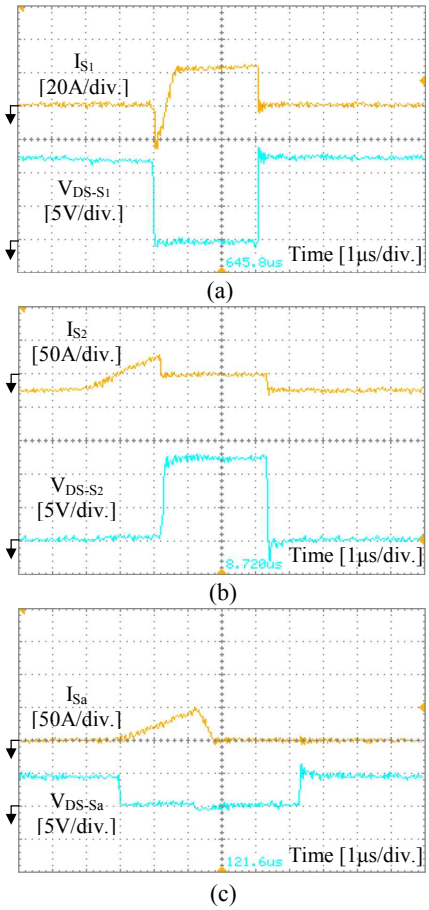

Fig. 10. (Top waveform) current and (bottom waveform) voltage of (a) S_1 (vertical scale is 5V/div or 20A/div). (b) S_2 (vertical scale is 5V/div or 50A/div). (c) S_a (vertical scale is 5V/div or 50A/div). Time scale is 1μs/div.

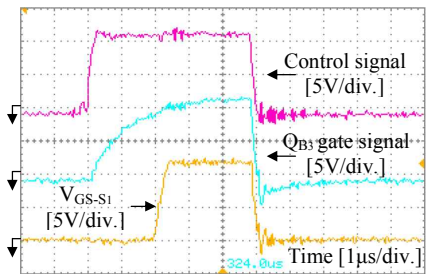

Fig. 11. Experimental waveforms of circuit B. (Top) control signal, (middle) gate signal of Q_{B3}, (bottom) gate signal of the main switch (the signals are shown with respect to the main switch source).

VI. CONCLUSIONS

Two new gate drive circuits are presented in this paper. One circuit drives the synchronous rectifier with the voltage-driven method. The other circuit drives both the main and auxiliary switches by the control signal. Both gate drive circuits are supplied by the input voltage. The ZVT synchronous buck converter along with the introduced gate drive circuits is analyzed. Various operating modes are discussed and the design guidelines are explained. Finally, a prototype converter is implemented to verify the validity of the theoretical analysis.

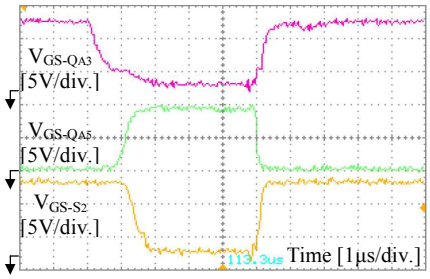

Fig. 12. Experimental waveforms of circuit A. (Top) gate-source voltage of Q_{A3}, (middle) gate-source voltage of Q_{A5}, (bottom) gate-source voltage of the SR switch.

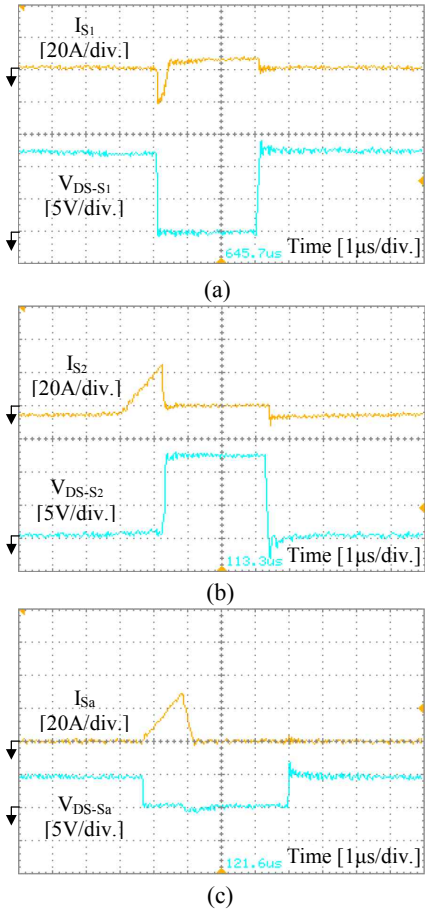

Fig. 13. Experimental waveforms under light load (20% of the nominal load). Current waveform (Top) and voltage waveform (bottom) of (a) S_1 (b) S_2 (c) S_a.

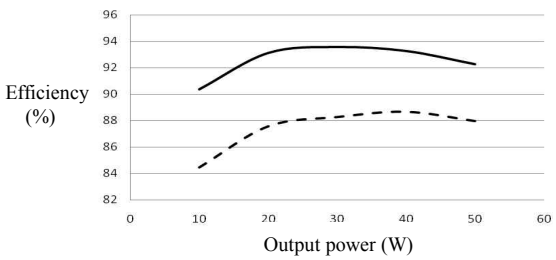

Fig. 14. Efficiency comparison of the proposed circuit (continuous line) and a hard-switching synchronous buck converter (broken line) versus output power.

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