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Robust Active LED Driver with High Power Factor and Low Total Harmonic Distortion Compatible with a Rapid-Start Ballast

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Abstract

A new active LED driver with high power factor (PF) and low total harmonic distortion (THD) compatible with a rapid-start ballast is proposed. An LC input filter is attached to the ballast to increase PF and reduce THD. A boost converter is then installed to regulate the LED current, where an unstable operating region has been newly identified. The unstable region is successfully stabilized by feedback control with two zeroes. The extremely high overall system of the 10th order is completely analyzed by the newly introduced phasor transformed circuits in static and dynamic analyses. Although a small DC capacitor is utilized, the flicker percentage of the LED is drastically mitigated to 1% by the fast controller. The proposed LED driver that employs a simple controller with a start-up circuit is verified by extensive experiments whose results are in good agreement with the design.

Key words: Active LED driver, High power factor, Low total harmonic distortion, Phasor analysis, Rapid-start ballast

I. INTRODUCTION

Conventional fluorescent lamps are being replaced with light emitting diode (LED) lamps to save energy and preserve the environment [1]-[13]. An LED lamp has higher efficiency than fluorescent lamps; its lifetime is longer than 50,000 hours, which is approximately 10 times that of a fluorescent lamp. Many countries thus promote the use of LED lamps even though these lamps are expensive. The replacement of fluorescent lamps with LED lamps in some countries, such as Japan, is highly impeded by this issue. Rapid-start ballasts are already firmly installed inside ceilings and are difficult to replace with new switching converter-type LED drivers. A practical solution is to attach an LED driver to a rapid-start ballast instead of removing the ballast from the ceiling [14]-[16]. A few practical design issues must be considered in dealing with LED drivers. First, the use of a large DC input capacitor for the LED driver should be avoided because it produces a large peak inrush current and may cause occasional fires inside the rapid-start ballast [16]. Second, the power factor (PF) and total harmonic distortion (THD) of the LED lamp should not be reduced although the power level of an LED lamp is typically half that of a fluorescent lamp . This problem can be resolved by attaching an appropriate LC filter to the rapid-start ballast [16]. Third, accurate static and dynamic circuit models, including a switching converter and a highly nonlinear rapid-start ballast, are required for the design of an LED lamp. This cumbersome problem can be addressed by the recently proposed unified general phasor transformation [18].

An active LED driver that is compatible with the rapid-start ballast and meets the three design considerations mentioned above is proposed in this study. A small DC capacitor with an LC filter is attached to the ballast, and a boost converter regulates the LED array (Fig. 1). Unlike a conventional boost converter, the power source of the converter is not an ideal voltage source but the small DC capacitor linked to an output of the ballast whose characteristic is highly nonlinear. Furthermore, an unstable operating region is identified in this study; such region can be avoided by selecting an appropriate duty cycle of the boost converter. The complete DC and AC phasor transformed circuit models for the 10th order LED lamp system developed in this study allow for the drastic reduction in LED ripple current even with a small DC capacitor. This design is extensively verified by experiments.

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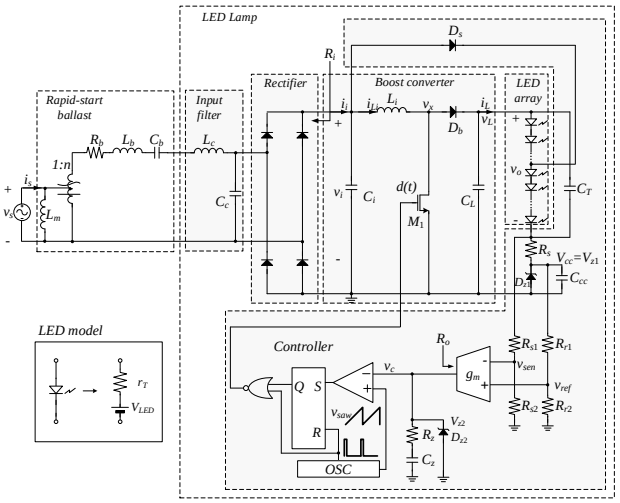


Fig. 1. Proposed boost converter-type LED lamp with a control circuit that is compatible with a rapid-start ballast..

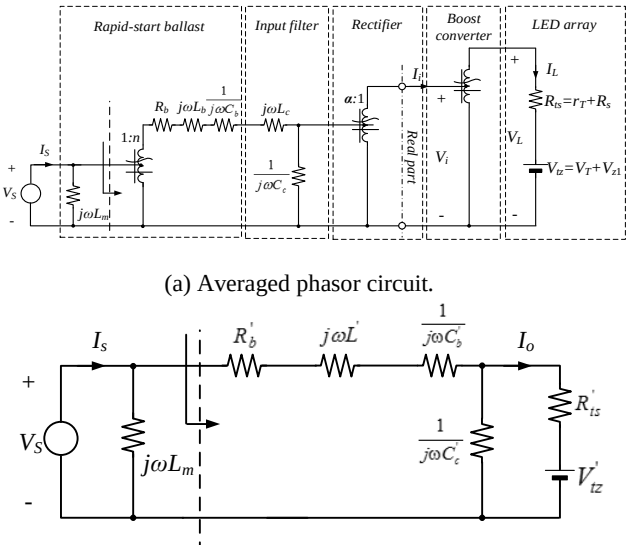
II. STATIC ANALYSIS AND DESIGN OF THE PROPOSED ACTIVE LED DRIVER

The LED lamp (Fig. 1) operates with a rapid-start ballast and is composed of an LED array and the proposed LED driver, which includes an input filter, a rectifier, a boost converter, and a controller. Regulated current is provided by controlling the duty cycle of the boost converter for the LED array regardless of the large rectified ripple voltage of 120 Hz caused by the small DC input capacitor. This capacitor is where the LED current obtains the feedback from the source voltage variation of the rapid-start ballast and other variations, such as temperature.

A. Selection of the Converter

A DC–DC converter is necessary to make the LED current constant regardless of the ripple voltage without any power loss. Galvanic isolation is not required for tubular-type LEDs; hence, an isolation transformer need not be used. Instead, a single-stage converter should be utilized considering the complexity of the gate driver and voltage rating of the LED array. Among various DC–DC converters, the boost converter was selected in this study because of the simple driver structure of its main MOSFET (Fig. 1). Although soft switching provides high efficiency in general, it is not considered because the use of high switching frequency to reduce the converter filter size does not contribute to the overall filter size, where the input filter is already extremely large for the operating frequency of 60 Hz. For a buck converter, the n-MOSFET utilized for a power switch requires a bootstrap gate driver, such as IR2101, which does not work properly when the load current is small.

The LED employed in this study (i.e., DG-82A83C-001-5S-3) has forward voltage drop V_{LED} = 3.0 V and equivalent series resistance r_{LED} = 6.3 Ω at 60 mA. The



(a) Averaged phasor circuit.

(b) Simplified circuit with the transformers removed.

Fig. 2. Static phasor transformed circuits of Fig. 1.

LED array can then be characterized by r_T and V_T as follows [10]:

$$r_T = m \cdot r_{LED} \qquad V_T = m \cdot V_{LED}\,, \tag{1}$$

where *m* is the number of series-connected LEDs. The output voltage applied to the LED array (Fig. 1) becomes the following:

$$V_o = V_T + I_L r_T \quad . \tag{2}$$

The voltage drop of an LED at 60 mA is determined from Eq. (2) as 3.38 V, and its power becomes 0.20 W. This condition means that approximately 100 LEDs are required for an output power of 20 W.

B. Derivation of the Static Models of the LED Lamp

The static behavior of the proposed lighting system (Fig. 1) was fully analyzed in this study through phasor transformations [17], [18], which enable us to determine the amplitude and phase of AC circuit variables such as in a DC circuit. By applying the transformation, an averaged DC phasor circuit was obtained (Fig. 2(a)). The imaginary resistors represent the reactance of inductors and capacitors in the steady state. The rapid-start ballast is highly nonlinear, but its parameters are assumed to be fixed at an operating point. The input filter composed of L_c and C_c is attached to this ballast to satisfy PF and THD regulations.

The boost converter and rectifier can be transformed to equivalent auto-transformers whose turn ratios are the complementary values of their corresponding switch duty cycles [19]. The boost converter and rectifier are assumed to operate in the continuous conduction mode (CCM) so that they can be replaced with the averaged switched transformers. All variables, including V_s and I_s, are represented as phasors and the Zener diode voltage V_{z1}. The LED array is modeled as DC

voltage source V_T and dynamic resistance r_T. Removing the complex transformer for the equivalent circuit of the rectifier (Fig. 2(a)) from the left side is possible with a recently proposed method [22]. By referring all parameters into the primary side of the rapid-start ballast while removing all transformers (Fig. 2(b)), the source current is as follows:

$$I_s = I_s\big|_{V_{tz}^{'}=0} + I_s\big|_{V_s=0} = \frac{V_s}{j\omega L_m} + \left(\frac{V_s}{R_b^{'} + j\omega L^{'} + \frac{1}{j\omega C_b^{'}} + \frac{R_{ts}^{'}}{1+j\omega C_c^{'} R_{ts}^{'}}}\right) - \left(\frac{\frac{V_{tz}^{'}}{1+j\omega R_{ts}^{'} C_c^{'}}}{R_b^{'} + j\omega L^{'} + \frac{1}{j\omega C_b^{'}} + \frac{R_{ts}^{'}}{1+j\omega R_{ts}^{'} C_c^{'}}}\right). \quad (3)$$

From Eq. (3), PF can be derived by identifying its real and imaginary parts as follows:

$$\mathrm{PF} = \frac{\mathrm{Re}(I_s)}{\sqrt{\mathrm{Re}(I_s)^2 + \mathrm{Im}(I_s)^2}} \quad (4)$$

$$\mathrm{L}^{'} = \frac{\mathrm{L_b} + \mathrm{L_c}}{\mathrm{n}^2} \quad \mathrm{C_b^{'}} = \mathrm{n}^2 \mathrm{C_b} \quad \mathrm{C_c^{'}} = \mathrm{n}^2 \mathrm{C_c} \quad \mathrm{R_b^{'}} = \frac{\mathrm{R_b}}{\mathrm{n}^2} \quad (5)$$

$$R_{ts}^{'} = \frac{(1\text{-}D)^2 R_{ts} \alpha^2}{n^2} \quad \alpha = \frac{2\sqrt{2}}{\pi} \quad V_{tz}^{'} = \frac{(1\text{-}D) V_{tz}}{\alpha n} \quad . (6)$$

From Eq. (6), the complex transformer is assumed to have a zero phase for simplicity so that the real part operator of Fig. 2(a) can be neglected; only the real value of equivalent voltage source $V_{tz}^{'}$ is provided. Given the nonlinearity of the ballast, the exact values of L_c and C_c were determined by experiments, which will be described in the succeeding section.

C. Determination of Stable Operating Points Using a Simplified Model

As described in the previous section, a detailed analysis of the lighting system (Fig. 2(a)) may yield inaccurate results because of the nonlinearity of the rapid-start ballast and rectifier. The left part of the rectifier circuit must be simplified to understand the behavior of the boost converter with the LED array. The output *V-I* characteristic of the rectifier in the steady state was measured as shown in Fig. 3. It was found to be quite linear for the operating range as shown in Fig. 4; hence, the system at the output of the rectifier can be characterized as equivalent resistance R_i = 270 Ω and voltage source V_{eq} = 168 V as follows:

$$V_i = V_{eq} - R_i \cdot I_i \quad . \quad (7)$$

The load current of LED array I_L versus the duty cycle of boost converter D in the steady state is derived from Fig. 4 as follows:

$$I_L = (1-D) I_i = D' \frac{V_{eq} - D' V_{tz}}{R_i + D'^2 R_{ts}}, \quad (8)$$

where

$$D' = 1 - D \, . \quad (9)$$

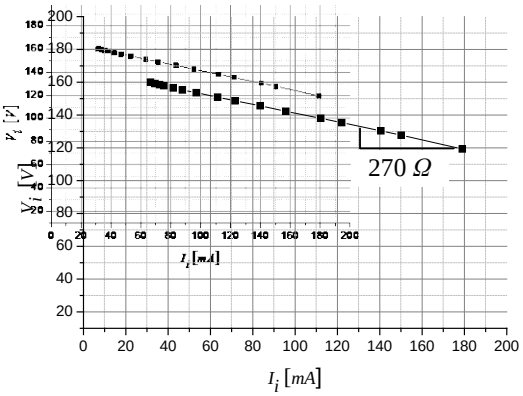


Fig. 3. Measured static rectifier output characteristic curve.

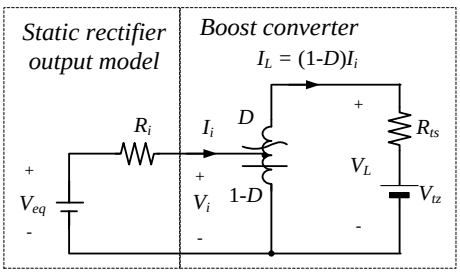


Fig. 4. Simplified model of the static rectifier output model and boost converter.

The critical duty cycle D_c that maximizes I_L is derived from Eq. (8) as follows:

$$D_c = D\Big|_{\frac{dI_L}{dD}=0} = \frac{V_{eq} R_{ts} + V_{ts} R_i - \sqrt{V_{ts}^2 R_i^2 + V_{eq}^2 R_{ts} R_i}}{V_{eq} R_{ts}} . \quad (10)$$

For the LED array of m = 100, the calculated I_L from Eq. (8) is compared with the experimental result as shown in Fig. 5. I_L increases for duty cycle D up to the critical value D_c = 0.75 similar to the conventional boost converter; however, it decreases when D is larger than D_c. Load current I_L can be either controlled for the lower region ($D < D_c$) or the higher region ($D > D_c$). However, the lower region is preferred because rectifier current *Ii* for the higher region increases for the same load current I_L as shown in Eq. (8). The maximum duty cycle should thus be restricted to $D < D_c$. In this study, the Zener diode D_{z2} was employed to limit the maximum duty cycle by clamping control voltage v_c .

III. Dynamic Analysis and Design of the Proposed Active LED Driver

A. Derivation of the Dynamic Models of the LED Lamp

Controlling the proposed active LED driver is challenging because of the highly nonlinear characteristics and the 10th order complexity of the overall system. As shown in Fig. 1, the proposed controller includes the differential current sensing part and frequency compensation circuit components C_T, R_z,

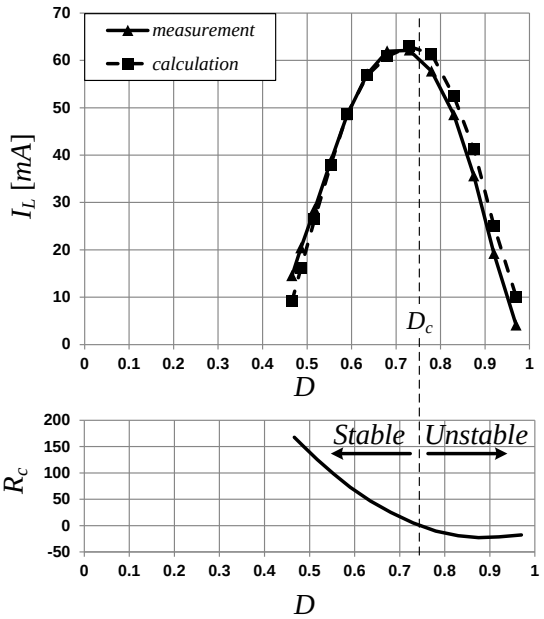


Fig. 5. Measured and analyzed static characteristics of I_L vs. D with the critical value of R_c of Eq. (17) that determines the dynamic stability of the LED driver.

and C_z as well as a conventional PWM control circuit. The dynamic models for the overall LED driver should be derived to design the proposed controller. As shown in Fig. 6(a), the models can be regarded as operating in a quasi-steady state; the same static model used in the steady state (Fig. 4) was thus adopted. This condition can be justified by the very slow dynamic response of the rapid-start ballast and input filter. Its operating frequency of approximately 60 Hz is more than 20 times lower than the bandwidth of the dynamics of the controller. One difference is rectified current ripple i_r, which is a surge current of 120 Hz that acts as a major disturbance to the control system. The proposed controller should mitigate these ripple harmonics by a fairly fast control loop. Considering that ripple voltage v_r that appears in capacitor C_i is easy to measure and analyze, an approximated equivalent circuit can be obtained as shown in Fig. 6(b) by applying the Thevenin theorem to the left part of the dotted line of the circuit of Fig. 6(a). The detailed analysis of v_r for a given i_r is complicated and avoided in this study. Instead, it will be measured for an open loop control condition and regarded as an independent source from here on.

The large signal model of Fig. 6(b) is then perturbed, and an AC model is obtained in the frequency domain by removing all DC sources but including the ripple voltage source [19]. The harmonic ripples and perturbed small signals appear in the same equivalent circuit; this occurrence is uncommon. Finally, the most simplified model (where the auto transformer of the boost converter is removed) is obtained as shown in Fig. 6(d). A filtered circuit with three independent voltage sources appears.

B. Transfer Function of Load Voltage vs. Duty cycle: $G_d(s)$

For the AC analysis, DC operating point I_i is calculated from Fig. 4 as follows:

$$I_i = \frac{V_L - V_{tz}}{D' R_{ts}} \quad . \tag{11}$$

The input side impedance is derived from Fig. 6(c) as follows:

$$Z_i(s) = R_i // \frac{1}{sC_i} + sL_i = \frac{s^2 L_i R_i C_i + sL_i + R_i}{1 + sR_i C_i} . \tag{12}$$

The small signal transfer function of boost converter output $\hat{V}_L(s)$ in CCM as a function of duty cycle $\hat{D}(s)$ of the switch can be derived from Fig. 6(d) for the two small signal-independent sources $I_i \hat{D}(s)$ and $V_L \hat{D}(s)$.

From Fig. 6(d), the transfer function from $\hat{D}(s)$ to $\hat{V}_L(s)$ when $I_i \hat{D}(s)$ is zero is as follows:

$$G_{d1}(s) \equiv \left. \frac{\hat{V}_L(s)}{\hat{D}(s)} \right|_{I_i \hat{D}(s)=0} \tag{13}$$

$$= \frac{V_L}{D'} \cdot \frac{D'^2 R_{ts}(1 + sR_i C_i)}{s^3 L_i R_i C_i R_{ts} C_L + s^2 (L_i R_i C_i + L_i R_{ts} C_L) + s(L_i + C_L R_{ts} R_i + R_{ts} R_i C_i D'^2) + R_i + R_{ts} D'^2}$$

The transfer function from $\hat{D}(s)$ to $\hat{V}_L(s)$ when $V_L \hat{D}(s)$ is zero is derived with Eq. (11) as follows:

$$G_{d2}(s) \equiv \left. \frac{\hat{V}_L(s)}{\hat{D}(s)} \right|_{V_L \hat{D}(s)=0} \tag{14}$$

$$= \frac{V_{tz} - V_L}{D'} \cdot \frac{s^2 L_i R_i C_i + sL_i + R_i}{s^3 L_i R_i C_i R_{ts} C_L + s^2 (L_i R_i C_i + L_i R_{ts} C_L) + s(L_i + C_L R_{ts} R_i + R_{ts} R_i C_i D'^2) + R_i + R_{ts} D'^2}$$

From Eqs. (13) and (14), transfer function $G_d(s)$ from $\hat{D}(s)$ to $\hat{V}_L(s)$ can be calculated as

$$G_d(s) \equiv \frac{\hat{V}_L(s)}{\hat{D}(s)} = \left. \frac{\hat{V}_L(s)}{\hat{D}(s)} \right|_{I_i \hat{D}(s)=0} + \left. \frac{\hat{V}_L(s)}{\hat{D}(s)} \right|_{V_L \hat{D}(s)=0} = G_{d1}(s) + G_{d2}(s) \tag{15}$$

$$= \frac{1}{D'} \cdot \frac{s^2 (V_{tz} - V_L) L_i R_i C_i + s\{V_L D'^2 R_{ts} R_i C_i + (V_{tz} - V_L) L_i\} + (V_{tz} - V_L) R_i + V_L D'^2 R_{ts}}{s^3 L_i R_i C_i R_{ts} C_L + s^2 (L_i R_i C_i + L_i R_{ts} C_L) + s(L_i + C_L R_{ts} R_i + R_{ts} R_i C_i D'^2) + R_i + R_{ts} D'^2}$$

The zero frequency response is obtained from Eq. (15) as follows:

$$G_d(0) = \frac{1}{D'} \cdot \frac{(V_{tz} - V_L) R_i + V_L D'^2 R_{ts}}{R_i + R_{ts} D'^2} \equiv \frac{V_L}{D'} \cdot \frac{R_c}{R_i + R_{ts} D'^2} , \tag{16}$$

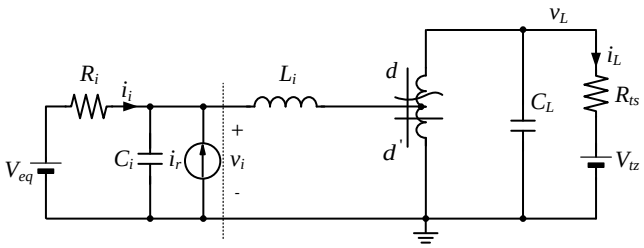
where R_c is critical resistance that determines the proposed system stability as follows:

$$R_c = (\frac{V_{ts}}{V_L} - 1) R_i + D'^2 R_{ts} . \tag{17}$$

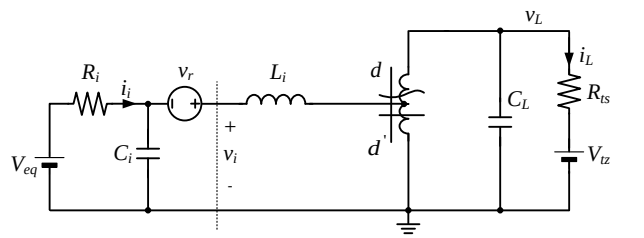
When the numerator of Eq. (16) is positive (i.e., $R_c > 0$), the gain is positive and thus corresponds to the positive slope of I_L in Fig. 5. This condition is justified considering that I_L is proportional to V_L as follows:

$$V_L = V_{ts} + I_L R_{ts} \tag{18}$$

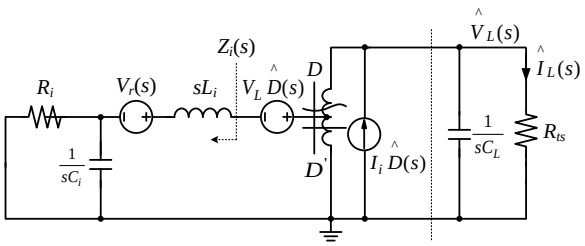
or



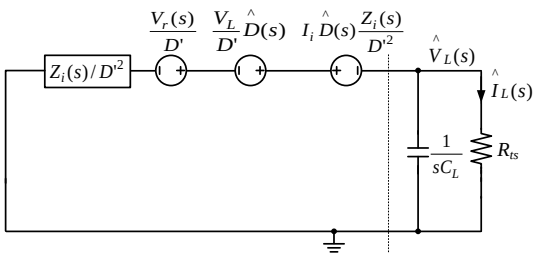
(a) Large signal averaged model of the converter, including the rectified current ripple in the time domain.



(b) Approximated model of (a) obtained by replacing the rectified current ripple with its equivalent voltage source in the time domain.



(c) AC model of (b) obtained by removing all DC sources but including the ripple and perturbed sources in the frequency domain.

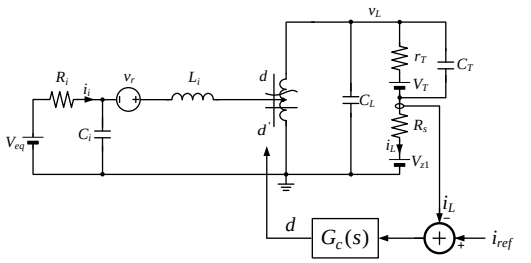


(d) Simplified model of (c) obtained by removing the auto transformer in the frequency domain.

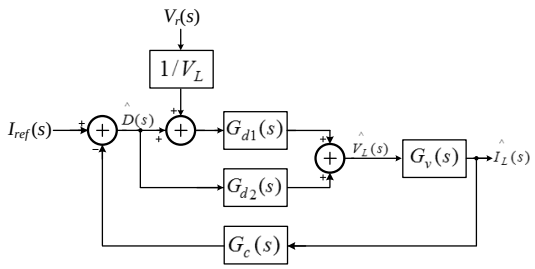
Fig. 6. Derivation of the dynamic models of the proposed LED driver with the rectified ripple disturbance of the dynamic stability of the LED driver.

$$G_d(0) = \frac{\partial V_L}{\partial D} = \frac{\partial I_L}{\partial D} R_{ts} . \quad (19)$$

Critical duty cycle D_c that maximizes I_L of Eq. (10) is also obtained from Eq. (17) when R_c = 0 as shown in the lower part of Fig. 5. Notably, the R_c of Eq. (17) should be positive to keep the proposed system stable. The first term of Eq. (17) is always negative as can be easily identified from Eq. (18).



(a) Control signals in the time domain.



(b) Control block diagram of the frequency domain.

Fig. 7. Overall control block diagram of the proposed LED driver of Fig. 1.

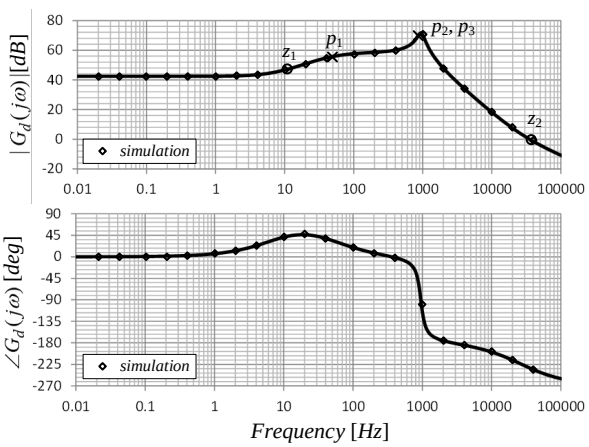


Fig. 8. Calculated bode plot of boost converter transfer function G_d (s) using Eq. (15) when D = 0.65. The diamond-shaped symbols denote the points of the simulated AC response of Fig. 6(b) to verify this calculation.

A. Transfer Function of Load Voltage vs. Rectified Ripple Voltage: $G_r(s)$

As discussed in the previous section, ripple voltage $V_i(s)$ is adisturbance, and its transfer function to load voltage $\hat{V}_L(s)$ should be obtained to mitigate the effect of this disturbance on the ripple current of the LED. This transfer function is easily derived from Fig. 6(d) in a very similar manner to Eq. (13) as follows:

$$G_r(s) \equiv \frac{\hat{V}_L(s)}{V_r(s)} = \frac{1}{D'} \cdot \frac{D'^2 R_{ts}(1+sR_iC_i)}{s^3 L_iR_iC_iR_{ts}C_L + s^2(L_iR_iC_i + L_iR_{ts}C_L) + s(L_i + C_LR_{ts}R_i) + R_i + R_{ts}(1+sR_iC_i)D'^2} = \frac{G_{d1}(s)}{V_L} \quad (20)$$

B. Transfer Function of Load Current vs. Load Voltage: $G_v(s)$

The overall configuration of the proposed controller is redrawn in Fig. 7(a). All the circuit parameters at the LED load side are highlighted. Fig. 7(a) is modeled for the complete modeling of the proposed LED driver for use in subsequent sections. Transfer function $G_v(s)$ is defined for perturbed load current $\hat{I}_L(s)$ against perturbed load voltage $\hat{V}_L(s)$ and obtained from Fig. 7(a) as follows:

$$G_v(s) \equiv \frac{\hat{I}_L(s)}{\hat{V}_L(s)} = \frac{1+sr_TC_T}{r_T+R_S+sr_TR_SC_T} \approx \frac{1}{r_T}\frac{1+sr_TC_T}{1+sR_SC_T} \ (\because r_T >> R_S). \quad (21)$$

C. Transfer Function of the Control Circuit: $G_c(s)$

The transfer function of the control circuit (Fig. 1) from $\hat{I}_L(s)$ to $\hat{D}(s)$ can be determined as follows:

$$G_c(s) \equiv -\frac{\hat{D}(s)}{\hat{I}_L(s)} = \frac{\hat{V}_{sen}(s)}{\hat{I}_L(s)} \cdot \frac{-\hat{V}_c(s)}{\hat{V}_{sen}(s)} \cdot \frac{\hat{D}(s)}{\hat{V}_c(s)} = \frac{R_SR_{s2}}{R_{s1}+R_{s2}} \cdot \frac{g_mr_m(1+sR_zC_z)}{1+s(r_m+R_z)C_z} \cdot \frac{1}{V_{saw}} \quad (22)$$

where g_m and r_m are the gain and output resistances of the operational transconductance amplifier (OTA), respectively. The amplitude of the saw tooth of the PWM is denoted as V_{saw}.

D. Controller Stability Design

The overall control block diagram of the proposed LED driver is drawn in Fig. 7(b) by combining the transfer functions of Eqs. (13) to (22). The overall transfer function for the reference current input is derived from Fig. 7(b) with Eq. (15) as follows:

$$H_1(s) \equiv \frac{\hat{I}_L(s)}{I_{ref}(s)} = \frac{G_c(s)G_d(s)G_v(s)}{1+G_c(s)G_d(s)G_v(s)} \quad . \quad (23)$$

The overall transfer function for the ripple voltage input is derived from Fig. 7(b) with Eq. (15) again as follows:

$$H_2(s) \equiv \frac{\hat{I}_L(s)}{V_r(s)} = \frac{1}{V_L} \cdot \frac{G_{d1}(s)G_v(s)}{1+G_c(s)G_d(s)G_v(s)} . \quad (24)$$

From Eqs. (23) and (24), the proposed LED driver is determined to have loop gain as follows:

$$LG(s) = G_c(s)G_d(s)G_v(s) \quad . \quad (25)$$

To make the system stable, converter transfer function $G_d(s)$ was examined with Eq. (15) and plotted in Fig. 8 for the circuit parameters of Table I used in the experiment. For clarity, these calculation results were verified by the circuit simulator MMSIM72 (Cadence) using the equivalent circuit in Fig. 6, which is found to be very accurate. As shown in Eq. (15), three poles and two zeroes exist in $G_d(s)$, which is rewritten as follows:

$$G_d(s) \equiv \frac{1}{D'} \cdot \frac{Z(s)}{P(s)} = \frac{1}{D'} \cdot \frac{b_2s^2+b_1s+b_0}{a_3s^3+a_2s^2+a_1s+a_0} . \quad (26)$$

From Eq. (26), the first pole and zero (i.e., p_1 and z_1, respectively) can be approximately obtained by neglecting the high-order terms at low frequency as follows:

$$P(s) = a_3s^3+a_2s^2+a_1s+a_0 \cong a_1s+a_0 \equiv a_1(s-p_1) = 0 \rightarrow p_1 = -a_0/a_1 \quad (27)$$

$$Z(s) = b_2s^2+b_1s+b_0 \cong b_1s+b_0 \equiv b_1(s-z_1) = 0 \rightarrow z_1 = -b_0/b_1 \quad . \quad (28)$$

As calculated from Eq. (28), the first pole and zero are $p_1/(2\pi)$ = -47 Hz and $z_1/(2\pi)$ = -13 Hz, respectively, which are mainly formed by large input capacitance C_i. The low-frequency pole and zero do not reduce the system stability because their values are negative and only a slight change occurs in the phase of much less than 90 degrees (Fig. 8).

However, the high-frequency zero, z_2, should be positive as far as $R_c > 0$. This condition can be proved from Eq. (26), considering $z_1 < 0$, as follows:

$$Z(s) = b_2s^2+b_1s+b_0 \equiv b_2(s-z_1)(s-z_2) \rightarrow z_1z_2 = \frac{b_0}{b_2} = \frac{V_LR_c}{-I_LR_{ts}L_iR_iC_i} < 0 \quad (29)$$

Complex poles p_2 and p_3 and positive zero z_2 are determined from Eq. (28) and Table I as $|p_2|/(2\pi) = |p_3|/(2\pi)$ = 951 Hz and $z_2/(2\pi)$ = 27 kHz, respectively. They may affect the system stability significantly because the phase of $G_d(s)$ approaches 180 degrees because of the poles and even crosses over it because of the positive zero. The complex poles are mainly formed by the L_i and C_L of the boost converter as identified from the highest-order coefficient of Eq. (27). However, the dominant pole compensation that allows the high-order dynamics to be buried cannot be used for the proposed design because fast response is crucial to eliminate the 120 Hz ripple caused by the feedback loop control.

Two additional zeroes are thus inserted to the frequency at the two poles so that they cancel each other out. The first zero is inserted to the OTA output, and the second one is added at the current sensing circuit as follows:

$$|p_2| = |p_3| = 1/R_zC_z \quad (30a)$$

$$|p_2| = |p_3| = 1/r_TC_T . \quad (30b)$$

From Eq. (30b), C_T is determined as 270 nF for r_T = 620 Ω; however, the value of R_zC_z only can be determined from Eq. (30a) for now.

E. Controller Gain Design to Mitigate the 120 Hz Ripple

Considering the increased concern over the flicker in LED lamps and its effect on human health [20], the ripple current of LEDs is mitigated in this study. The small voltage change across LEDs causes a large current variation because of the

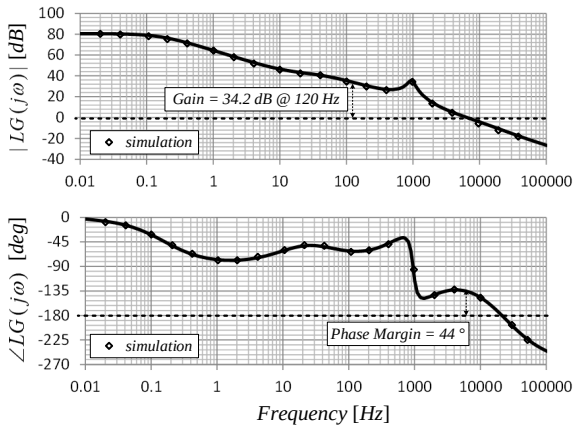


Fig. 9. Calculated bode plot of the loop gain of the proposed LED driver from Eq. (25) after being compensated. The diamond-shaped symbols denote the simulated AC response of Fig. 6(b) to verify the calculation.

small dynamic resistance. The flicker percentage (percent flicker) is defined as follows [21]:

$$Percent\ flicker \equiv 100\times\frac{A_{\max}-A_{\min}}{A_{\max}+A_{\min}} \approx 100\times\frac{I_{\max}-I_{\min}}{I_{\max}+I_{\min}} \approx 100\times\frac{I_{ripple}}{2\cdot I_{avg}}, \quad (31)$$

where A_{max} and A_{min} are the maximum and minimum brightness, I_{max} and I_{min} are the maximum and minimum currents, and I_{ripple} and I_{avg} are the ripple and average currents of the LED lamp, respectively. In Eq. (31), the brightness of the LED is assumed to be linearly proportional to its current. The targeted flicker percentage was set to approximately 1% to be nearly flicker-free. Given that the average current of the LED array in this study is 60 mA, I_{ripple} should be less than 1.2 mA to meet the specification in Eq. (31).

From Eq. (24), the ripple current can be obtained for the ripple frequency of ω_r (= 2π x 120 *rad/s*) in the steady state as follows:

$$\left|H_2(j\omega_r)\right| \equiv \left|\frac{\hat{I}_L(j\omega_r)}{V_r(j\omega_r)}\right| \cong \frac{1}{V_L}\left|\frac{G_{d1}(j\omega_r)}{G_c(j\omega_r)G_d(j\omega_r)}\right|, \quad (32)$$

where it has been approximated considering that the loop gain of Eq. (25) is much larger than 1 at the ripple frequency. Applying Eqs. (13), (15), and (26) to (32) and neglecting all poles and zeroes higher than 120 Hz result in the following:

$$\left|H_2(j\omega_r)\right| \cong \left|\frac{D'^2 R_{ts}(1+j\omega_r R_i C_i)}{\frac{R_S R_{s2}}{R_{s1}+R_{s2}}\cdot\frac{g_m}{j\omega_r C_z}\cdot\frac{1}{V_{saw}}(j\omega_r b_1+b_0)}\right| \quad \because r_m >> R_z \quad (33a)$$

$$\Rightarrow \quad C_z = \frac{R_S R_{s2} g_m \sqrt{b_0^2+(\omega_r b_1)^2}}{(R_{s1}+R_{s2})\omega_r V_{saw} D'^2 R_{ts}\sqrt{1+(\omega_r R_i C_i)^2}}\left|H_2(j\omega_r)\right| \cdot \quad (33b)$$

For the operating conditions in Table I, peak-to-peak ripple voltage V_r is measured to be approximately 13 *V* when C_i is 47 μF. C_z can thus be calculated from Eq. (33b) as 330 nF for the given value of $\left|H_2(j\omega_r)\right|$ = 1.2 mA/13 V = -80.7 dB. C_z is thus selected as 250 nF considering a 25% margin. From Eqs. (30a) and (33b), R_z is finally determined to be 670 Ω as follows:

$$R_z = 1/C_z \mid p_2 \mid \ . \quad (34)$$

As shown in Fig. 9, the compensated loop gain and phase margin at 120 Hz are 34.2 dB and 44º, respectively. This finding confirms the design of fairly high gain and appropriate margin. This calculation was verified by simulation using the equivalent circuit of Fig. 6(b); good agreement was observed.

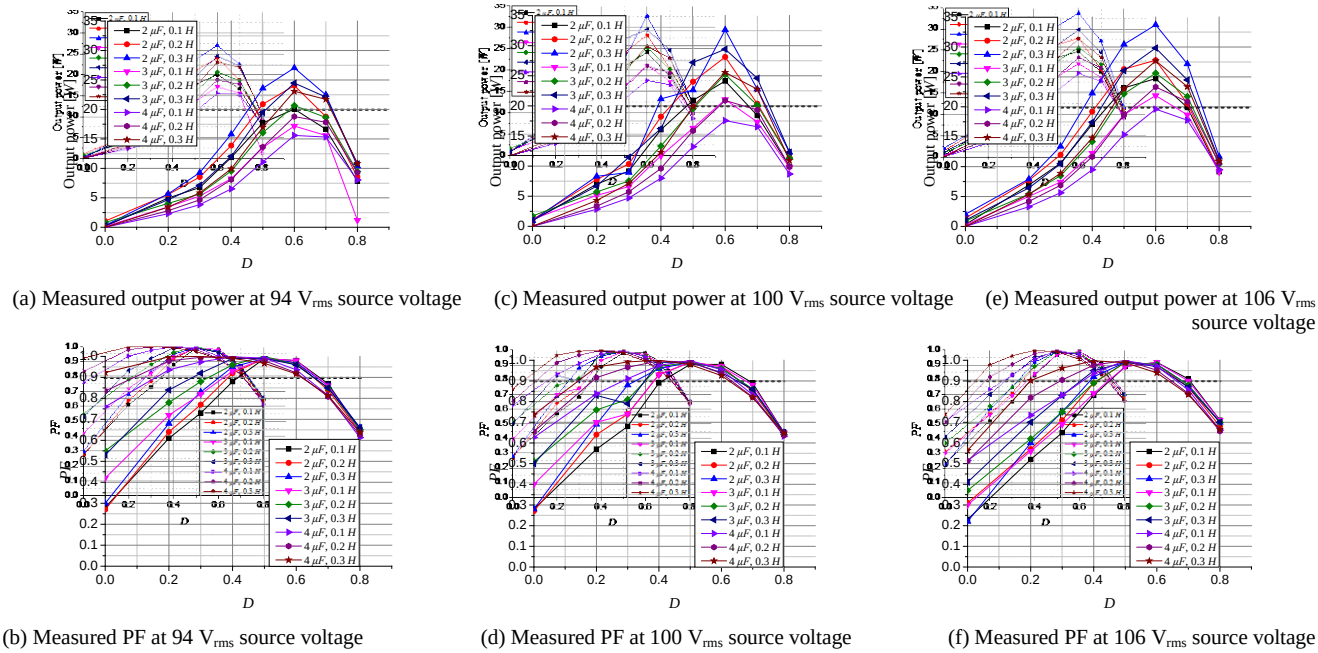
IV. Fabrications and Experimental Verifications

A. On-board Power Supply for the Controller

For the operation of the proposed LED driver without an external power supply, a cheap and simple on-board power supply is required for the controller. A Zener regulator in series with the LED array was used as shown in Fig. 1. At start-up, this regulator cannot generate any voltage because the boost converter does not operate until the regulator activates the control circuit. A start-up circuit is thus implemented by simply adopting the diode D_s connected between v_i and an appropriated intermediate point of the LED array. During start-up, D_s is turned on to provide the regulator with LED current directly from v_i. D_s is automatically turned off after start-up because load voltage v_L is increased as the boost converter operates. The point near the center of the array was carefully selected to meet this condition.

B. Experiments to Determine the Combination of L_c and C_c

Several design requirements, such as load power of 20 W, PF higher than 90%, low THD characteristics, and high efficiency, should be considered for the source voltage variable range to determine the suitable values of L_c and C_c of the input filter (i.e., from 94 V_{rms} to 106 V_{rms}). The proposed boost converter-type LED driver is very similar to the passive LED driver in terms of output power and resonant frequency [16]. Therefore, the inductor of the input filter is considered to be approximately 0.1 H to 0.3 H. The suitable value of C_c that increases PF to above 0.9 is approximately 2 μF to 4 μF from Eq. (4). However, determining the exact values of L_c and C_c is theoretically impossible because of the non-linearity of the rapid-start ballast. Eq. (4) is inaccurate because the rectifier does not always operate in CCM and the elimination of the complex transformer is approximated and imperfect. The equations can thus be used as a guideline to select L_c and C_c, which were actually determined by experiments. The load power and PF for different source voltages were measured as



(a) Measured output power at 94 V_{rms} source voltage (c) Measured output power at 100 V_{rms} source voltage (e) Measured output power at 106 V_{rms} source voltage

(b) Measured PF at 94 V_{rms} source voltage (d) Measured PF at 100 V_{rms} source voltage (f) Measured PF at 106 V_{rms} source voltage

Fig. 10. Measured output power and input power factor with respect to duty ratio D for the source voltages from 94 V_{rms} to 106 V_{rms}.

shown in Fig. 10. The results are shown in Table II. The combination of 0.1 H, 3 μF or 0.1 H, 4 μF cannot satisfy the operating point of 20 W. The value of L_c was selected as 0.2 H in consideration of the THD of the source current and the cost.

Two additional experiments were conducted to determine the exact value of C_c considering the power loss and PF by changing C_c from 2 μF to 4 μF as shown in Fig. 11. As a result, 0.2 H and 2.4 μF were selected as the optimal values of L_c and C_c, respectively.

C. *Experimental Verifications of the Design*

The proposed boost converter type LED driver was built based on the proposed design procedure and verified in the laboratory. The value of input capacitor C_i was set to as small as 47 μF to decrease the maximum peak voltage across capacitor C_b in the initial transient period [16]. This LED driver can thus ensure a stable initial start-up.

The experimental results for load voltage V_L, load current I_L, source power P_s, ballast power loss P_b, load power P_L, PF, and the efficiency for source voltages from 94 V_{rms} to 106 V_{rms} are summarized in Table III. Compared with a previous study [16], the load power in the present study is perfectly regulated within 0.1% offset error without system instability. Source voltage v_s, source current i_s, rectified voltage v_i, and LED current i_L were measured in ms (Fig. 12) to verify the line regulation. The measured rectified ripple voltage v_r and LED ripple current $\hat{i}_L$ are approximately 13 $V_{p\text{-}p}$ and 1 $mA_{p\text{-}p}$, respectively. With regard to the ratio of these peak-to-peak values to that of the 120 Hz ripples, themeasured loop gain at 120 Hz is 33.2 dB, whereas the simulated one (Fig. 9) is 34.2 dB. The discrepancy of 1.0 dB is of no practical concern; the experiment thus verifies that the proposed design guarantees the required mitigation of an LED ripple current of 1.2 $mA_{p\text{-}p}$. LED ripple current $\hat{i}_L$ with

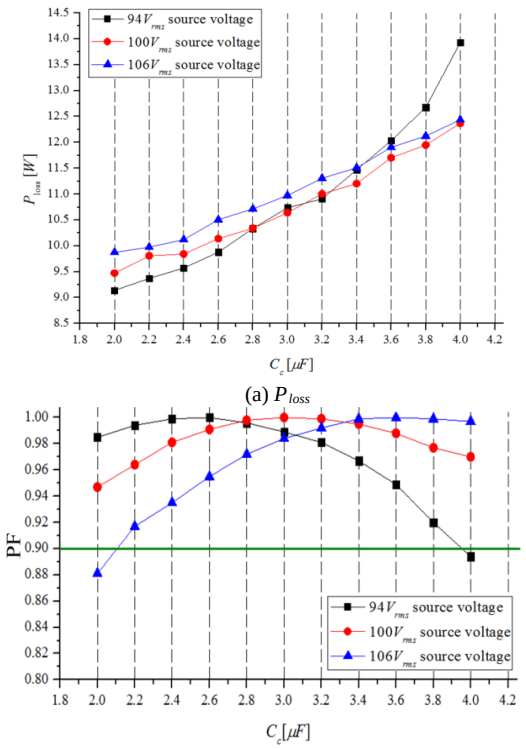
TABLE I
CIRCUIT PARAMETERS OF THE PROPOSED LED LAMP

Parameters	Values	Parameters	Values	Parameters	Values
R_i	270 Ω	r_m	4 MΩ	g_m	3 mS
r_T	620 Ω	L_i	4 mH	D	0.65
R_s	30 Ω	C_i	47 μF	V_t	300 V
R_{s1}	82 kΩ	C_L	1 μF	V_L	340 V
R_{s2}	27 kΩ	C_T	270 nF	V_{saw}	3 V
R_z	670 Ω	C_z	250 nF		

TABLE II
EXPERIMENT RESULTS

Parameters		PF			THD Regulation
L_c	C_c	V_s = 94 V_{rms}	V_s = 100 V_{rms}	V_s = 106 V_{rms}	
0.1*H*	2 μF	0.98	0.98	0.89	Unsatisfactory
	3 μF	-	0.98	0.98	Unsatisfactory
	4 μF	-	-	0.98	Unsatisfactory
0.2*H*	2 μF	0.98	0.95	0.88	Satisfactory
	3 μF	0.99	0.99	0.98	Satisfactory
	4 μF	0.90	0.97	0.99	Satisfactory
0.3*H*	2 μF	0.97	0.99	0.88	Unsatisfactory
	3 μF	0.99	0.97	0.97	Unsatisfactory
	4 μF	0.94	0.98	0.99	Satisfactory

THD regulation IEC61000-3-2 class C standard - 5th: 10%, 7th: 7%, 9th: 5%



(a) P_{loss}

(b) PF

Fig. 11. Measured P_{loss} and PF with respect to C_c for the source voltage from 94 V_{rms} to 106 V_{rms}.

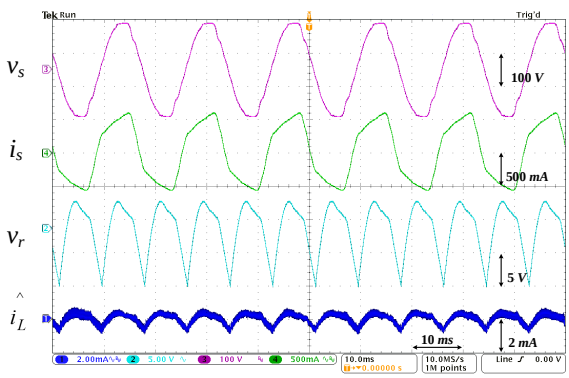


Fig. 12. Measured waveforms of the proposed LED driver to verify the line regulation capability for V_s = 100 V_{rms}.

line frequency is substantially decreased compared with that in a previous study [16].

This experiment also shows that the selected combination of L_c and C_c meets the THD regulation for source voltages from 94 V_{rms} to 106 V_{rms} as shown in Fig. 13. Excluding the power dissipation of the rapid-start ballast, the efficiency of the proposed boost converter-type LED driver was measured to be 88.5%, which is decent considering the hard switching.

The switching waveforms of MOSFET drain voltage v_x, inductor current i_{Li}, load voltage v_L, and LED current i_L were measured in μs as shown in Fig. 13; a large reverse recovery current appeared in i_{Li} as expected. The prototype of the proposed LED driver is shown in Fig. 15. The prototype is

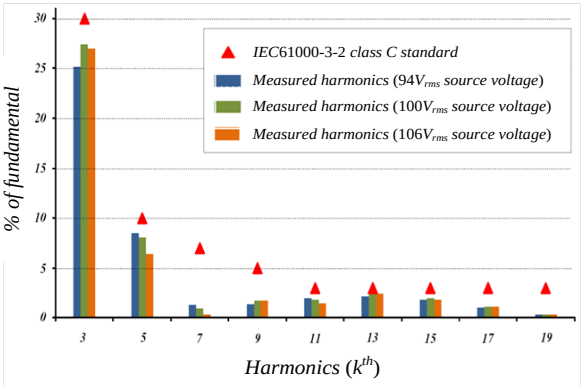


Fig. 13. Measured source side harmonic currents for the source voltage from 94 V_{rms} to 106 V_{rms}.

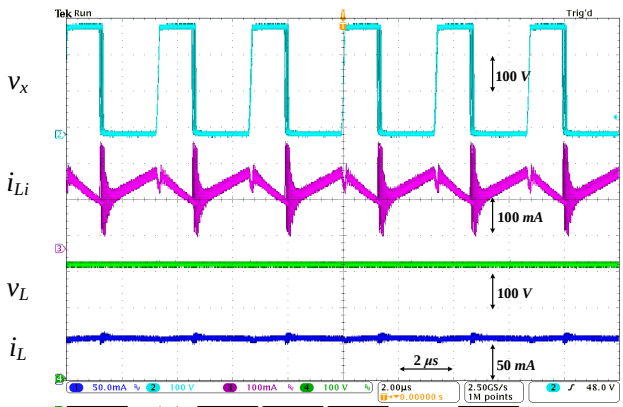


Fig. 14. Measured waveforms of the proposed LED driver for V_s = 100 V_{rms}.

TABLE III

MEASUREMENT RESULTS FOR PF AND EFFICIENCY

Parameters	Results for each source voltage		
	94 V_{rms}	100 V_{rm}	106 V_{rms}
I_L	61.7 mA	61.8 mA	61.7 mA
V_L	324 V	324 V	324 V
P_s	29.4 W	29.7 W	30.0 W
P_b	6.9 W	7.1 W	7.2 W
P_L	20.0 W	20.0 W	20.0 W
PF	0.999	0.983	0.939
Efficiency of the LED driver	88.9%	88.5%	87.7%

compact in size and inexpensive.

V. CONCLUSIONS

The proposed boost converter-type LED driver compatible with a rapid-start ballast was proven to be very stable with fairly high PF and low THD characteristics. The very complicated 10th order overall system was completely analyzed for static and dynamic characterizations through reasonably simplified models. A systematic design procedure was fully

established and verified by extensive simulations and experiments as having good agreement. The flicker percentage was successfully mitigated by the proposed fast feedback controller to as low as 1% even though a small DC capacitor was used. The experiments also showed that all the design requirements and standards were completely satisfied for source voltages from 94 V_{rms} to 106 V_{rms}.

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