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Topology Generation and Analysis of the No Dead Time AC/DC Converter

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Abstract

A novel topology generation method for the no dead-time three-phase AC/DC converter is proposed in this study. With this method, a series of no dead time topologies are generated and their operation principles are analyzed. The classic three-phase bridge AC/DC converter can realize a bidirectional operation. However, dead-time should be inserted in the driving signals to avoid the shoot-through problem, which would cause additional harmonics. Compared with the bridge topology, the proposed topologies lack the shoot-through problem. Thus, dead time can be avoided. All of the no dead time three-phase AC/DC converters can realize bidirectional operation. The operating principles of the converters are analyzed in detail, and the corresponding control strategies are discussed. Comparisons of waveform distortion and efficiency among the converters are provided. Finally, 9 KW DSP-based principle prototypes are established and tested. Simulation and experimental results verify the theoretical analysis.

Keywords: Bidirectional work, No dead time, Shoot-through problem, Three-phase AC–DC converter, Zero-crossing distortion

I. INTRODUCTION

With the development of industries, the demand for three-phase AC/DC converters is becoming more urgent. These converters can realize power conversion and power factor control and are widely applied in the field of wind power and electric vehicles [1]. Bridge topology is commonly utilized in three-phase AC/DC converters [2]. This topology can realize bidirectional operations and is easy to control. However, in each phase, the upper and lower power switches connect directly and may cause a shoot-through problem. Dead time must be inserted to the driving signals and additional harmonics should be introduced to increase the AC current THD and solve the abovementioned problem [3].

The harmonics caused by dead time can be reduced in two ways. One is through dead-time compensation [4], [5]. During the parameter search, the quality of the compensation is continuously assessed against the harmonic distortion of output currents. This method may complicate the control strategy of the converter. The other method is to improve the topology. If the topology does not have a shoot-through problem, dead time is unnecessary. Dual-buck topology is a no dead time topology originally applied to single-phase inverters [6]. When the driving signals of the upper and lower power switches are complementary, the two buck circuits work together. This condition can be defined as full-cycle control. In this case, a bias current flows through the power switches. The driving signals should be shielded for half of the grid cycle to eliminate the bias current; this condition is defined as half-cycle control [7]. However, half-cycle control would lead to zero-crossing distortion [8].

Three-phase dual-buck inverters have been discussed recently [9]. These inverters are suitable for direct current control in the *d-q* coordinate system and can obtain high PF (Power Factor). The dual-buck topology can also realize bidirectional operation. When the power flows from the AC side to the DC side, the converter operates as a rectifier and the topology can be viewed as dual-boost. For different power flowing directions, the half-cycle of the driving signals corresponds to different phase-sections of the grid voltage. The control strategy for the no dead time converter should also be considered to realize bidirectional operation.

For the abovementioned reasons, a topology generation method for no dead time three-phase AC/DC converters is proposed in this study. A series of no dead time topologies without the shoot-through problem is generated. All of the

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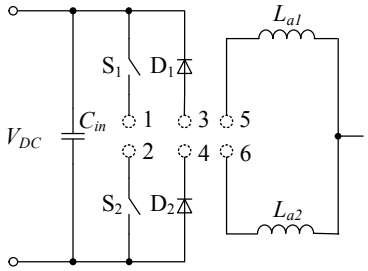


Fig. 1. No dead time structure of each phase.

topologies can realize bidirectional operation. The improved control strategies based on direct current control in the *d-q* coordinate system are applied to the no dead time topologies to obtain high efficiency and low THD. The topology generation method is described in Section II. The operating principle of the no dead time topologies is described in Section III. The control strategies and the comparison of the no dead time topologies are introduced in Section IV. The simulation and experimental results of 9 kW no dead time three-phase AC/DC converters are presented to verify the theoretical analysis in Section V.

II. Topology Generation Method

In the three-phase AC/DC converter, each phase arm has a similar operating principle. Thus, topology generation can consider only a single phase. The power switches of the upper and lower arm cannot connect directly to avoid the shoot-through problem. As shown in Fig. 1, inductors L_{a1} and L_{a2} have a filtering effect. The AC side filter inductor of the bridge topology can be replaced by L_{a1} and L_{a2}. Each phase contains power switches, freewheeling diodes, and filter inductors. Six ports exist for connection and combination: Ports 1 to 6. Among them, Ports 1 and 2 cannot connect directly. Two types of combinations exist for Ports 1 to 4. One is Port 1 connecting with Port 4 and Port 2 connecting with Port 3; this combination is defined as the 14/23 combination. The other is Port 1 connecting with Port 3 and Port 2 connecting with Port 4; this combination is defined as the 13/24 combination. The two newly generated ports can connect with Ports 5 and 6 directly or through power switching devices.

The 14/23 combination is equivalent to the topologies shown in Figs. 2(a) and 2(b). For this combination, the corresponding diode D_2 or D_1 freewheels after S_1 or S_2 is turned off. The current of inductance L_{a1} and L_{a2} would not mutate. Therefore, the two newly generated ports can not only connect with the inductance directly, but can also connect with the diode. Fig. 2(a) shows the dual-buck/boost topology. In Fig. 2(b), D_{aq} participates in the freewheeling of the inductors. It connects the two newly generated ports 14 and 23. Thus, the topology can be defined as self- loop.

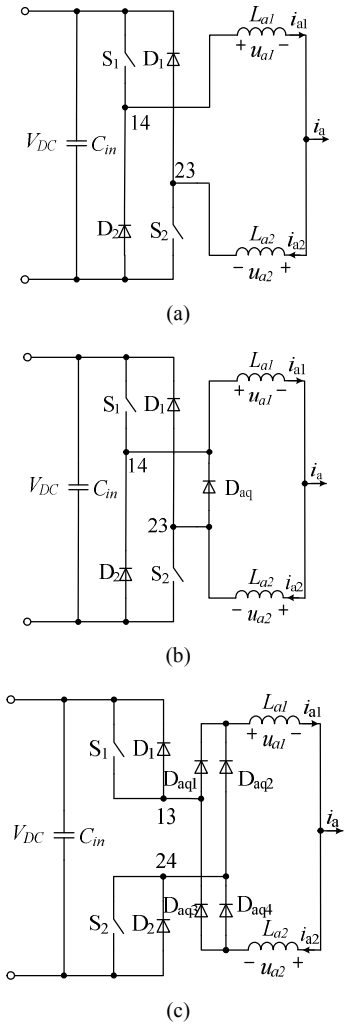


Fig. 2. Equivalent topology of the 14/23 and 13/24 combinations. (a) Dual-buck/boost topology. (b) Self-loop topology. (c) AC/DC topology with HFR.

The problem with the 13/24 combination is that no freewheeling diode exists after S_1 or S_2 is turned off. This condition may lead to a voltage spike during inductor current mutation. A current freewheeling branch should thus be constructed. The 13/24 combination is equivalent to the topology shown in Fig. 2(c). High-frequency rectifiers (HFR) connect with the output of the upper and lower arms. D_{aq1}–D_{aq4} form HFR. For example, after S_1 is turned off, L_{a1} freewheels through D_{aq2} to avoid the current mutation of the inductor. The reference direction of the current and voltage are shown in Fig. 2. Grid-side current i_a is the difference of inductor currents i_{a1} and i_{a2}. When the grid voltage is in the positive half cycle and i_a is larger than 0, the three types of converters operate as inverters. If i_a is lower than 0, the three kinds of converters operate as rectifiers. For the converter with HFR shown in Fig. 2(c), i_a being lower than 0 when i_{a1} is lower than i_{a2} is possible. All the topologies can realize bidirectional operation.

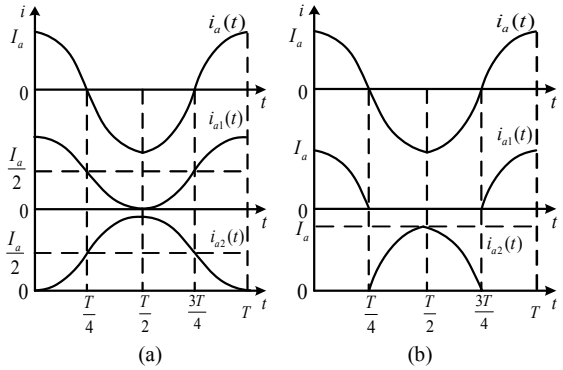


Fig. 3. Current waveforms of two situations. (a) Continuous inductor current. (b) Half-cycle inductor current.

III. OPERATING PRINCIPLE

A. Dual-buck/boost Topology

Two types of inductor currents exist for the dual-buck/boost topology. Under full-cycle control, the driving signals of S_1 and S_2 are complementary. Inductor currents that contain bias current always exist. Under half-cycle control, the driving signals of S_1 and S_2 are forced to be low for half of the grid cycle. The inductor currents would also last for half of the grid cycle. Fig. 3 presents the inductance current waveforms of the two situations.

The operation of the converter can be divided into two modes according to the direction of i_a. In mode 1, the direction of i_a is positive. In mode 2, the direction of i_a is negative. With mode 1 as an example, Fig. 4 presents the probable working condition of mode 1.

Bias currents exist under full-cycle control. As shown in Fig. 4(a), when S_1 is turned on, the current of L_{a2} freewheels through D_1, i_{a1} increases, and u_{a1} is positive. The potential of dot A is lower than that of dot P. Given that D_1 conducts to ensure the current path, the potential of dot A is also lower than that of dot F. At this time, u_{a2} is negative and i_{a2} decreases. When S_1 is turned off, the current of L_{a2} increases and flows through S_2. As shown in Fig. 4(b), the switching and conduction losses of S_2 cannot be avoided.

The current of L_{a2} is 0 under half-cycle control. Fig. 4(c) shows that when S_1 is turned on, the grid-side current equals i_{a1} and D_1 is turned off. When S_1 is turned off, S_2 is still turned off. Fig. 4(d) shows that no switching or conduction loss of S_2 is observed during this period. Therefore, half-cycle control can obtain higher efficiency than full-cycle control.

The operating principle of mode 2 is similar. In one grid cycle, the full-cycle controlled inductor current of L_{a1} and L_{a2} can be expressed as

$$\begin{aligned} i_{a1} &= \frac{I_a}{2}\cos\omega t + \frac{I_a}{2} \\ i_{a2} &= -\frac{I_a}{2}\cos\omega t + \frac{I_a}{2} \end{aligned} \quad . \tag{1}$$

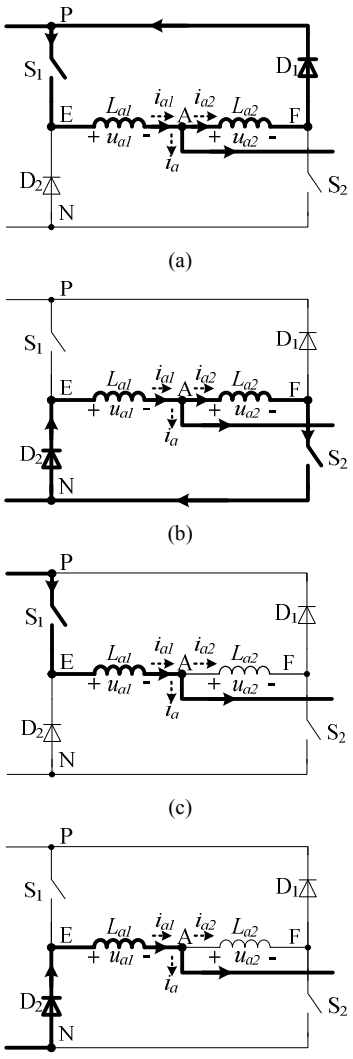


Fig. 4. Probable working condition of Mode 1. (a) S_1 on, S_2 off, and D_1 on. (b) S_1 off, S_2 on, and D_1 off. (c) S_1 on and S_2 off. (d) S_1 off, S_2 off, and D_1 off.

The half-cycle controlled inductor current of L_{a1} and L_{a2} can be expressed as

$$\begin{aligned} i_{a1} &= \begin{cases} I_a\cos\omega t & \text{(Mode 1)} \\ 0 & \text{(Mode 2)} \end{cases} \\ i_{a2} &= \begin{cases} 0 & \text{(Mode 1)} \\ I_a\cos\omega t & \text{(Mode 2)} \end{cases} \end{aligned} \quad . \tag{2}$$

B. Self-loop AC/DC Topology

The operation of the self-loop AC/DC converter can also be divided into two modes. Fig. 5 presents the operating modes of the self-loop converter.

The currents of L_{a1} and L_{a2} are always continuous because of D_{aq}. When S_1 is turned on similar to the full-cycle controlled dual-buck/boost converter, i_{a1} increases and i_{a2} decreases. This condition means that i_a also increases. When

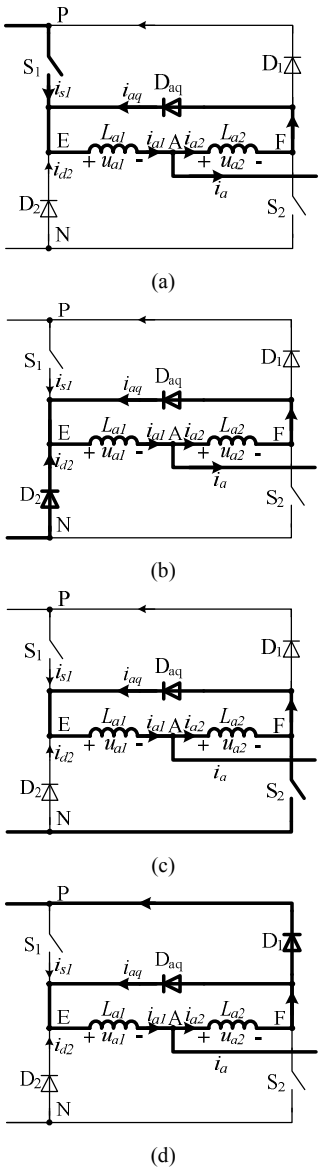


Fig. 5. Operating mode of the self-loop AC/DC converter. (a) S_1 on in mode 1. (b) S_1 off in mode 1. (c) S_2 on in mode 2. (d) S_2 off in mode 2.

S_1 is turned off, the current of L_{a2} still flows through D_{aq}. i_{a2} has no relationship with the switching state of S_2. Therefore, full-cycle control does not cause additional switching and conduction losses of S_2. However, additional conduction loss is caused by D_{aq}. The current of D_{aq} can be expressed as

$$\begin{cases} i_{aq} = i_{a2} = i_{a1} - i_{s1} & S_1ON \\ i_{aq} = i_{a2} = i_{a1} - i_{d2} & S_1OFF \end{cases} \quad (3)$$

where i_{s1} and i_{d2} are the current flow through S_1 and D_2, respectively. The difference between the self-loop AC/DC converter and the dual-buck/boost converter is that L_{a1}, L_{a2}, and D_{aq} of the self-loop topology can form a current loop. Although full-cycle control is applied, the current flow through S_1 and S_2 only lasts for half of the grid-cycle.

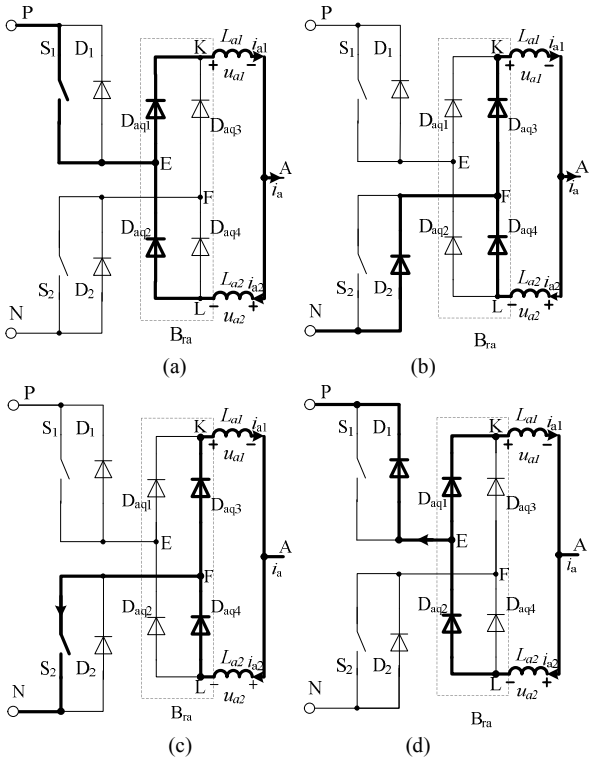


Fig. 6. Operating mode of the converter with HFR. (a) S_1 on in mode 1. (b) S_1 off in mode 1. (c) S_2 on in mode 2. (d) S_2 off in mode 2.

C. AC/DC Topology with HFR

Fig. 6 presents the operating modes of the converter with HFR. The operating principle is similar to that of the self-loop AC/DC converter. D_{aq1} to D_{aq4} are the HFR diodes. They form a loop with L_{a1} and L_{a2} instead of D_{aq}. Although no current flows through S_2 when S_1 is turned off and S_2 is turned on, the loss of HFR diodes is high.

IV. Control Strategies and Their Comparison

A. Control Strategies for the No Dead Time Converters

The SVPWM control strategy is widely used in three-phase AC/DC converters for its precise control of the AC side current and high DC voltage utilization. A three-phase dual-buck/boost converter requires half-cycle control to obtain high efficiency. The control method is shown in Fig. 7. The actual circuit utilizes an LCL filter in the AC side to inhibit high-frequency harmonics [10]. L_{a1}, L_{a2}, L_{b1}, L_{b2}, L_{c1}, and L_{c2} can be viewed as the converter-side inductors of the LCL filter. The part in the dashed box is half-cycle control. For full-cycle control, if the direction of active current set i_{qg}^* is changed, the converter would change between the rectifier and inverter to realize a bidirectional operation. For half-cycle control, the direction of i_{qg}^* and the half cycle shielding driving signals should both be changed.

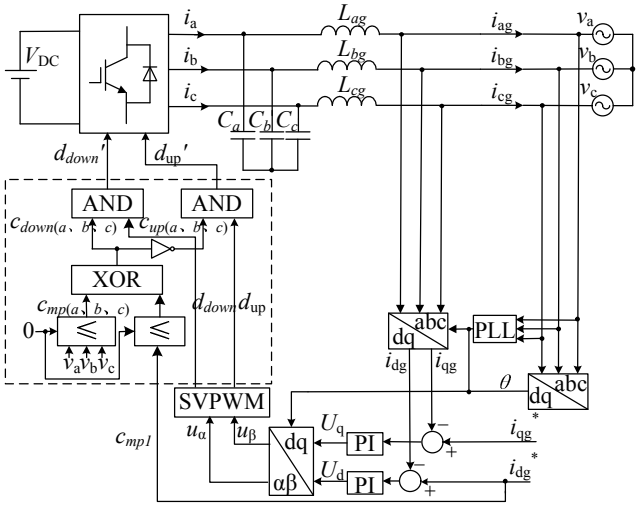


Fig. 7. SVPWM control method.

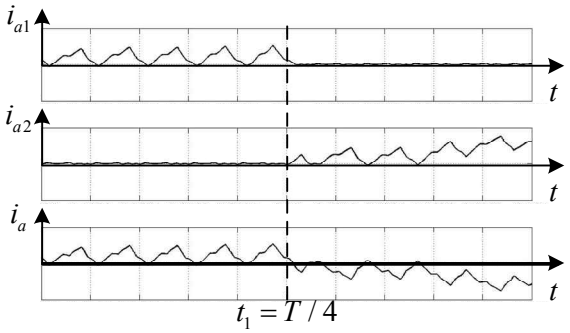


Fig. 8. High-frequency current ripple of inductance work switching.

With the arm of phase *a* as an example, i_{dg}^* is positive when the converter operates as an inverter. When $0 \le i_{dg}^*$, the comparison signal c_{mp1} is at a high level. When phase voltage v_a is positive, the inverter converter-side current i_{ac} is also positive. The drive signal of S_2 should be shielded. When $0 \le v_a$, comparison signal c_{mpa} is at a high level. For the XOR operation of c_{mpa} and c_{mp1}, the S_2 shielding signal c_{downa} is at a low level. The drive signal of S_2 is shielded after the AND operation with the drive signal of S_2. The S_1 shielding signal c_{up} is the NOT operation of c_{downa} and is at a high level. Thus, the drive signal of S_1 would not be shielded. When v_a is negative, c_{up} is at a low level and the drive signal of S_1 is shielded. When the converter operates as a rectifier, i_{dg}^* is negative. For $0 \ge i_{dg}^*$, c_{mp1} is at a low level. At this time, the shielding signal is opposite to the inverter mode.

However, a self-loop three-phase AC/DC converter and a three-phase AC/DC converter with HFR do not require half-cycle control. The control strategy can thus be simplified. The part in the dashed box can be left out. Except for no dead time, the strategy for the two types of converters is similar to that of a traditional three-phase bridge converter.

B. Comparison of the No Dead Time Converters

Half-cycle controlled dual-buck/boost converters can obtain high efficiency, but zero-crossing distortion is a serious problem. With time t_1 = T/4 as an example, the current of L_{a1} and L_{a2} switches at this time. Thus, the high-frequency current ripple of i_a changes suddenly from positive to negative. The process is shown in Fig. 8.

The current ripple of i_a can be expressed as

$$\Delta i_a = \frac{0.5(V_{DC} - e_a)D_s T_s}{L_{a1} + L_{ag}} \tag{4}$$

where D_s is the duty cycle. At the zero-crossing time of i_a, the equivalent modulation wave of SVPWM can be expressed as

$$u_{\mathrm{mod}} = \frac{V_{DC}}{2} + \frac{3}{4} M V_{DC} \sin(\omega_1 t + \frac{\pi}{2}) \cdot \tag{5}$$

At t_1 time, D_s equals 0.5 and e_a equals 0. Δi_a is high. Its effect on i_a cannot be ignored. Zero-crossing distortion is more serious in the half-cycle, SVPWM–controlled, three-phase dual-buck/boost converter than in the single-phase converter. SVPWM control requires coordinate transformation, and the three-phase currents influence each other. The current zero-crossing distortion of one phase would distort the other phases. Zero-crossing distortion thus reduces the quality of the current. The further improvement of the control strategy for the dual-buck/boost converter should also be considered.

Full-cycle controlled dual-buck/boost converters, self-loop AC/DC converters, and AC/DC converters with HFR do not exhibit zero-crossing distortion. However, additional losses may reduce the efficiency of the converters. Four types of losses exist: conduction loss of IGBT, conduction loss of the diode [11], switching loss of IGBT, and reverse recovery loss of the diode [12].

The mathematical model of IGBT and the diode can be expressed as

$$U_{tv} = \frac{U_{ron} - U_{on}}{I_N} * I_{con} + U_{on} \tag{6}$$

where U_{tv} is the terminal voltage, U_{ron} is the voltage drop at rated current I_N, U_{on} is the voltage drop at light load, and I_{con} is the actual current of the power device. The conduction loss of IGBT and the diode can thus be expressed as

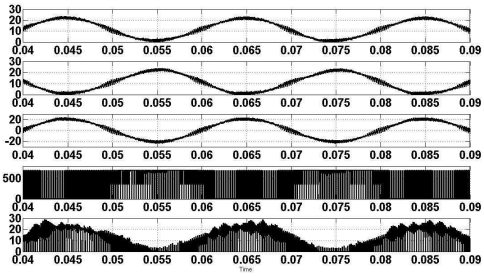
$$P_{cl} = \frac{1}{T}\int_0^T (\frac{U_{ron} - U_{on}}{I_N} {I_{con}}^2 D_s + U_{on} I_{con} D_s) dt \cdot \tag{7}$$

The switching loss of IGBT can be expressed as

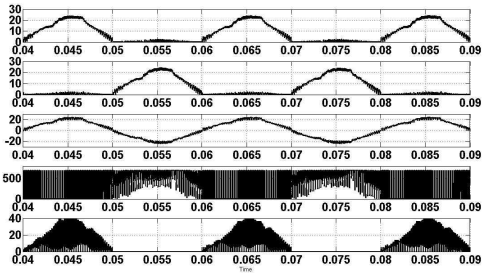
$$P_{sw} = (E_{sw(on)} + E_{sw(off)}) f_s * \frac{2}{T I_a} \int_0^{T/2} I_{con} dt \tag{8}$$

where $E_{sw(on)}$ and $E_{sw(off)}$ are the turn-on and turn-off losses at a rated current, respectively. These values can be obtained from the datasheet. Reverse recovery loss can be expressed as

$$P_{rec} = E_{rec} f_s * \frac{2}{T I_a} \int_0^{T/2} I_{con} dt \cdot \tag{9}$$



(a)



(b)

Fig. 9. Key waveforms of the dual-buck/boost AC/DC converter. (a) Full-cycle control. (b) Half-cycle control.

With mode 1 of the three topologies as an example, for the half-cycle controlled dual-buck/boost converter, S_2 does not turn on and no additional conduction or switching loss of S_2 occurs when S_1 is turned off. For the full-cycle controlled dual-buck/boost converter, S_2 turns on and an additional conduction or switching loss of S_2 occurs when S_1 is turned off. For the self-loop AC/DC converter, when S_1 is turned off and regardless of S_2 being turned on, no additional conduction or switching loss of S_2 occurs. However, an additional conduction loss of D_{aq} occurs. For the AC/DC converter with HFR, additional conduction and reverse recovery losses of D_{aq1} to D_{aq4} occur.

V. Simulation and Experimental Results

The three types of no dead time, three-phase, AC/DC converters are simulated with the simulation software MATLAB/Simulink to verify the theoretical analysis. The DC-link voltage is 700 V, and the AC side is connected with a 220/380 V/50 Hz three-phase grid. For the inverter operation, the given active power P is 9 kW and reactive power Q is 0. For the rectifier operation, the given active power P is -9 kW and reactive power Q is 0.

Fig. 9 presents the simulation result of the dual-buck/boost AC/DC converter. The waveforms are inductance currents i_{a1} and i_{a2}, AC current i_a, voltage of S_1, and current of S_1. Fig. 9(a) corresponds to full-cycle control. i_{a1} and i_{a2} have a DC bias, and the current flow through S_1 lasts for the full grid cycle; thus, high switching and conduction losses would occur. Fig. 9(b) corresponds to half-cycle control. The driving signals only last for half of the grid cycle. Thus, the current of S_1 lasts for half of the grid cycle. Zero-crossing distortion occurs. Moreover, given the three-phase coordinate transformation, one phase distortion would affect the other two phases and would exacerbate the distortion.

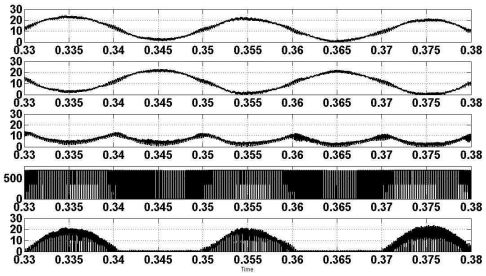
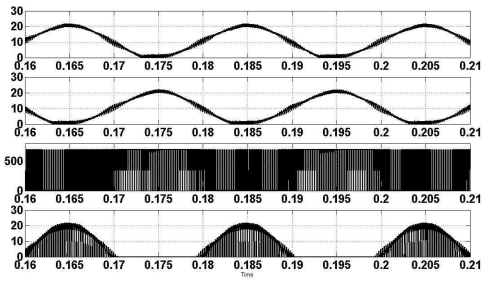
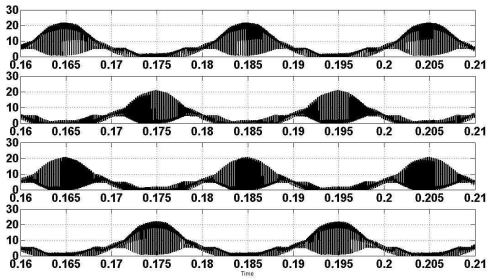


Fig. 10. Key waveforms of the self-loop AC/DC converter.



(a)



(b)

Fig. 11. Key waveforms of the AC/DC converter with HFR. (a) Waveforms of the inductance and power switch. (b) Waveforms of the HFR diodes.

Fig. 10 presents the simulation result of the self-loop AC/DC converter. The waveforms are inductance currents i_{a1} and i_{a2}, current of diode D_{aq}, voltage of S_1, and current of S_1. Regardless of full-cycle or half-cycle control, the current of S_1 only lasts for half of the grid cycle and the current of L_{a1} and L_{a2} are continuous. Zero-crossing distortion can thus be avoided. The current flow through D_{aq} causes conduction loss, which would reduce the converter efficiency. However, the current value and the loss are low.

Fig. 11 presents the simulation result of the AC/DC converter with HFR. The waveforms in Fig. 11(a) are inductance currents i_{a1} and i_{a2}, voltage of S_1, and current of S_1. i_{a1} and i_{a2} have a DC bias, but the current of S_1 only lasts for half of the grid cycle. The switching and conduction losses of

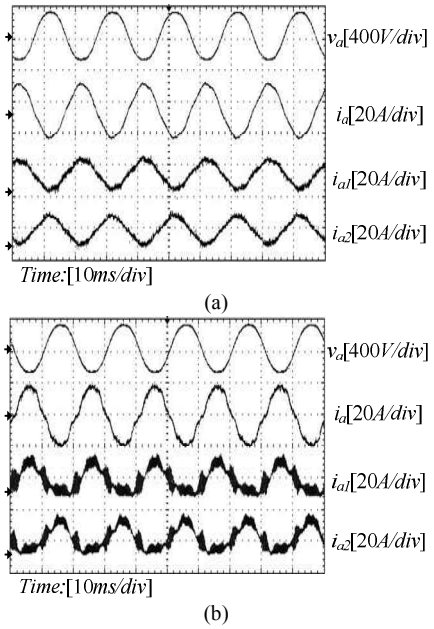


Fig. 12. Experimental results of the dual-buck/boost AC/DC converter. (a) Full-cycle control. (b) Half-cycle control.

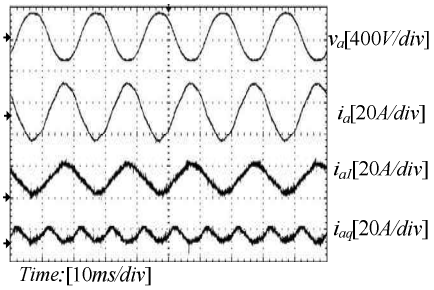


Fig. 13. Experimental results of the self-loop AC/DC converter.

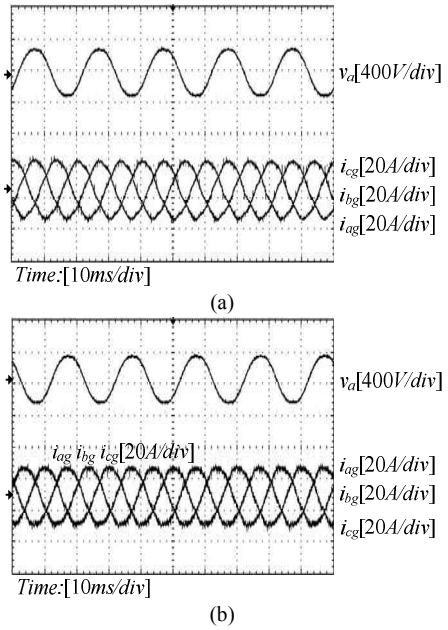


Fig. 14. AC side voltage and current. (a) Traditional bridge converter. (b) Self-loop converter.

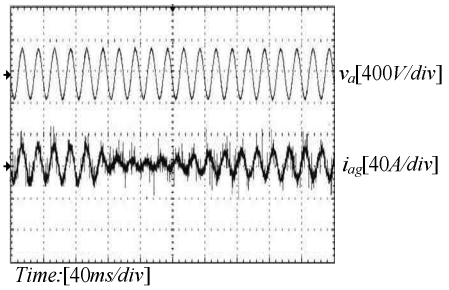


Fig. 15. Bidirectional operation waveform.

S_1 caused by a redundant driving signal can be avoided. However, additional conduction loss in the HFR diodes is inevitable. In Fig. 11(b), the waveforms are the currents of HFR diodes D_{aq1} to D_{aq4}. i_{a1} is the sum of the current flow through D_{aq1} and D_{aq3}. i_{a2} is the sum of the current flow through D_{aq2} and D_{aq4}. The current causes a high conduction loss of D_{aq1} to D_{aq4}.

Compared with the self-loop three-phase AC/DC converter, the AC/DC converter with HFR has more power devices and exhibits higher power loss. The advantages of these two converters are similar. Hence, the 9 kW self-loop AC/DC converter and the dual-buck/boost AC/DC converter are built to verify the analysis with the same parameters as in the simulation. A 9 kW traditional-bridge three-phase converter is also built for the comparison.

Fig. 12 presents the experimental results of the full-cycle and half-cycle controlled dual buck/boost AC/DC converter in terms of rectifier operation. The waveforms are grid voltage, AC-side current, and inductance currents i_{a1} and i_{a2}. The waveform quality of full-cycle control is much higher than that of half-cycle control. Fig. 13 presents the experimental results of the self-loop AC/DC converter in terms of rectifier operation. The waveforms are grid voltage, AC-side current, inductance current i_{a1}, and the current of diode D_{aq}. These waveforms are consistent with those in the simulation results.

Fig. 14 presents the voltage and current of traditional-bridge and self-loop converters when they operate as inverters. Table I presents the comparison data of these topologies. The efficiency of the self-loop AC/DC converter is higher than that of the full-cycle controlled dual-buck/boost AC/DC converter because the conduction loss of the diodes is lower than the switching and conduction losses of the power switches. The THD of the self-loop AC/DC converter is lower than that of the half-cycle controlled dual-buck/boost AC/DC converter because no zero-crossing distortion occurred in the former.

Fig. 15 shows the bidirectional operation of the self-loop three-phase converter. The current should be controlled to change gradually to avoid current impact. When the converter changes from rectifier to inverter, no current rush occurs and the response time is short.

TABLE I
COMPARISON OF EFFICIENCY AND THD

	Efficiency (%)	THD (%)
Traditional-bridge AC/DC converter	98.35	6.0
Full-cycle controlled dual-buck/boost AC/DC converter	94.38	3.2
Half-cycle controlled dual-buck/boost AC/DC converter	98.41	7.9
Self-loop AC/DC converter	98.26	3.1

VI. CONCLUSIONS

A topology generation method for the no dead zone AC/DC converter was developed in this study. Three topologies, including a dual-buck/boost converter, were generated. No shoot-through problem was observed in the converters, and bidirectional operation was realized. The low-frequency harmonics and the filter specifications can be reduced. The proposed no dead time converters have the following characteristics.

1) The dual-buck/boost converter requires half-cycle control to achieve high efficiency. The reverse recovery loss of the external diodes in this converter is less than that of the integrated diodes in the classic bridge converter. However, zero-crossing distortion may reduce the THD of the half-cycle controlled dual-buck/boost converter.
2) The self-loop AC/DC converter does not require half-cycle control and has no zero-crossing distortion. However, the additional diodes cause additional loss, and the efficiency of this converter may be less than that of the half-cycle controlled dual-buck/boost converter. The self-loop AC/DC converter has one more diode than the classic bridge converter; nevertheless, their efficiencies have minimal difference.
3) The AC/DC converter with HFR also does not require half-cycle control. However, the number of additional diodes is more than that in the self-loop AC/DC converter. The efficiency of the AC/DC converter with HFR is low.

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