JPE 14-2-8

http://dx.doi.org/10.6113/JPE.2014.14.2.271
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Wind Energy Interface to Grid with Load Compensation by Diode Clamped Multilevel Inverters

Paulson Samuel*, M. Kishore Naik**, Rajesh Gupta†, and Dinesh Chandra*

*†Department of Electrical Eng., Motilal Nehru National Institute of Technology, Allahabad, India
**Depatment of Industrial Eng., University of Padua, Padua, Italy

Abstract

Fluctuating wind conditions necessitate the use of a variable speed wind turbine (VSWT) with a AC/DC/AC converter scheme in order to harvest the maximum power from the wind and to decouple the synchronous generator voltage and frequency from the grid voltage and frequency. In this paper, a combination of a three phase diode bridge rectifier (DBR) and a modified topology of the diode clamped multilevel inverter (DCMLI) has been considered as an AC/DC/AC converter. A control strategy has been proposed for the DCMLI to achieve the objective of grid interface of a wind power system together with local load compensation. A novel fixed frequency current control method is proposed for the DCMLI based on the level shifted multi carrier PWM for achieving the required control objectives with equal and uniform switching frequency operation for better control and thermal management with the modified DCMLI. The condition of the controller gain is derived to ensure the operation of the DCMLI at the fixed frequency of the carrier. The converter current injected into the distribution grid is controlled in accordance with the wind power availability. In addition, load compensation is performed as an added facility in order to free the source currents being fed from the grid of harmonic distortion, unbalance and a low power factor even though the load may be unbalanced, non-linear and of a poor power factor. The results are validated using PSCAD/EMTDC simulation studies.

Key words: Diode clamped multilevel inverter (DCMLI), Fixed switching frequency current control, Level shifted multi-carrier PWM, Wind turbine

I. INTRODUCTION

The proportion of distributed generation (DG) in modern electric power systems is steadily increasing in several countries. Wind generation is a renewable source and it is an important component of DG which has traditionally been used for energy conversion and is more recently being harnessed for grid support functions as well [1]. Different classes of power converters have been proposed for the integration of renewable energy resources into the distribution grid [2]. Multilevel inverters have been the preferred option for the high power applications in industrial drives for many years and more recently in wind power generation systems due to the fact that they can transfer high power using matured power semiconductor technology with reduced voltage stress on semiconductor switches, better waveforms and a lower THD.

The major problems faced by wind generation systems in general are variations in available power due to varying wind speeds and variations in the frequency and voltage of the generator output when synchronous generators are used with variable speed wind turbines (VSWT). To address these problems, an AC/DC/AC system is used to decouple the generator frequency and voltage from the grid frequency and voltage. In this system the power output of the synchronous generator is first rectified to DC and then a DC-AC power converter interfaces with the grid with a constant voltage and frequency operation. Thus, there are two converters in use in such a scheme; a machine side converter which converts the AC to DC and a grid side converter which interfaces with the grid at an appropriate frequency and voltage. In addition, it

Manuscript received Dec. 1, 2012; accepted Aug. 18, 2013
Recommended for publication by Associate Editor Yongsug Suh.
†Corresponding Author: rajeshgupta310@rediffmail.com
Tel: +91-532-2271416, Fax: +91-532-2545341, Motilal Nehru National Institute of Technology
*Dept. of Electrical Eng., Motilal Nehru National Institute of Technology, India
**Dept. of Industrial Eng., University of Padua, Italy

provides all of the needed grid support functions. For high power wind generation systems involving either a single high power wind generator or a pool of power available from a wind farm, the rating of the converter should match the maximum power transferred from the wind generation system. In this paper a three phase diode bridge rectifier (DBR) is used as a machine side converter, which is readily available in the range of the required high power ratings. However, the major problem lies with a grid side converter that requires controllable switches having large voltage and power ratings. In this paper a diode clamped multilevel inverter (DCMLI) has been considered as the grid side converter. The DCMLI is operated as a voltage source inverter (VSI) in the current control (CC) mode in order to inject a current according to the maximum available power from the wind turbine under the prevalent wind conditions. It also provides load compensation for local loads at the point of common coupling (PCC). The added duty of providing local load compensation necessitates a converter rating that is larger than the generator. Depending upon the rating of the DCMLI, it is capable of partly or fully compensating the load currents so that the source (grid) currents drawn are pure sinusoids, balanced and in phase with the PCC voltages.

Although there are three topologies for multi-level inverters, the DCMLI has an edge over the others for wind turbine applications since it requires only one DC source which matches with the fact that a three phase diode bridge rectifier connected to a synchronous generator yields only one isolated DC source. The DCMLI has a simple construction and the modified DCMLI [3] has the added advantage of a reduced number of blocking diodes. However, the usual problem of voltage balancing between the capacitors has to be addressed in order to maintain the stable operation of a DCMLI, for which two methods have been suggested [4], [5]. These are the external balancing circuits and special PWM techniques which have their own advantages/disadvantages such as added cost for the former and increased control complexity and difficulty of control for certain operating conditions for the latter.

There are several current control methods for inverters. The hysteresis control of power converters has been very popular since it has good dynamic characteristics and easier implementation for two-level inverter [6]. However, this method suffers from the problems of variable and unequal switching frequencies for different switches in a VSI. This leads to the problem of unequal charging/discharging and unbalancing of the dc link capacitors, when extended for multilevel converter control [7]. To overcome the problem of variable and unequal switching frequencies, the ramp-comparison modulation scheme of two level inverters has great potential for the control of the multilevel inverters [8], due to its property of a constant switching frequency which is decided by the triangular carrier frequency.

A control strategy has been proposed in this paper for the modified topology DCMLI with a reduced number of diodes for achieving the objective of the grid interface of wind power systems together with local load compensation. A novel fixed frequency current control method is proposed based on level shifted multi carrier PWM modulation for achieving the required control objectives with equal and uniform switching frequency operation. The condition for ensuring that constant frequency operation is maintained at all times has been derived for the proposed modulation method. The inverter power output to the grid is regulated to match the available power at the wind turbine, in order to evacuate the power available from the wind turbine as per the wind conditions.

II. Speed and Power Relations of a Wind Turbine

The kinetic energy in the air moving at the speed V_W is given by the following equation:

$$W = \frac{1}{2}\rho A V_W^3 \tag{1}$$

where, ρ is the air density and A is the rotor area swept by the turbine blades. The mechanical power delivered by a wind turbine is expressed as:

$$P_{turbine} = \frac{1}{2}\rho A C_p V_W^3 \tag{2}$$

where, C_p is the power coefficient defined as the ratio of the turbine power to the available wind power. The power coefficient is a function of the pitch angle β and the tip speed ratio λ which is defined as the ratio of the turbine speed at the tip of the blade to the wind speed V_W, which is given by (3).

$$\lambda = \frac{\omega R}{V_W} \tag{3}$$

where, ω is the turbine angular speed and R is the turbine rotor radius. The turbine power coefficient C_p, is a function of the tip-speed ratio λ, and for a fixed pitch angle β, peaks at a certain value of the rotor speed for a given value of wind speed. Hence, the objective of the power controller is to operate the turbine at an optimal rotor speed for the prevalent wind speed. The mechanical torque of the wind turbine is expressed as:

$$T_{mech} = \frac{P_{turbine}}{\omega}. \tag{4}$$

The electrical power output from the generator is given by:

$$P_{gen} = P_{turbine}\eta_{gen}\eta_{gear} \tag{5}$$

Where η_{gen} and η_{gear} are the generator and gear efficiencies.

III. Wind Energy Interface to the Grid Using a VSI in the Current Control Mode

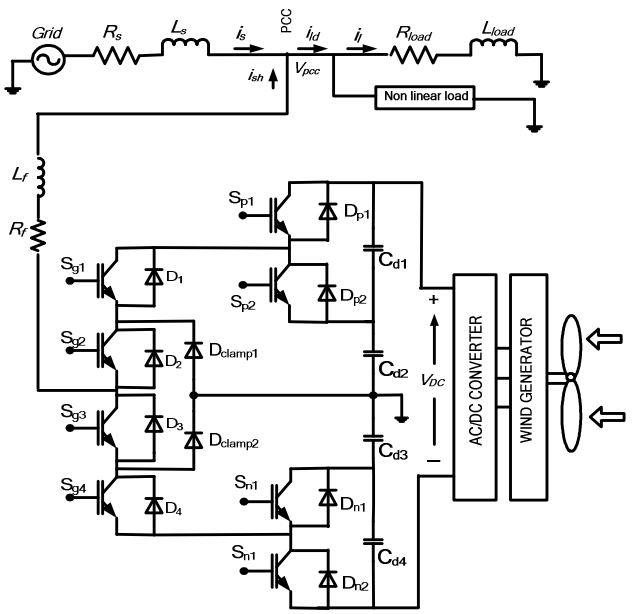


Fig. 1. Block diagram (shown only for single phase) of the wind generation system connected to grid through a modified DCMLI.

A VSI is capable of operating in either voltage or current control mode. If one is used in current control mode it can also compensate the load currents so that the source currents are sinusoidal, balanced and have the specified phase angle with respect to the PCC voltage, which improves the power factor at the PCC, irrespective of unbalancing, a low power factor and harmonic distortion of the load currents [9]. The dc link of the VSI is fed from the output of the uncontrolled diode bridge rectifier connected to the synchronous generator.

Fig. 1 shows the proposed wind generation system interfaced with the grid through a modified DCMLI [3]. It is assumed that the load is reactive, which deteriorates the power factor and has harmonic components due to the presence of nonlinear loads and/or may be unbalanced. The output terminal voltage of the synchronous generator usually has a variable magnitude and frequency due to wind speed variations. However, in the present case the terminal voltage is held constant due to the excitation controller which keeps the dc link voltage constant over the normal speed and load range. The VSI is required to inject current according to the available wind power and provide the required compensation at the PCC.

As the power levels of individual wind turbines increase and cross into the multi-megawatt range, the converter technology also needs to be improved to handle the increased thermal stress. It is becoming increasingly clear that the current practice of having low voltage two level converters and then stepping up the voltage in order to interface with medium voltage (MV) grids will not suffice. MV inverters are fast emerging alternatives and have been around in drives applications for several years. Instead of using several devices in series and parallel to handle the increased voltage and current stress, multi level converters offer the advantages of reductions in voltage stress, THD and current stress at medium voltage for the same power. For medium voltage distribution systems, it is desired that multi-level inverters (MLI) be used as grid side converters since they offer the promise of interfacing wind energy conversion systems (WECS) directly to the grid without the bulky and costly transformers which are being placed at the tower bases in current designs. As pointed out earlier in this paper, because of its advantages over the other topologies for wind energy conversion systems (WECS), a DCMLI has been used in this paper for grid connection of the wind turbine generator.

The DCMLI injects current in such a way that the harmonics and reactive power component of the current are supplied by the shunt connected DCMLI thus relieving the grid of the need to supply these components. As a result the grid current drawn is sinusoidal and balanced and in phase with the PCC voltage. In low wind conditions the main ac source, i.e., the grid, supplies the bulk of the power required by the load and a small part of the load power may be supplied by the wind turbine. When the wind power availability is good the operating strategy is to inject as much of the wind power as possible to the PCC, so that all or a major component of the load is supplied by wind power and the import from the grid is reduced. Thus, the DCMLI controls the power flow according to the wind power availability so as to inject the maximum amount of power into the PCC. During times when the load is more than the capacity of the wind generator, the load can be shared by both the turbine and the main source (grid).

IV. Capacitor Voltage Balancing Strategy

One of the major problems associated with all diode-clamped multilevel inverters having more than three levels is the unbalancing of the DC link capacitor voltages under the steady state. It is difficult to ensure voltage balancing of the DC link capacitors under all operating conditions including high modulation indices and large power factors, which greatly limit the practical applications of the DCMLI. The DC link capacitor voltage unbalancing is termed as the divergence of the capacitor voltages. This results in voltage collapse across some of the capacitors and voltage rise across others due to the non uniform power drawn from the DC link capacitors. As a result, the output voltage waveform quality deteriorates as the number of levels is reduced and the voltage ratings of the components are at risk of being exceeded resulting in a converter trip and operational disruption. Simulation results showing the collapse of the five-level output of a five-level DCMLI to three levels is shown in Fig. 2.

This shows how the inner levels of the five-level voltage waveform get collapsed and the outer levels increase thus

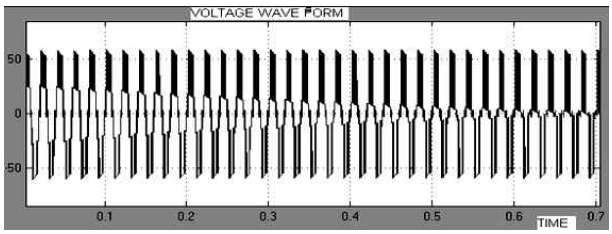


Fig. 2. Output voltage of a DCMLI showing the collapse of the voltage levels.

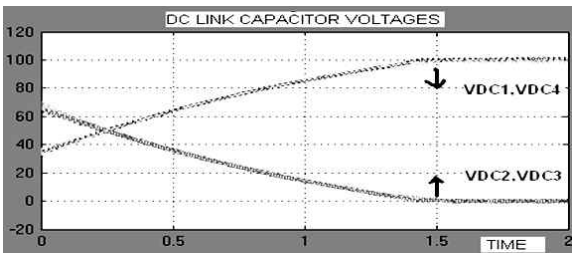


Fig. 3. Divergence of capacitor voltages in DCMLI.

finally resulting in three-levels. This occurs within a few cycles in the absence of any control. Fig. 3 shows the divergence of the capacitor voltages with respect to time. The two existing solutions for the voltage balancing problem for the DCMLI are as follows.

1) Installation of a voltage balancing circuit on the DC side of the inverter [10], [11].
2) Modifying the converter switching pattern according to the control strategy [12], [13], for self-balancing of the voltages.

The later is preferred in terms of cost as the former requires additional hardware, which adds to the system cost and complexity. For applications involving only reactive power exchange, the switching pattern modification strategies can be used for the voltage balancing problem [14], [15]. However, the voltage self-balancing can influence the reactive power control if priority is given only to the balancing problem [16]. Moreover, switching pattern modifications cannot always be used to control the capacitor voltages as it is mainly effective at low modulation indices. Furthermore, medium and high voltage power converters intended for installation to a utility grid, require more reliable and robust operation against line faults and transients. It should also be noted that for back-to-back converter applications, the switching modification strategy requires the two converters to operate at a fixed ac voltage ratio for capacitor voltages equalization. Therefore, extra balancing circuits [17] have been used for the capacitor voltage balancing in this paper.

Fig. 4 shows the external balancing circuit for balancing the capacitor voltages.

The balancing circuit shown in Fig. 4, works on the principle of transferring energy from an overcharged capacitor to an undercharged one through an energy storing

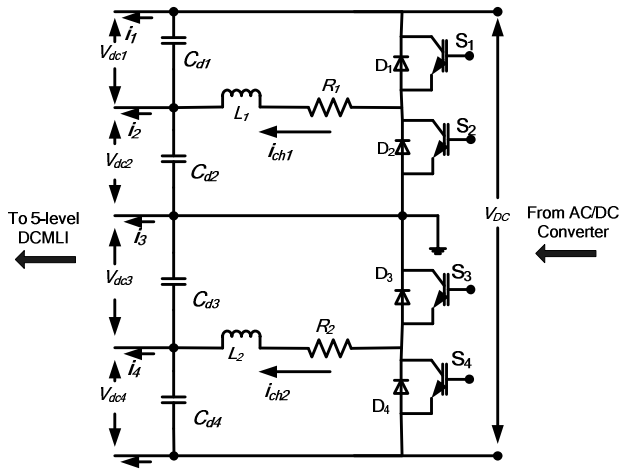


Fig. 4. External balancing circuit for capacitor voltages.

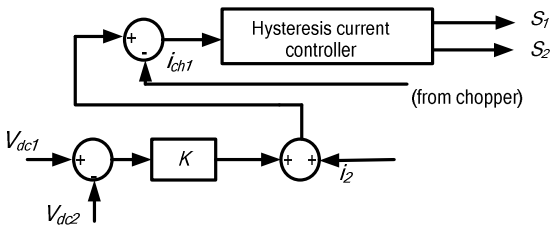


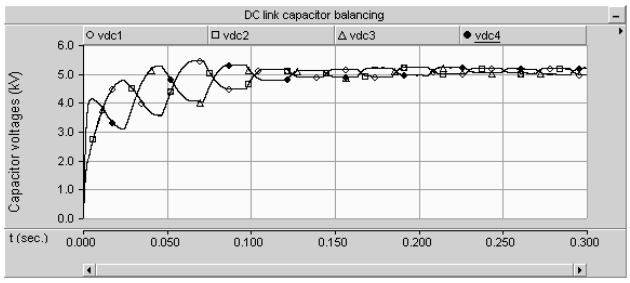
Fig. 5.Hysteresis current control for capacitor voltage balancing.

inductor. In this way, the capacitor voltages at the DC link are equalized. Though the utilization of these additional balancing circuits improves the operation of multilevel inverters, the devices in these circuits have to handle high currents and voltages which may be even higher than the ratings of the devices used in the main converter.

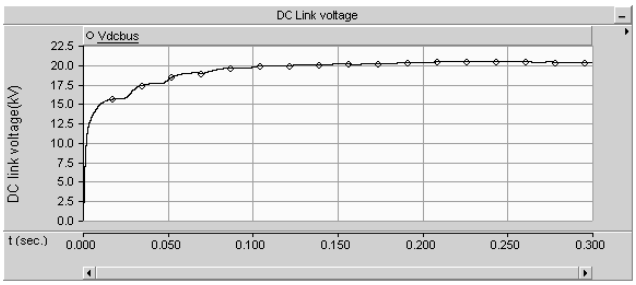
In Fig. 4, inductor L_1 in the upper part of the circuit is used to exchange the energy between capacitors C_{d1} and C_{d2}, using switches S_1, S_2 and diodes D_1, D_2. Similarly, inductor L_2 in the lower part of the circuit exchanges the energy between capacitors C_{d3} and C_{d4} using switches S_3, S_4 and diodes D_3, D_4. The charge transfer in the balancing circuit is bidirectional in nature through the anti-parallel diodes. Therefore, this circuit could be more useful to restore voltage balancing under transient conditions. Furthermore, most of the power semiconductor switches have built in anti-parallel diodes.

A control block diagram of the hysteresis band chopper current control for the capacitor voltage control is shown in Fig. 5. This control scheme has fast dynamics due to the chopper current feedback. For controlling V_{dc1} and V_{dc2}, current i_2 is sensed and filtered to get the average value of current i_2. The corresponding capacitor voltages (V_{dc1} and V_{dc2}) are also measured and filtered to eliminate the ripples.

The difference of the average capacitor voltages (ΔV_{dc}= V_{dc1} - V_{dc2}) is passed through the proportional voltage controller gain K, which is then added to the average current



(a)



(b)

Fig. 6. (a)Balancing of capacitor voltages with balancing circuit. (b) DC link voltage buildup.

i_2 to generate the reference chopper current, $i_{ch1\ ref}$. In this control scheme, the chopper circuit is employed to track $i_{ch1\ ref}$ in a hysteresis band. This control scheme nullifies the voltage drift due to the non-zero average values of i_2 and i_4 as well as the initial voltage imbalance in the capacitors by using the proportional gain multiplied average voltage errors. To obtain the control signals for S_3 and S_4 switches in Fig. 4, an additional hysteresis controller is required. The controller response is simulated in Fig. 6. It can be seen that the capacitor voltages are balanced within a few cycles.

V. Modeling and Control of a DCMLI Using the Proposed Fixed Switching Frequency Current Control Method

A. Proposed Control Scheme for DCMLI

A *n*-level DCMLI helps in reducing the device voltage stress by a factor of 2/(*n*-1) times the required net DC link voltage. The total number of semiconductor switches required per phase is 2(*n*-1). However, the total number of clamping diodes is 2 for a 5 level modified DCMLI compared with the 12 diodes required per phase for a conventional DCMLI [3].

The use of level shifted unipolar PWM results in the harmonic spectrum of the output voltage to lie at the carrier frequency and the sidebands are shifted from this center in multiples of the fundamental frequency [18]. The switching harmonics amplitude is also reduced by a factor of 1/(*n*-1) in the output voltage. The ripples are thus reduced to a great extent and smooth modulation is possible at a fixed switching frequency. For a *n*-level DCMLI, (*n*-1) carriers are required which are in phase but level shifted by an appropriate value.

The carrier frequency used in this paper is 5.0 kHz. Hence, on average each switch operates at 5.0 kHz/(*n*-1) = 1.25 kHz for $n = 5$.

In this paper a fixed switching frequency current control method based on the multi-carrier level shifted PWM modulation method has been proposed to control the modified DCMLI in order to track a desired shunt current to be injected into the PCC. Fig. 7 shows the modulation method proposed in detail for one phase of the DCMLI. The four level shifted carriers are: Carrier 1 with an upper limit of $+2A_c$ and a lower limit of $+A_c$, Carrier 2 with an upper limit of $+A_c$ and a lower limit of 0, Carrier 3 with an upper limit of 0 and a lower limit of $-A_c$, and Carrier 4 with an upper limit of $-A_c$ and a lower limit of $-2A_c$. The switching logic is explained below.

With reference to Fig. 1 and Fig. 7, the following control algorithm is proposed.

1) S_e is compared with a level shifted positive maximum triangular carrier 1 with peak: A_c and $2A_c$.
   If $+2A_c > S_e$ then S_{p1} is ON and S_{p2} is OFF
   If $+2A_c < S_e$ then S_{p2} is ON and S_{p1} is OFF
2) S_e is compared with a level shifted positive minimum triangular carrier 2 with peak: 0 and A_c.
   If $+A_c > S_e$ then S_{g1} is ON and S_{g3} is OFF
   If $+A_c < S_e$ then S_{g3} is ON and S_{g1} is OFF
3) S_e compared with a level shifted negative minimum triangular carrier 3 with peak: 0 and $-A_c$.
   If $-A_c > S_e$ then S_{g2} is ON and S_{g4} is OFF
   If $-A_c < S_e$ then S_{g4} is ON and S_{g2} is OFF
4) S_e compared with a level shifted negative maximum triangular carrier 4 with peak: $-A_c$ and $-2A_c$.
   If $-2A_c > S_e$ then S_{n1} is ON and S_{n2} is OFF
   If $-2A_c < S_e$ then S_{n2} is ON and S_{n1} is OFF

where, S_e is the switching function obtained after multiplying the current error e with the gain K. For the other phases the references are shifted by 120˚ and 240˚. With sine-triangle PWM, the semi conductor switches operate at the frequency of the triangular carrier and produce well-defined harmonics [6]. Multiple crossings of the switching function with the triangular carrier may become a problem when the time rate of change for the switching function becomes greater than that for the slope of the carrier.

B. System Modeling

A block diagram of the per phase equivalent of a weak distribution system with the shunt connected WECS of Fig. 1 and with the DCMLI using the proposed current control mode is shown in Fig. 8.

The nominal linear load is represented by R_{load} and L_{load}. The grid is represented by the voltage source v_s, and the equivalent Thevenin impedance (which includes the source and feeder impedances) is represented by R_s and L_s. The shunt impedance is represented by R_f and L_f and includes

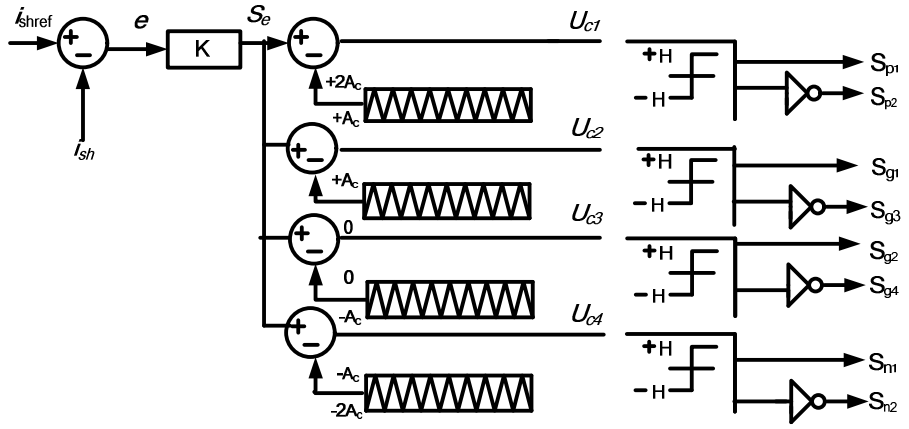


Fig. 7. Fixed switching frequency current control method for one phase of the DCMLI.

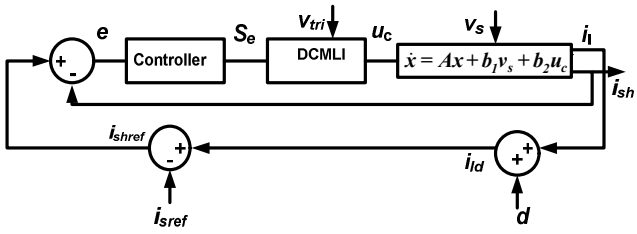


Fig. 8. Model of the weak distribution system with shunt connected WECS using DCMLI in current control mode.

the impedance of the cable/line connecting the VSI to the PCC. The PCC voltage is denoted by v_{pcc}. The DCMLI, which works as a VSI, outputs a voltage whose magnitude is $u_c V_{dc}$, where u_c = -1, -1/2, 0, +1/2, +1, for a five level DCMLI. The current control loop of the VSI can be modeled as discussed below [19]. Choosing a state vector as $x = [i_{sh} \quad i_l]^T$, the following state space equation can be obtained.

$$L_{eq}\dot{x} = Ax + b_1 v_s + b_2 u_c \tag{6}$$

where, $L_{eq} = L_{sh}L_s + L_{load}L_{sh} + L_{load}L_s$

$$A = \begin{bmatrix} -(R_{sh}L_s + R_{sh}L_{load} + R_sL_{load}) & (R_sL_{load} - R_{load}L_s \\ (L_{sh}R_s - L_sR_{sh}) & -(R_sL_{sh} + R_{load}L_{sh} + L_sR_{load}) \end{bmatrix}$$

$$b_1 = \begin{bmatrix} -L_{load} \\ L_{sh} \end{bmatrix}, \quad b_2 = \begin{bmatrix} (L_s + L_{load})V_{dc} \\ L_sV_{dc} \end{bmatrix}$$

In the block diagram of Fig. 8, the non-linear load is represented by a disturbance d and it is added to the nominal load current. The reference shunt current i_{shref} is derived from the net load current i_{ld} after subtracting the reference source current i_{sref}. The calculation of the reference currents i_{sref} and i_{shref} is discussed in the Section 6. The resultant closed loop system is an output feedback switched linear system. The switching ripple amplitude can be determined for the multi-level carrier shifted modulation by extending the method used in [19] and [20]. The proper modulation of a multi-level inverter requires a smooth switching function $s_e(t)$. However, the control signal u_c contains high frequency pulses which result in switching ripples in the shunt current i_{sh} and the load current i_l. The reference i_{shref} current is a computed quantity. As a result, it is free from ripples. The contribution due to a nonlinear load is neglected in this analysis as it is assumed to be very small in comparison with the total load current.

It was reported in [18] that the spectrum of the level shifted unipolar SPWM output u_c of a n-level DCMLI carries a fundamental frequency component as well as switching components at a frequency of f_s and its multiples with the sidebands centered around these frequencies, where f_s is the carrier signal frequency. The PWM output u_c consists of two components; the fundamental component u_{cf} and the switching component u_{co}. Since the fundamental component u_{cf} is the desired signal, it is used for the tracking of the reference input. The switching component u_{co} is filtered and gets propagated through the system controller and combined with the switching function S_e. Here an approximate analysis has been done to determine the ripple present in the switching function S_e. It is assumed that the switching component u_{co} is a square shaped pulse with an amplitude of 1/(n-1), i.e., equal to (1/4) of that for a 5 level inverter [19]. The Fourier series for u_{co} can be written as:

$$u_{co}(t) = \frac{4}{\pi(n-1)} \sum_{p=1,3,5}^{\infty} \frac{1}{p} Sin(p\omega_s t) \quad . \tag{7}$$

Using the linear system theory the expression for the ripples in the switching function can be obtained as:

$$s_r(t) = \frac{4}{\pi(n-1)} \sum_{p=1,3,5}^{\infty} \frac{1}{p} k \left| G_t(jp\omega_{s)} \right| \times Sin(p\omega_s t + \theta_p) \quad (8)$$

where, $G_t(s) = \left[G_{f2}(s) - G_{f1}(s) \right] G(s)$ and $\theta = \tan^{-1}\{ \mathrm{Im}\left| G_t(jp\omega_s) \right| / \mathrm{Re}\left| G_t(jp\omega_s) \right|$. The transfer functions $G_{f1}(s) = i_{sh}(s)/u_c(s)$ and $G_{f2}(s) = i_l(s)/u_c(s)$ are obtained from (6) by substituting $v_s(s) = 0$. $G_c(s)$ is the transfer function of the controller, k is the feed-forward gain and ω_s is the carrier frequency in rad/s. The peak of the switching ripple occurs at the positive to negative transition of the square switching pulses, i.e., at $t = \pi / \omega_s$. The peak value of s_r may be obtained from (8) as:

$$S_r = -\frac{4}{\pi(n-1)} \sum_{p=1,3,5}^{\infty} \frac{1}{p} k \left| G_t(jp\omega_{s)} \right| \sin(\theta) \quad (9)$$

The following can be written using the trigonometric relationship, $\sin(\theta) = \mathrm{Im}\left[G_t(jp\omega_s) \right] / \left| G_t(jp\omega_s) \right|$, and (9) can be reduced as:

$$S_r = -\frac{4}{\pi(n-1)} \sum_{p=1,3,5}^{\infty} \frac{k}{p} \mathrm{Im}\left[G_t(jp\omega_s) \right] . \quad (10)$$

An analysis of the ripple present in the switching function s_e has been done in [19] and it has been reported that multilevel PWM may be modeled by a constant gain and a fixed delay. It can be seen that the frequency of the switching component is the same as the switching frequency and the ripple magnitude is reduced by a factor of 1/(n-1) [18].

The feed-forward gain k is selected on the basis of the maximum ripple condition. It is observed that an increase in the gain k results in increases in both the error amplitude and the amplitude of the ripple. The gain k should be high for improvements in both the steady state and the dynamic performance of the system. Fig. 9 shows the intersection of the switching function with the level shifted carriers for a five level inverter at a specific value of the gain k.

Let V_{tri} be the value of the level of the upper most carrier, as shown in Fig. 9, and T_s be the time period of the carrier. Then the peak-peak magnitude A_c of any level shifted carrier for an n-level inverter will be $2V_{tri}/(n–1)$. The time period of the ripple is the same as that of the carrier. In order for the slope of the carrier to be greater than the slope of the ripple in the switching function, the condition that must be met is as follows.

$$\frac{2V_{tri}/(n-1)}{T_s/2} > \frac{2S_r}{T_s/2} \Rightarrow V_{tri} > S_r(n-1). \quad (11)$$

Substituting (11) in (10), the expression for the feed-forward gain k is obtained as:

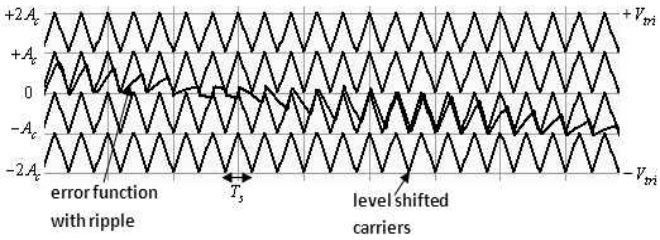


Fig . 9. Error function with ripple intersecting with one triangular carrier in a five level DCMLI.

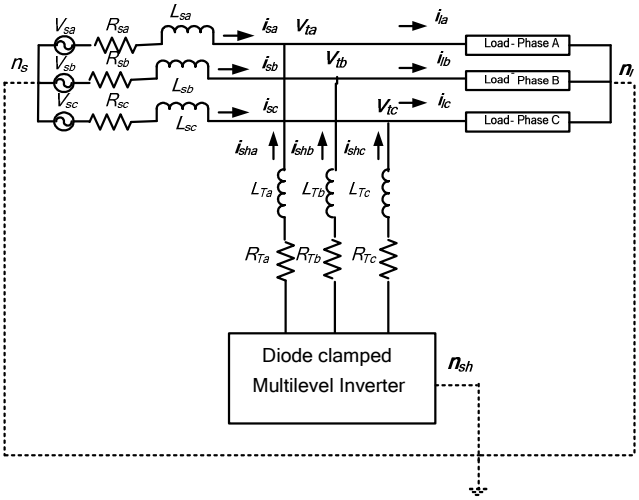


Fig. 10. Shunt compensator used in three-phase four-wire distribution system.

$$k < \frac{\pi V_{tri}}{4 \sum_{p=1,3,5\ldots}^{\infty} \frac{1}{p} \mathrm{Im}\left[G_t(jp\omega_s) \right]} . \quad (12)$$

It can be seen that as the gain is increased beyond the value obtained in (12), the magnitudes of the error function and the ripple also increase and this leads to multiple crossings on each slope of the carrier crossings. As a result, multiple switching takes place, which violates the principle of the fixed frequency switching control method.

VI. Current Generation Algorithm for Three-Phase Systems

Fig. 10 shows a three-phase four-wire shunt compensated distribution system. The three-phase load shown in the figure is supplied from the voltage source v_{sk} through a feeder with an impedance of (R_{sk}, L_{sk}), where k = a,b,c, denote the three-phases. The diode clamped multilevel inverter block shown in the figure represents the VSC configuration. The shunt path contains the interfacing inductance L_{shk} and resistance R_{shk} . The voltage at the grid terminal is denoted by $v_{tk.}$ The currents flowing through the different branches are the source current $i_{sk,}$ the load current i_{lk} and the current injected by shunt branch $i_{shk.}$ For the three-phase, four-wire

configuration, the load neutral and the compensator neutral are connected to the source neutral n_s. The common dc link voltage is represented by V_{dc}.

The data considered for the distribution system and the shunt compensator are given in Table. 1. The load connected to the distribution system is considered to be composed of both linear and nonlinear loads. The linear load is represented by the linear elements L_{lk} and R_{lk}. The nonlinear load consists of the bridge rectifier with the dc side resistance and capacitance represented by (R_{ldc}, C_{ldc}). This nonlinear load is interfaced with the grid through an input impedance represented by (L_{lac}, R_{lac}).

With reference to Fig. 10, the current control of each phase current requires the generation of separate reference shunt currents i_{shref} for each phase. The reference current generation follows the method described in [9], [21]. Taking into account the available wind power through the generator p_{gen}, the expression of the injected reference shunt current is derived [22]. For independent control of the shunt currents in all the three phases in Fig 10, the references are determined using the following equations:

$$\left.\begin{aligned} i_{sharef} &= i_{la} - i_{saref} = i_{la} - \frac{(v_{ta} - v_0)}{\Delta}\left(p_{lav} - p_{gen}\right) \\ i_{shbref} &= i_{lb} - i_{sbref} = i_{lb} - \frac{(v_{tb} - v_0)}{\Delta}\left(p_{lav} - p_{gen}\right) \\ i_{shcref} &= i_{lc} - i_{scref} = i_{lc} - \frac{(v_{tc} - v_0)}{\Delta}\left(p_{lav} - p_{gen}\right) \end{aligned}\right\} \quad (13)$$

where:

$$\Delta = v_{ta}^{\ 2} + v_{tb}^{\ 2} + v_{tc}^{\ 2} - 3v_0^{\ 2}; \quad \frac{v_{ta} + v_{tb} + v_{tc}}{3} = v_0$$

i_{shkref} and i_{skref} (k=a, b, c), respectively, are the reference shunt currents and the reference source currents for the three phases. P_{lav} is the average load power (linear plus non-linear) that is obtained by a moving average filter using continuous measurements of the instantaneous power. The averaging window can be considered to be the immediate previous half cycle [9], [21]. The PCC terminals voltages used (13) are the fundamental frequency components of the switching frequency contaminated terminal voltage extracted online from the measurements of the actual voltages. Therefore, source reference currents i_{skref} in (13) are free from switching ripples.

VII. Simulation Results

Simulations have been performed in PSCAD (ver 4.2.1) software. Both conrol loops, i.e., the capacitor voltage control loop and the shunt current control loop have been implemented in separate modules developed using FORTRAN codes in PSCAD. The data considered in the simulations is given in Table I. A sampling time step of 10 μs is considered for the simulation studies. The moving average filtering of a half-cycle has been considered for the extraction of the average load power P_{lav} in (13). A total of 1000 samples are taken in the averaging window from the immediate previous half cycle.

Table I

System Parameters for 6.6 kV, 1500 kVA Distribution System with Wind Generation System

Parameters		Numerical value
Base voltage, base power		6.6 kV rms (L-L), 1.5 MVA
Frequency f_o		50 Hz.
Wind turbine rotor radius		40 m
Generator rating, phase voltage		1.5 MVA, 7.0 kV
Feeder impedance R_{sk}, L_{sk}, where $(k = a,b,c)$		0.16 Ω, 4.6 mH (0.16 + j1.44) Ω 0.1656 p.u.
Shunt impedance R_{Tk}, L_{Tk},		0.2 Ω, 5.5 mH (0.2 + j1.73) Ω
DC link voltage V_{dc} DC link capacitor C_{dc}		22.0 kV 11000 μF
Load: Linear	Unbalanced	phase-a (68.0+j 34.55) Ω, phase-b (64.0+j 31.41) Ω phase-c (60.0+j 28.27) Ω
	Balanced	(40.0+j 13.19) Ω,
Load: Non Linear		R_{ldc}= 100.0 Ω ,C_{ldc}= 1000 μF R_{lac}= 0.1 Ω , L_{lac}= 2.7 mH

A frequency of f_c= 5 kHz is chosen for the carriers used in the modulation process proposed in Section 3. The uppermost amplitude V_{tri} = 0.05 kV is considered in the simulation. The gain k = 0.945 kV/A is calculated using (12) for fixed switching conditions and the results are obtained at k = 0.9 kV/A, to ensure fixed switching frequency operation.

Varying load conditions are considered in the simulation. Initially, a combination of nonlinear and unbalanced linear loads is connected as given in Table 1. The linear load is increased at time t = 0.2 sec with the insertion of a balanced linear load with the values given in Table 1. The wind speed changes from 8 m/sec to 12 m/sec at t = 0.24 sec. Fig. 11 shows the five level three-phase inverter output voltages. The tracking of the shunt current to its reference is shown in Fig. 12. The three phase compensated source currents, the load currents and the injected shunt currents are shown in Fig. 13. It can be seen from Fig. 13 that the source current becomes balanced and sinusoidal. The unbalanced and harmonic component of the load current is supplied from the DCMLI converter supported

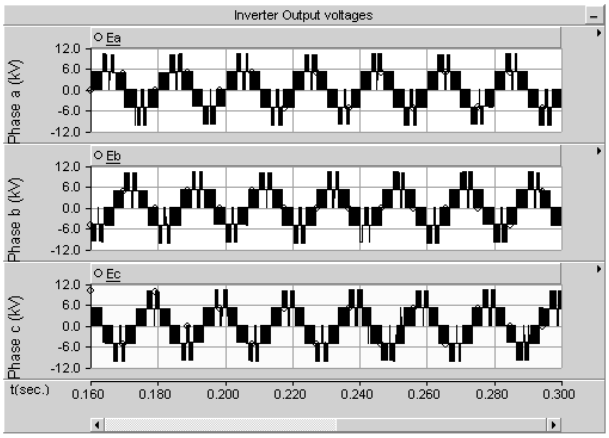


Fig.11. Five level inverter output voltages for three phase system.

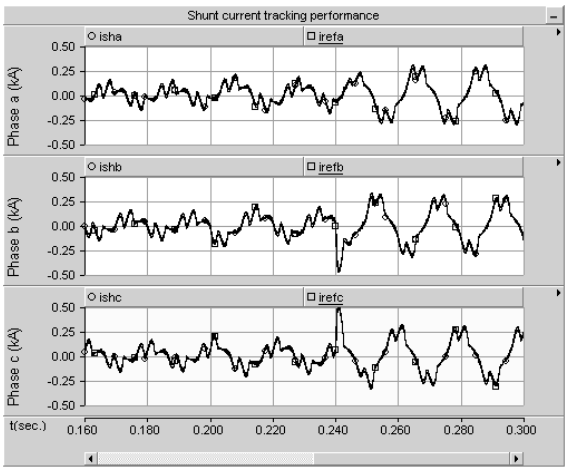


Fig. 12. Shunt current tracking performance of three-phases.

by the wind generator system. In addition, the source current become in-phase with the grid terminal voltage, as shown in Fig. 14, for phase-a.

It is seen from Fig 6 (a) and Fig. 6 (b) that the voltage across the capacitor gets balanced using the capacitor balancing algorithm as per the desirable expectations. The operation of the DCMLI at a fixed switching frequency at the calculated gain k = 0.9 kV/A is shown in Fig. 15. The carriers and error functions shows clear intersections leading to the operation of all of the switches at 5.0 kHz. However, if the gain is increased from the calculated one k = 0.945 kV/A, then it violates condition (12) and leads to multiple crossings. This is shown in Fig. 16 when the simulation is performed at k = 1.1 kV/A and the switches operate at a frequency higher than 5.0 kHz, due the multiple crossings of the switching function with the carriers.

The real power distribution of the load, based on (13), among the grid supply and shunt inverter is shown in Fig. 17. It can be seen that the net load real power is supplied from the wind turbine power and the balance is supplied from the

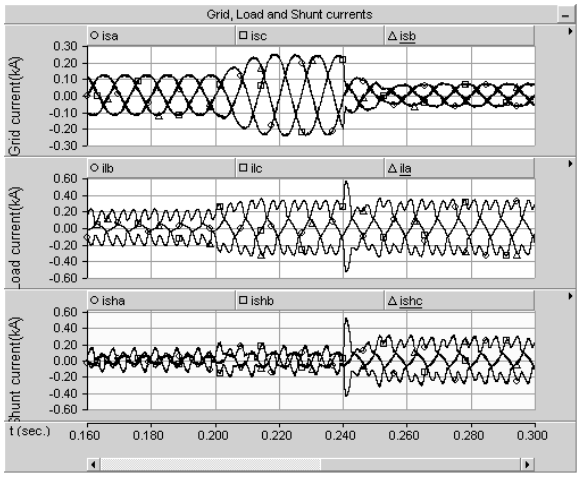


Fig. 13. Source, load and shunt currents for three phase system.

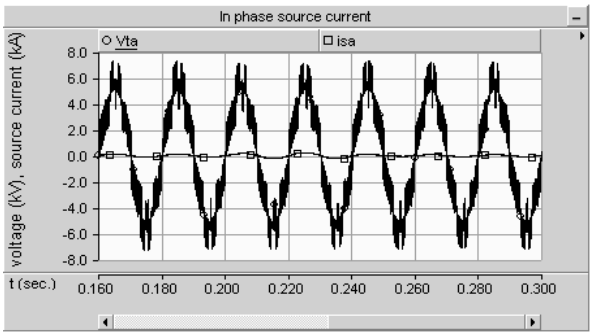


Fig. 14. In-phase source current with the grid terminal voltage for phase-a.

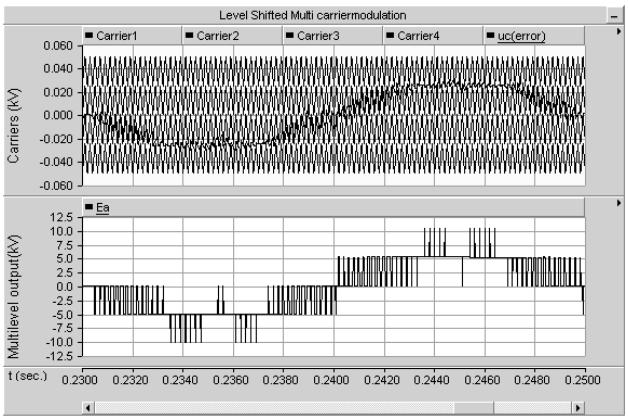


Fig. 15. Fixed switching frequency operation at 5.0 kHz at the gain k = 0.9 kV/A.

grid. At time t = 0.24 sec, when the wind turbine power increases due to increase in wind speed from 8 m/sec to 12 m/sec, the contribution of real power from the grid significantly decreases since the major part of the load is supplied from the shunt inverter. It should be noted that part of the turbine power is also consumed in meeting the inverter circuit losses.

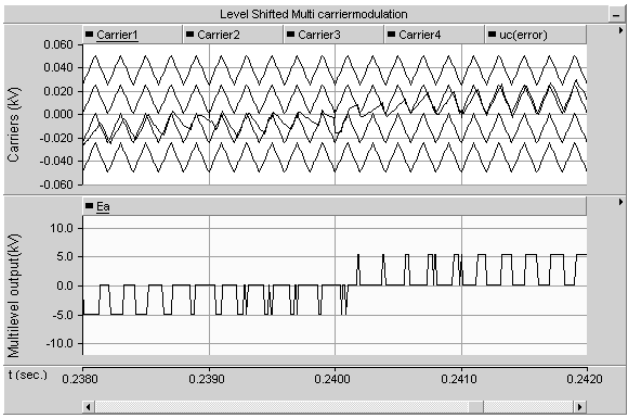


Fig. 16. Multiple crossings and higher switching frequency operation at the gain k = 1.1 kV/A.

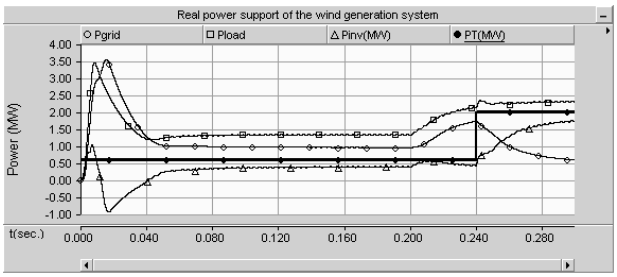


Fig. 17. Distribution of load real power between grid and shunt inverter for addition of balanced load at t = 0.2 sec. and step change in the wind turbine power due to wind speed change from 8 m/sec. to 12 m/sec. at t = 0.24 sec.

VIII. CONCLUSIONS

A diode clamped multilevel inverter is well suited for the current control of a DCMLI used as the grid interface of a higher power rated wind energy conversion system, since it has only a single dc source. The proposed fixed switching frequency control leads to an equal and uniform distribution of the switching stress among the various switches. It is shown that following the proposed gain calculation method ensures the operation of the DCMLI at the fixed frequency of the carrier. With the multicarrier level shifted current control, the net switching frequency increases and the ripple magnitude is reduced leading to a higher feed forward gain and hence better control characteristics. It is shown through simulation results that the available wind power can be controlled to feed the load real power with the balance real power being supplied from the grid. In addition to real power injection, the objective of load compensation is also achieved leading to a balanced, distortion free, unity power factor source current. The voltages across the capacitors of the DCMLI remain balanced under all conditions with the proposed control method.

REFERENCES

[1] G. Todeschini and A. E. Emmanuel, "Wind energy conversion systems as active filters: design and comparison of three control methods," *IET Renewable Power Generation,* Vol. 4, pp. 341-353, Jul. 2010.

[2] A. H. Kasem, E. F. Al-Saadani, H. H. El-Tamaly and M. A. A. Wahab, "Power ramp rate control and flicker mitigation for directly connected wind turbines," *IET Renewable Power Generation,* Vol. 4, No. 3, pp. 261-271, May 2010.

[3] A. Chen, L. Hu and X. He, "A novel type of combined multilevel converter topologies," *30th Annual conf. of IEEE Industrial Electronics Society*, 2004.

[4] M. K. Mishra, A. Joshi and A.Ghosh, "Control schemes for equalization of capacitor voltages in neutral clamped shunt compensator," *IEEE Trans. Power Del*., Vol. 18, No. 2, pp. 538-544, Apr. 2003.

[5] A. Shukla, A. Ghosh and A. Joshi, "Control schemes for DC capacitor voltages equalization in diode-clamped multilevel inverter-based DSTATCOM," *IEEE Trans. Power Del.*, Vol. 23, pp. 1139-1149, Apr. 2008.

[6] D. M. Brod and D. W. Novotny, "Current control of VSI-PWM inverters," *IEEE Trans. Ind. Appl.,* Vol. IA-21, No. 3, pp. 562-570, May 1985.

[7] R. Gupta, A. Ghosh, and A. Joshi, "Cascaded multilevel control of DSTATCOM using multiband hysteresis modulation," in *Proc. IEEE PES General meeting*, pp. 18-22, 2006.

[8] R. Gupta, A. Ghosh, and A. Joshi, "Generalized converter modulation and loss estimation for grid interface applications," *Proc. IEEE PES General meeting*, 2008.

[9] A. Ghosh and G. Ledwich, *Power Quality Enhancement using Custom Power Devices*, 1st Ed., Springer, USA, 2002.

[10] Y. Chen, B. Mwinyiwiwa, Z. Wolanski, and B. T. Ooi, "Unified power flow controller (UPFC) based on chopper-stabilized diode-clamped multi-level inverter," *IEEE Trans. Power Electron*., Vol. 15, No. 2, pp 258-267, Mar. 2000.

[11] J. V. Bloh and R. W. D. Doncker, "Design rules for diode-clamped multilevel inverters used in medium voltage applications," in *Proc. IEEE PESC Conf,*. pp. 165-170, 2002.

[12] J. Pou, R. Pindado, D. Boroyevich, P. Rodriguez, and J. Vicente, "Voltage balancing strategies for diode-clamped multilevel converters," in *Proc. IEEE PESC Conf.*, Queensland, Vol. 5, pp. 3988-3993, 2004.

[13] T. Ishida, K. Matsue, K. Sugita, L. Huang, and K. Sagawa, "DC voltage control strategy for a five-level converter," *IEEE Trans. Power Electron*., Vol. 15, No. 3, pp. 508-515, May 2000.

[14] Y. Chen, B. Mwinyiwiwa, Z. Wolanski, and B. T. Ooi, "Regulating and equalizing DC capacitance voltages in multilevel STATCOM," *IEEE Trans. Power Del*., Vol. 12, No. 2, pp. 901-907, Apr. 1997.

[15] S. Kincic, A. Chandra, and S. Babic, "Five level diode-clamped voltage source inverter and its applications in reactive power compensation," *in Proc. IEEE LESCOPE*, pp. 86-92, 2002.

[16] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6 kV transformer-less STATCOM Based on a five-level diode-clamped PWM converter: system design and experimentation of a 200 V, 10 kV laboratory model," in *Proc. 14th IAS Conf.*, Vol. 1, pp. 557-546, 2005.

[17] M. K. Mishra, A. Joshi, and A. Ghosh, "A new closed loop control scheme for capacitor voltage equalization in shunt compensator using neutral current injection," in *Proc. IEEE PES Winter Meeting*, Vol. 1, pp. 126-131, 2001.

[18] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters* , John Wiley & Sons, IEEE press, 2003.

[19] R. Gupta, A. Ghosh, and A. Joshi, "Control of cascaded transformer multilevel inverter based DSTATCOM," *Electric Power System Research (EPSR),* Vol. 77, No. 8, pp. 989-999, Jun. 2007.
[20] R. Gupta and A. Ghosh, "Frequency-domain characterization of sliding mode control of an inverter used in DSTATCOM application," *IEEE Trans. Circuits Syst. I, Reg. Papers,* Vol. 53, No. 3, pp. 662-676, Mar. 2006.
[21] A. Ghosh and G. Ledwich "Load compensating DSTATCOM in weak AC systems," *IEEE Trans. Power Delivery,* Vol.18, No.4, pp. 1302- 1309, Oct. 2003.
[22] P. Samuel, R. Gupta, and D. Chandra, "Grid interface of wind power with large split-winding alternator using cascaded multilevel inverter," *IEEE Trans. Energy Convers.*, Vol. 26, No.1, pp. 299-309, Mar. 2011.

Paulson Samuel received his B. E. degree in Electrical Engineering from the Shri Govindram Seksaria Institute of Technology and Science, Indore, India, in 1984, and his M. E. degree in Computer Science and Engineering from the Motilal Nehru National Institute of Technology, Allahabad, India, in 1998, where he also received his Ph.D. degree, in 2013. He is presently an Associate Professor in the Department of Electrical Engineering, Motilal Nehru National Institute of Technology. From 1984 to 1990 he served as an Engineer in the National Thermal Power Corporation, New Delhi, India. Since 1990 he has served as a faculty member in the Department of Electrical Engineering, Motilal Nehru National Institute of Technology. His current research interests include power quality, distributed generation, distribution automation and the control of power converters.

M. Kishore Naik received his B.Tech. degree in Electrical Engineering from Sri Venkateswara University, Tirupati, India, India, in 2008, and his M.Tech. degree in Electrical Engineering from the Motilal Nehru National Institute of Technology, Allahabad, India, in 2010. From 2010 to 2011, he was an Assistant Professor at Amity University, Noida, India. Since January 2012, he has been working towards his Ph.D. degree at the University of Padua, Padua, Italy. His current research includes power electronics, power quality and wireless power transfer for electrical vehicles.

Rajesh Gupta received his B. E. degree from the Madan Mohan Malaviya Engineering College, Gorakhpur, India, in 1993, his M. E. degree from the Birla Institute of Technology, Ranchi, India, in 1995, and his Ph.D. degree from the Indian Institute of Technology, Kanpur, India, in 2007, all in Electrical Engineering. From 1996 to 1999, he was a Lecturer with the Govind Ballabh Pant Engineering College, Pauri Garhwal, India. He is currently an Associate Professor with the Department of Electrical Engineering, Motilal Nehru National Institute of Technology, Allahabad, India. His current research interests include control theory, power quality, distributed generation, control of power electronics systems and multilevel converters.

Dinesh Chandra received his B. E. degree in Electrical Engineering from the Madan Mohan Malaviya Engineering College, Gorakhpur, India, in 1973. He received his M. E. and Ph.D. degrees in Electrical Engineering from the Motilal Nehru National Institute of Technology, Allahabad, India, in 1979 and 2002, respectively. He is presently a Professor with the Department of Electrical Engineering, Motilal Nehru National Institute of Technology, Allahabad. His current research interests include control systems, reduced order modeling, optimization and converters control.