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Investigation of Capacitor Voltage Regulation in Modular Multilevel Converters with Staircase Modulation

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Abstract

This paper presents a detailed theoretical analysis and performance assessment of the capacitor voltage balancing strategies for staircase modulated modular multilevel converters (MMC) in terms of the algorithm structures, voltage balancing effect, and switching frequency. A constant-frequency redundancy selection (CFRS) method with minimal switching loss is proposed and the function realization of specific modules of the algorithm is given. This method is simple and efficient in both switching frequency and regulation capacity. Laboratory results show very good agreement with the theoretical analysis and numerical simulations.

Key words: Capacitor voltage balancing, Modular multilevel converter, Redundant switching states, Staircase modulation, Switching frequency

I. INTRODUCTION

The modular multilevel converter (MMC) is a newly devloped and promising power electronic topology due to its remarkable features [1]-[12]. Since this innovative topology was first presented in 2003 [1], [2], it has been catching the attention of the academic and industrial communities [7]. With the rapid development of the manufacturing and control techniques of high-voltage high-power semiconductors, MMC based high-voltage direct current (HVDC) transmission systems have witnessed a great-leap-forward in the growth in many engineering practices [13], [14]. Furthermore, scholars and professionals around the world have achieved fruitful results form research of the theories and applications of MMC [3]-[12].

In the field of high-voltage high-power electric power conversion applications, the switching loss and output waveform quality are commonly regarded as the key performance indicators of the power electronics converter. In addition, the switching loss becomes a serious issue in high-power converters [15]. The fundamental frequency modulation technique, also known as the staircase modulation technique, is shown to be a feasible solution to address this problem [15]-[17], and it has grown up into one of the important research trends of MMC [8], [9], [12].

However, when using the staircase modulation technique, there is an inherent difficulty in capacitor voltage regulation. The staircase modulation, due to its lower switching frequency, has a slower dynamic response speed in terms of voltage regulation than the carrier modulation [4], [6] and space vector modulation (SVM) [2], [3].

In [18] the capacitor voltage of the power unit was compared with the theoretical values using the closed-loop feedback control. Then the phase of the output voltage of each power unit was calibrated according to the proportional-integral (PI) converter to change the received or delivered active power of each power unit in the cascaded H-bridge converter, achieving capacitor voltage balance. In the closed-loop feedback method it is required that the arm currents contain only the fundamental component, but the dc and secondary components cannot be neglected in the arm currents of the MMC [11]. Thus, for the issues of voltage regulation in MMC, the method in [18] can not be adopted directly. The authors of [12] proposed a switching mode to maintain the stability of the stored capacitor energy in each sub-module (SM) during multiple fundamental frequency cycles. This enables MMC to run under the

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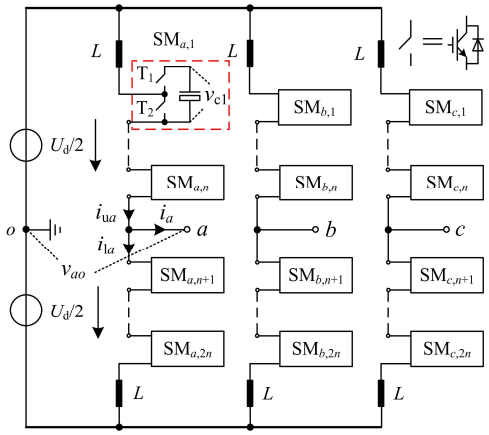


Fig. 1. Basic topology of an MMC.

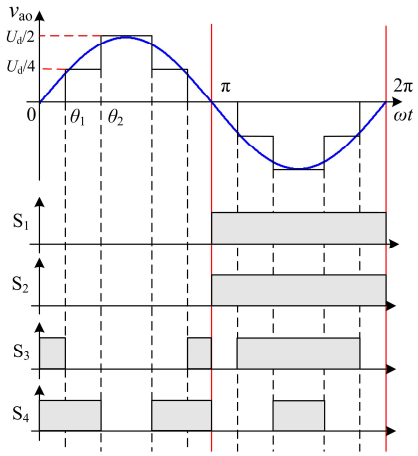


Fig. 2. Diagram of staircase modulation method for MMC.

condition of non-voltage feedback. Nevertheless, the stored energy balance of the capacitor of the sub-module depends on the load type and running status of the MMC. In addition, the dynamic regulation speed is still a challenge. Capacitor voltage balance control strategies, such as switching sequence rotation [19], [20] and redundancy selection [17], [21], [22], are utilized in previous studies but no clear criteria for the feasibility or algorithm structures have been explored. In addition, the applicability of these two strategies in staircase modulated MMC remains to be seen. Moreover, another important matter that needs to be addressed is the contradiction between the effects of capacitor voltage balancing and the converter switching frequency.

The objective of this paper is to explore a reliable capacitor voltage balancing strategy for staircase modulated MMC with an optimized switching frequency. To mitigate the reckless rise of the switching frequency of the MMC, the redundancy selection method has been modified by adding a timing comparator to the feedback loop. The working mechanism, hardware realization, and control performance of the proposed control method are analyzed in detail. The correctness of theoretical analysis and the comparative study are verified through simulations and experimental results.

This paper is organized as follows. Section II describes the MMC system configuration and the operation principles of the staircase modulation. Then, the capacitor voltage balancing strategy is explained in Section III. Section IV provides simulation studies of the voltage balancing control methods which are carried out in the Matlab/Simulink environment. Experimental results conducted on a small-scale prototype are included in Section V. Finally, concluding remarks are drawn in Section VI.

II. Principle and Analysis of the Staircase Modulation in MMC

The main circuit of a MMC is connected with half bridge inverters in series, and its basic topology is shown in Fig. 1. In the Figure, the inductor L is used to provide some buffering against arm current spikes and to restrict the internal circulating currents in the MMC during normal operation. The internal structures of all SMs are uniform. In each SM, T_1 and T_2 are switch units composed of fully controlled power electronic devices (usually IGBTs or MOSFETs) and an anti-parallel diode. T_1 represents the upper switch, T_2 represents the lower switch, and C_{SM} denotes the dc capacitor which provides a stable dc voltage for an individual SM to ensure normal operation. Both the upper and lower arms of each phase contain n SMs. For convenience, S_i (i = 1~2n) is defined as the switching signal of the sub-module $SM_{k,i}$ in phase k (k = a, or b, or c). Then each module has the following equivalence relation:

$$\begin{cases} S_i=1 \Leftrightarrow T_1 \text{ on, and } T_2 \text{ off} \\ S_i=0 \Leftrightarrow T_1 \text{ off, and } T_2 \text{ on} \end{cases} \quad (1)$$

Considering the circulating current suppression and controllability of the capacitor voltage balance, the N+1 level modulation mode [10] is adopted in this paper. In this mode, the SM switching signals of the lower arm are complementary to those of the upper arm, i.e.

$$S_{n+i}=\overline{S_i} \quad (1 \le i \le n) \quad (2)$$

Fig. 2 shows a diagram of the staircase modulation for a single-phase five-level MMC (n=4). S_1~S_4 represent the switching signals of the four SMs on the upper arm of the a-phase from top to bottom, respectively. The shaded area means that the SM is switched on while the non-shaded area implies that the corresponding SM is bypassed. It should be pointed out that the switching signals of the SM on the lower arm are exactly the same as those of the upper, except that they are half a fundamental cycle lagging, which is not described in the Figure due to a lack of space. Note that Fig. 2 only provides one switching sequence among many alternatives. The switch-on and switch-off intervals of the

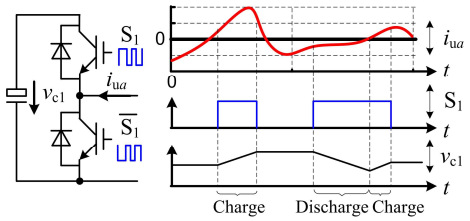


Fig. 3. Diagram of fluctuation of capacitor voltage.

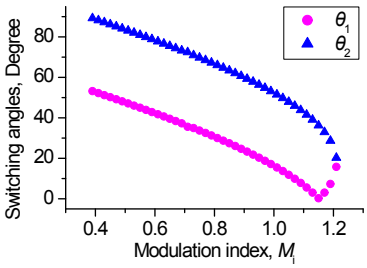


Fig. 4. Switching angles θ_1, θ_2 versus modulation index M_i.

TABLE I

RELATIONSHIP BETWEEN OUTPUT VOLTAGE LEVELS AND THE NUMBERS OF REQUIRED SMS

v_{ao}	$2V_{dc}$	V_{dc}	0	$-V_{dc}$	$-2V_{dc}$
N_U	4	3	2	1	0
N_L	0	1	2	3	4

SMs are equal in each fundamental cycle when the MMC works the switching sequences shown in Fig. 2.

Assume that the rated voltage of each SM remains V_{dc}, then the dc bus voltage U_d should be set to nV_{dc} (= $4V_{dc}$) to fulfil the normal operation requirements. The relationship between the output phase voltage v_{ao} and the number of switched on SMs on the upper and lower arms, N_U and N_L, are shown in Table I. In fact, the capacitor voltages are time-variant, and are closely related to the switching signals and the arm currents. Fig. 3 describes the fluctuations of the capacitor voltage, taking SM number 1 as an example. On the premise of S_1=1, the capacitor voltage swells as the sign of the arm current is positive, and declines only when its sign turns negative. When S_1=0, the capacitor voltage remains unchanged regardless of the changing arm current.

The phase voltage v_{ao} shown in Fig. 2 can be expressed by the Fourier series as follows [15]:

$$v_{ao}(\omega t)=\sum_{m=1,5,7,11,13...}^{\infty}\frac{4V_{dc}}{m\pi}(\cos(m\theta_1)+\cos(m\theta_2)+\cos(m\theta_3)+...+\cos(m\theta_s))\sin(m\omega t) \quad (3)$$

where m represents the harmonic order, and θ_s represents the s^{th} switching angle of the staircase waveform. All of the switching angles satisfy the following restricted condition:

$$0\le\theta_1\le\theta_2\le...\le\theta_s\le\frac{\pi}{2} \quad (4)$$

If V_1 is defined as the fundamental component amplitude of the desired output phase voltage v_{ao} and M_i represents the converter modulation index, then the following relations can be derived:

$$M_i=\frac{V_1}{V_{dc}\cdot n/2}=\frac{2V_1}{nV_{dc}} \quad (5)$$

The switching angles equations can be obtained from (3) and (5) as:

$$\begin{cases}\cos(\theta_1)+\cos(\theta_2)=\dfrac{\pi V_1}{4V_{dc}}=\dfrac{\pi M_i}{2}\\ \cos(5\theta_1)+\cos(5\theta_2)=0\end{cases} \quad (6)$$

By solving the switching angle equation in (6), the switching sequences of the staircase modulated MMC can be developed naturally. Fig. 4 shows the curves of the switching angles versus the modulation indexes. The switching angles are calculated by using the Newton-Raphson method [23].

III. CAPACITOR VOLTAGE REGULATION SCHEMES

Capacitor voltage balancing control is one of the challenging issues in the research of MMC. There are many reasons for imbalances, including both inconsistent circuit parameters and various working statuses. The former is mainly reflected in discrepancies of the parasitic parameters of the switching devices, the switching loss, the shunt loss of the SM, and the delay of the gate signals [24-25]. The latter mainly refers to the unequal charging and discharging of the capacitor, which is caused by the variable switching time intervals of the SMs.

A. Switching Sequence Rotation Method

The capacitor voltage balance cannot be guaranteed if the fixed switching sequences displayed in Fig. 2 have been repeating constantly in each fundamental cycle. Since the switching sequences are ideal, this might result in deviations of the normal operation statuses.

The switching sequence rotation method provides a relatively simple solution for capacitor voltage imbalances, and its realization process is shown in Fig. 5. The pulse width modulation (PWM) signals are generated by rotating the operation of the fixed switching sequences. The switching sequences for an arbitrary modulation index are obtained through the subsystem links of a look-up table and mapping. Meanwhile, the rotation subsystem is controlled by an external fundamental frequency (50Hz) clock.

At a fixed interval of time the algorithm makes the SMs hold certain switching sequences in each fundamental cycle. Usually, the switching sequences rotate once every fundamental cycle, and are illustrated in Fig. 6. Fig. 6 (a) shows the switching sequence distribution of the four SMs on

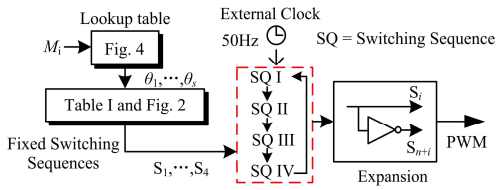


Fig. 5. Block diagram of the switching sequences rotation method.

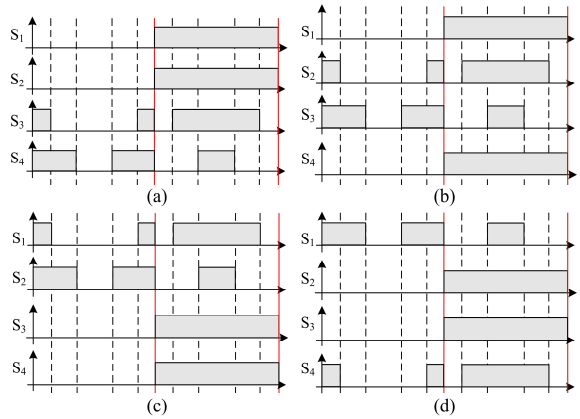


Fig. 6. Combinations of switching sequences. (a) Switching sequence I, (b) Switching sequence II, (c) Switching sequence III, (d) Switching sequence IV.

the upper arm in the first cycle. Only the case of the four upper arm SMs is given here since the PWM signals of the upper and lower arms are mutually complementary. In the next three cycles, the switching sequences are shown in Fig. 6 (b), (c), and (d), respectively. After handling the rotation process, all of the SMs have the same basic switching statuses in multiples of the four fundamental cycles. Therefore, the capacitor voltages of the SMs are theoretically balanced [19], [20].

B. Proposed Control Scheme for Voltage Balancing

It is clear from the illustrations in Table I that outputting different voltage levels only depends on the corresponding number of switched on SMs, provided that the capacitor voltages are kept constant. This indicates that there is redundancy in the switching states [26-27]. Fig. 7 shows an example of all the existing redundant states for a three-level MMC. A total of four redundancy states are shown when the zero level is output. The number of redundancy states R can be calculated by multiplying two combinatorial numbers, as described below.

$$R = C(n, N_U) \cdot C(n, N_L) \tag{7}$$

Analysis shows that the capacitor voltage balancing can be solved by rearranging the switching states while focusing on redundancies in synthesizing the desired output voltage [6, 21]. According to the rearranging principle, priority should be

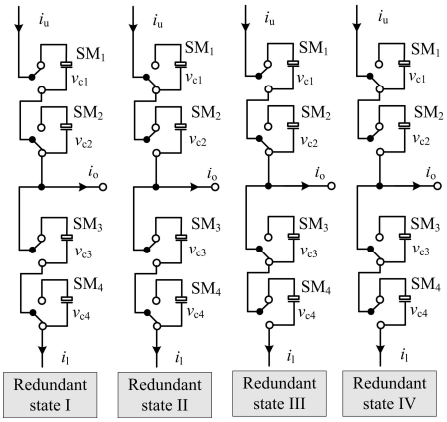


Fig. 7. Diagram of redundant states of MMC.

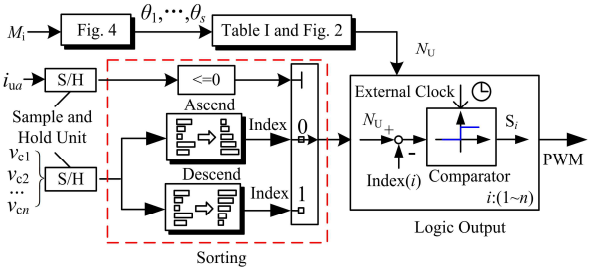


Fig. 8. Block diagram of the CFRS method.

given to the SMs with higher voltages in case of discharging and the SM with a lower voltage has a greater chance of being charged. However, there is little literature available regarding the switching frequency of individual SMs in transitional redundant states, in particular with regard to the application of the staircase modulation strategy. In this paper, a modified control scheme hereafter referred to as the constant-frequency redundancy selection (CFRS) method is proposed.

The CFRS method is divided into three functional modules: sampling, sorting and logic output. Fig. 8 shows a block diagram of the proposed method. The capacitor voltage balancing strategy for the upper and lower arms involves the same functional modules. Therefore, only the control flow for the SMs on the upper arm is described in Fig. 8. In order to reduce the switching frequency of the individual SMs and restrain unnecessary switching actions, the above three functional modules share a synchronous low frequency control clock. The steps for this technique are as follows:

1) N_U is prepared in advance after treatment with look-up table and mapping operations. In addition, a real-time update of N_U is offered for the logic output module.
2) The arm current and capacitor voltages are discretized using a common sample clock.
3) The capacitor voltages are sorted and the sorting direction is determined by the sign of the arm current. The sorting results are expressed by the Index, where

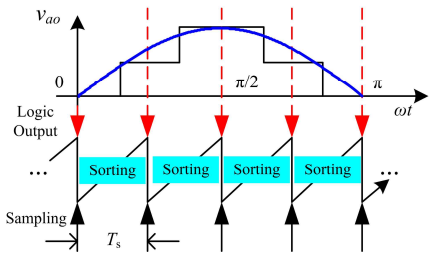


Fig. 9. Time series chart of the CFRS method.

Index(i) represents the numerical order of the i^{th} SM after sorting;

4) The difference between N_U and Index (i) determines the switching status of the i^{th} SM, and is sent to a timing comparator. The timing comparators generate the final output for the PWM signals. The sampling frequency of the sample and hold units should be equal to the external clock frequency of the timing comparators.

5) Repeat steps (2)-(4) while M_i is not updated, otherwise repeat steps (1)-(4).

It should be noted that the emphasis of the CFRS method is on accurate and efficient sorting. Therefore, it is necessary to reserve plenty of time for the controller to execute the time-consuming sorting algorithm. Fig. 9 shows the time sequence of the CFRS method in half a fundamental cycle. This method performs the sampling and logic output procedures at the beginning and the end of each sampling cycle, respectively. Meanwhile, the sorting procedure is completed between them on the timeline. In Fig. 9, the sampling frequency f_s (=1/T_s) is 400Hz. This means that the CFRS method runs 8(=400/50) times in each fundamental cycle. It is clear that as a result of a greater sampling frequency the balancing effect will be improved, on account of the shorter response delay.

IV. Simulation Results

To verify the effectiveness of the proposed method and to compare the performances of the different algorithms on the capability of the voltage regulation, simulations have been carried out with a three-phase five-level MMC with the staircase modulation strategy. The detailed circuit parameters are shown in Table II.

Fig. 10 shows the comparison results of the steady-state capacitor voltage balancing effect with two control strategies. Fig. 10 (a) presents the steady-state behavior employing the switching sequence rotation method. Fig. 10 (b) and (c) display the balancing effects using the CFRS method with sampling frequencies f_s of 50Hz and 200Hz, respectively. As can be seen from the figures, the capacitor voltage ripple of the switching sequence rotation method at the steady state is relatively small, and the algorithm presents a periodic pattern

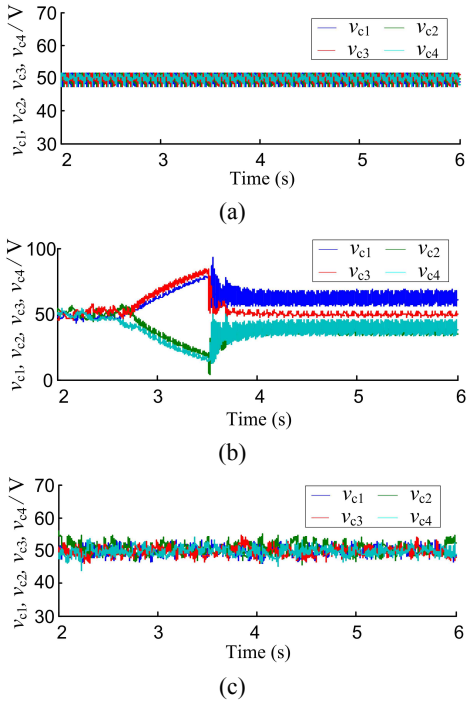


Fig. 10. Simulation results of capacitor voltage balance control in steady-state. (a) Switching sequence rotation. (b) CFRS with f_s of 50Hz. (c) CFRS with f_s of 200Hz.

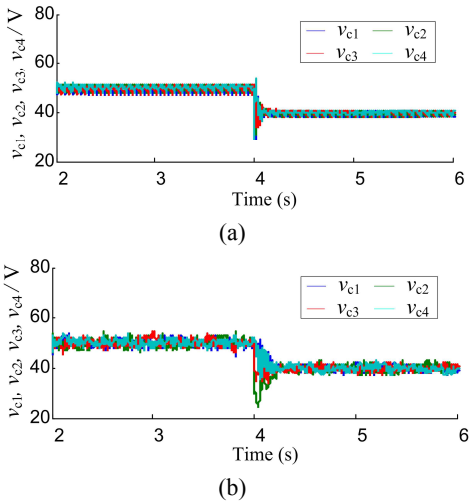


Fig. 11. Simulation results of capacitor voltage balance control under the disturbance of input source change. (a) Switching sequence rotation. (b) CFRS with f_s of 200Hz.

due to its own characteristics. As for the CFRS method, the capacitor voltage imbalance is improved as the sampling frequency is increased. With the application of the N+1 level modulation mode, the capacitor voltage fluctuations of the upper and lower arms of the SMs are approximately consistent. Thus, only the capacitor voltage fluctuations of the upper arm are provided in the rest of the full text.

TABLE II

CIRCUIT PARAMETERS OF THE FIVE-LEVEL MMC SYSTEM

Parameters	Symbols	Values
Total DC bus voltage	U_d	200V
DC bus capacitor capacitance	C_d	4.7mF
Theoretical value of SM voltage	V_{dc}	50V
Individual SM capacitor capacitance	C_{SM}	2.2mF
Number of SMs	n	4
Buffer reactor impedance	L	1mH
Fundamental frequency	f	50 Hz
Modulation index	M_i	1
Load resistance	R_L	20Ω

Fig. 11 shows the simulation results of the capacitor voltage behavior under disturbances of the input source change. The external disturbance in this case study comes from the input DC bus voltage sag. This voltage sag (20%) occurs at 4s of the simulation time. Short-term adjustments (approximately 10~15 fundamental cycles) can be observed from Fig. 11. The simulations reveal that both the switching sequence rotation method and the CFRS method have roughly the same capabilities in resisting external light interference.

To simulate the imbalance phenomenon caused by the parameter drifting of individual SMs during the running of the MMC, a discharge resistance of 100Ω was parallel connected to the sub-module $SM_{a,1}$, while keeping the rest of the SMs unaltered. The resistance is connected at 1s of the simulation time and is removed at 2s. Fig. 12 shows the variation curves of the capacitor voltages on the upper arm with the two different balancing methods. As can be seen from the figure, the voltage offsets, regulated by the switching sequence rotation method, gradually increase with the internal disturbance and cannot be restore even if the disturbance is removed. The CFRS method with a sampling frequency of 200Hz can compensate for the changes of the equivalent power loss of the abnormally working SMs, and it can enable a balance between the charging and discharging of each SM. Therefore, the disturbance has little influence on the capacitor voltage balancing effect.

Fig. 13 shows a comparison of the switching pulses of the sub-module $SM_{a,1}$ with the same initial conditions when the capacitor voltage transits from the transient-state to the steady-state. As shown in the figure, for the switching sequence rotation method, the switching pulse appears repetitively in every four fundamental cycles. Under the same conditions, the CFRS method allows the capacitor voltage to enter into the steady-state faster. In addition, in the transient-state the switching frequency is high, but in the steady-state the switching frequency decreases while the duty cycle remains irregular.

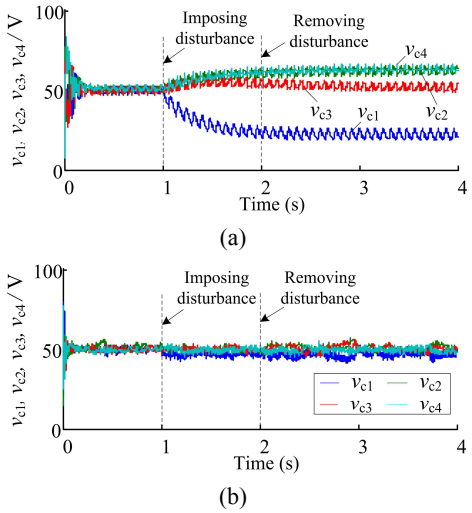


Fig. 12. Simulation results of capacitor voltage balance control under the disturbance of SM voltage discharging. (a) Switching sequence rotation. (b) CFRS with f_s of 200Hz.

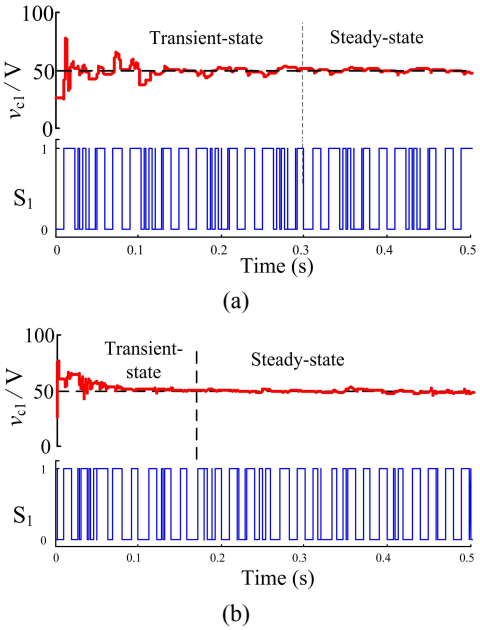
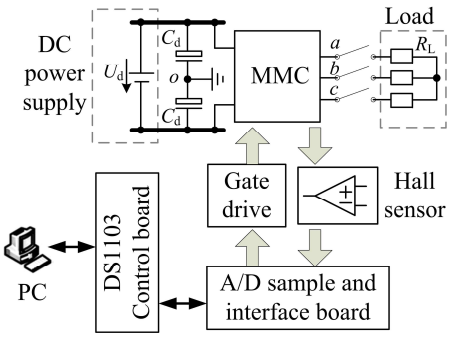


Fig. 13. Simulation results of changes of switching frequency. (a) Switching sequence rotation. (b) CFRS with f_s of 200Hz.

V. EXPERIMENTAL RESULTS

In order to verify the simulation and analytical results, a hardware prototype of the system was developed. In the experiments, the dc bus is fed by a 200-V dc source and two 4.7-mF capacitors are connected in series to the dc bus to construct the neutral point. The voltage of each SM capacitor is set to 50 V. The staircase modulation strategy has been



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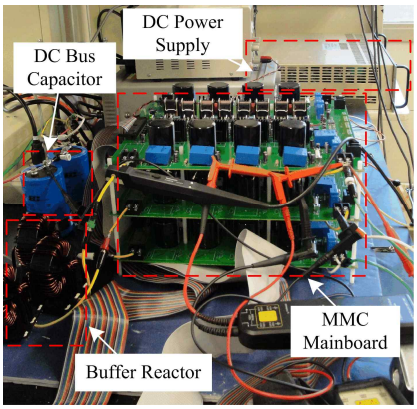


(b)

Fig. 14. The MMC hardware used for experimental validation. (a) Hardware configuration. (b) Laboratory prototype.

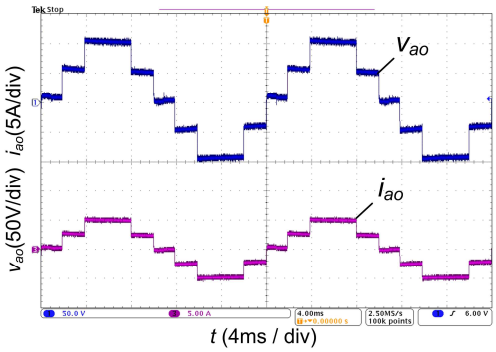
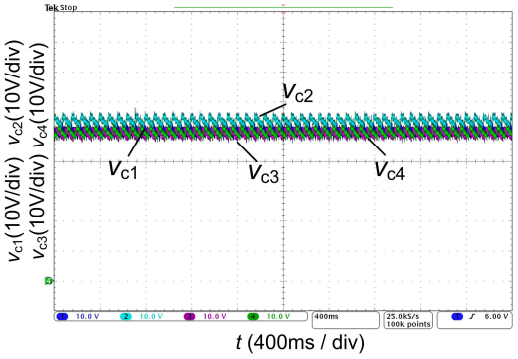


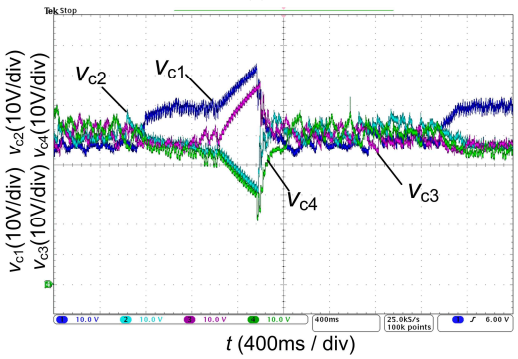
Fig. 15. Experimental waveforms of output voltage and current of a-phase.

implemented on the three-phase five-level MMC system. The complete system is controlled by a dSPACE DS1103 board to carry out the algorithm execution and the real-time control, as shown in Fig. 14. To compare the experiment results with the previous MATLAB simulations, the circuit parameters used in the experiments are identical to those used in the simulations.

Fig. 15 shows the waveforms of the output phase voltage and current of the *a*-phase employing the CFRS method at a sampling frequency of 200Hz.



(a)



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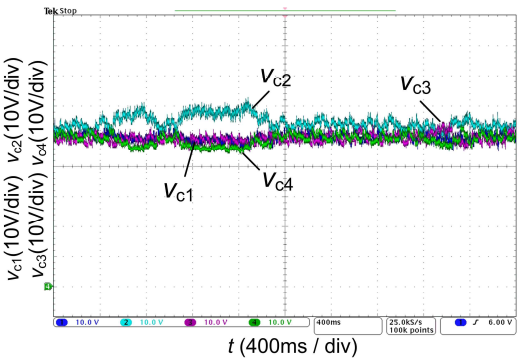

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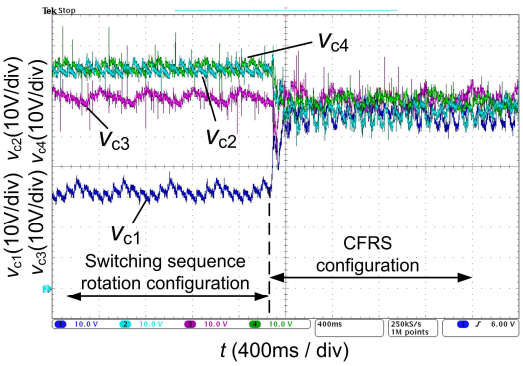

(d)

Fig. 16. Experimental results of capacitor voltage balance control. (a) Switching sequence rotation in steady-state. (b) CFRS with f_s of 50Hz in steady-state. (c) CFRS with f_s of 200Hz in steady-state. (d) Transition control between switching sequence rotation and CFRS configurations in transient-state.

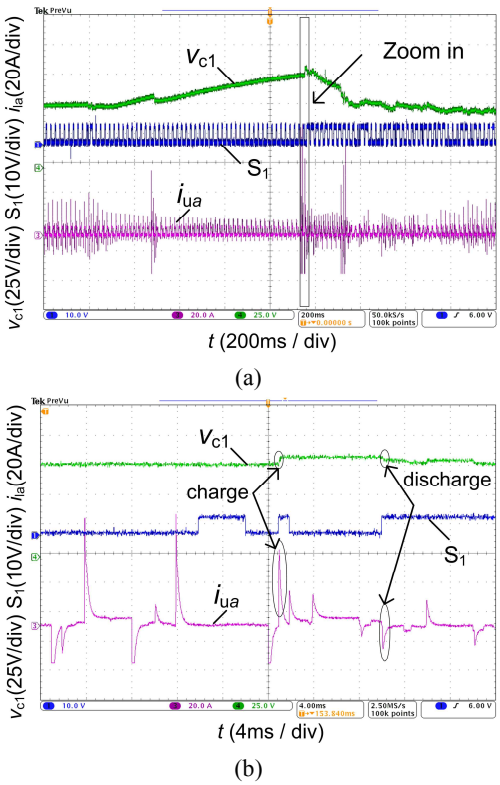

Fig. 17. Examples of measured waveforms of capacitor voltage fluctuations using CFRS with f_s of 50Hz. (a) in steady-state. (b) Expanded waveforms.

Fig. 16 displays the control performance of the different voltage balancing control strategies. The steady-state experimental results for capacitor voltage regulation utilizing the switching sequence rotation method are shown in Fig. 16(a). Fig. 16(b) and (c) show the steady-state experimental waveforms of the capacitor voltages with the CFRS method at sampling frequencies of 50Hz and 200Hz, respectively. It can be seen that the voltage imbalance is improved by turning up the sampling frequency. Fig. 16(d) shows the transient-state performance of the capacitor voltages during the transition from the switching sequence rotation configuration to the CFRS configuration with a sampling frequency of 200Hz. During the switching sequence rotation configuration, an imbalance occurs when an external resistance of 100Ω was parallel connected to the sub-module $SM_{a,1}$. However, the capacitor voltages are gradually adjusted to the normal range within 10 fundamental cycles when the CFRS method takes action. As can be seen from Fig. 16, in the steady-state the control effect of the switching sequence rotation method is better than that of the CFRS method both in terms of stability and regularity. However, it lacks reliable regulation capacity, which affects the control effect in the transient-state. On the other hand, the CFRS method has a disturbance-recovery ability in the presence of the disturbance.

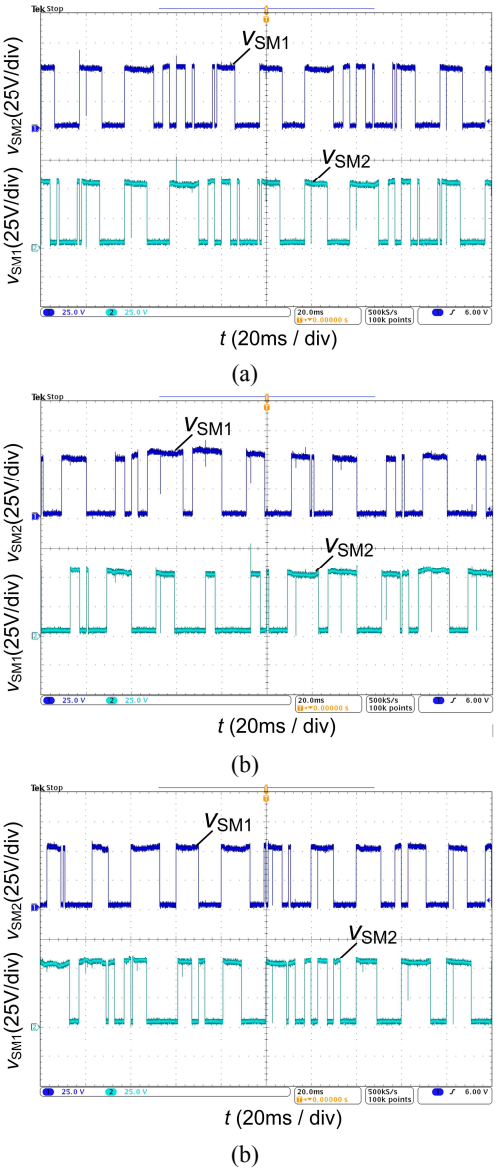

Fig. 18. Experimental waveforms of changes of switching frequency of individual SM in steady-state. (a) Switching sequence rotation. (b) CFRS with f_s of 50Hz. (c) CFRS with f_s of 200Hz.

Fig. 17 shows the capacitor voltage fluctuations of individual SMs by means of monitoring the capacitor voltage, the gate drive signal, and the arm current. It should be pointed out that the experiment in Fig.17 is an extreme example, which is intended to validate the associations among the capacitor voltages, the switching signals, and the arm currents. In this experiment, the CFRS method at a sampling frequency of 50Hz is adopted. The processes of charging and discharging, as seen in Fig. 17(b), coincide with the theoretical analysis.

Fig. 18 shows the steady-state output voltages of two SMs on the upper arm of the *a*-phase under the different balancing

control strategies. According to the principle of the MMC, the changes of the switching frequency of individual SMs can be observed indirectly through the measurement of v_{SM1} and v_{SM2}. As can be seen from Fig. 18, the equivalent switching frequency of the SMs, controlled by the switching sequence rotation method, is fixed, while that of the CFRS method is not constant. In addition, it is slightly higher than the former during the steady-state, and the maximum limit of the CFRS method is near to its sampling frequency.

VI. CONCLUSIONS

This paper presents a comprehensive analysis and experimental evaluation of the staircase modulation techniques for the implementation of the capacitor voltage balance control in MMC systems. The operation principle and implementation details of the capacitor voltage regulation methods are examined. This paper also presents a constant-frequency redundancy selection method to restrict the excessive rise in the switching frequency for the whole converter, and to offer the possibility of low switching losses and a low computation burden on the processor. The simulations and hardware implementation of a three-phase five-level MMC are carried out to evaluate the theory. The simulation and experimental results show that the steady-state performance of the switching sequence rotation method is excellent, while the constant-frequency redundancy selection method exhibits a strong ability in terms of transient regulation, which results in good practicality and reliability.

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