Design and Analysis of an Interleaved Boundary Conduction Mode (BCM) Buck PFC Converter

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Abstract

This paper presents the design considerations and analysis for an interleaved boundary conduction mode power factor correction buck converter. A thorough analysis of the harmonic content of the AC line current is presented to examine the allowable voltage gain (K value) for meeting the EN61000-3-2, Class D standard while maximizing efficiency. The results of the harmonic analysis are used to derive the required value of K and therefore the output voltage necessary to meet the class D requirements for a given AC line voltage. The discussed design consideration and harmonic current analysis are verified on a 300W universal line experimental prototype converter with an 80V output. The measured efficiencies remain above 96% down to 20% of the full load. The input current harmonics also meet the IEC61000-3-2 (class D) standard.

Key words: Boundary Conduction Mode (BCM), Buck converter, Interleaving, PFC

I. INTRODUCTION

Typically the power supplies used in computing, networking and telecom systems operate at below 50% of their rated power due to redundancy in design. Even the power supplies used in personal computers, which do not have redundancy in design, rarely operate at their rated capacity. Environmental concerns about the efficiency of power conversion circuits under their actual operating conditions have prompted the creations of minimum efficiency requirements through a number of government energy efficiency standards and specifications.

Specifically, the U.S. Environmental Protection Agency's (EPA) Energy Star and the European Code of Conduct (CoC) specifications have defined the minimum average efficiencies at 100%, 75%, 50% and 25% of full load [1], [2]. The 80 PLUS initiative certifies computer power supply products that meet efficiency requirements at 100%, 50% and 20% of rated load [3] as summarized in Table I. Some advanced specifications, such as 80 PLUS Titanium, have already included 10% load efficiency requirements [3] and it is very likely that other specifications will be affected.

For universal input applications that require power factor

correction (PFC) in the front end to meet input current harmonic regulations such as IEC61000-3-2, maintaining a high efficiency over the entire load and line range has been a major design challenge. This is due to the fact that the preferred boost topology for PFC typically exhibits a 1%–3% lower efficiency at low line when compared to that of high line since a large input current causes severe conduction losses in the switch and bridge rectifier diode. The high output voltage of a boost converter, which is typically in the 380-400 V range, also has an unfavorable effect on the switching losses and electro-magnetic interference (EMI) of down-stream DC-DC converters.

These drawbacks of boost PFC pre-regulators can be overcome by using a buck converter for the PFC. This allows for high efficiency across the entire line range while reducing the switching losses and EMI of down-stream DC-DC converters. The buck PFC converter operation was first described in [4]. Detailed comparative analyses between buck PFC and its boost counterpart have shown that buck PFC features a higher efficiency at low line and exhibits lower common mode (CM) EMI [5], [6]. Detailed analyses and improvements on the control method have been discussed to maximize efficiency while complying with harmonic current limits [6]-[18]. The clamp current buck PFC proposed in [6], [7] simplified the control of the continuous conduction mode (CCM) buck PFC which is suitable for cost sensitive applications. The boundary conduction mode (BCM)

80 PLUS Certification	115V Internal Non-Redundant				230V Internal Redundant			
% of Rated Load	10%	20%	50%	100%	10%	20%	50%	100%
80 PLUS	---	80%	80%	80%	N/A			
80 PLUS Bronze	---	82%	85%	82%	---	81%	85%	81%
80 PLUS Silver	---	85%	88%	85%	---	85%	89%	85%
80 PLUS Gold	---	87%	90%	87%	---	88%	92%	88%
80 PLUS Platinum	---	90%	92%	89%	---	90%	94%	91%
80 PLUS Titanium	---	---	---	---	90%	94%	96%	91%

operation of buck PFC and its analysis were presented in [8], which simplified the control and improved the efficiency by eliminating the reverse recovery loss of the freewheeling diode. However, the BCM approach exhibits a relatively large pulsating input current whose peak is twice its CCM counterpart and inevitably necessitates a larger differential mode (DM) EMI filter in the input side. This offsets the benefits of the BCM approach and the practical power level has been limited to below 150W. Another shortcoming of BCM operation is that its switching frequency becomes extremely high, especially for high line and light load conditions. This causes detrimental effect on the efficiency at the light load condition.

The limitations of BCM operation can be overcome by using the interleaving technique. This reduces the input current ripple and, consequently, the size of the EMI filter extending their practical power level to above 150W. In addition, the output current ripple can be also significantly reduced by ripple cancellation resulting in a longer life time of the output capacitor. Another benefit of interleaving is that the light load efficiency can be improved by shedding one of the parallel connected converters under the light load condition, which is known as phase management. By shedding one converter, the power that the remaining converter should handle becomes doubled allowing the switching frequency to be halved. This technique is very effective in improving light load efficiency at the high line condition by reducing the switching loss.

While interleaving converters with a fixed switching frequency is relatively easy, interleaving BCM converters is challenging since the switching frequency continuously varies with the instantaneous line voltage and output load conditions [9]-[10]. In general, interleaving techniques can be classified into two categories: the open loop master-slave method ([11]-[12]) and the PLL based closed loop method ([13]-[17]). The open loop master-slave method has difficulty in guaranteeing stable BCM operation against tolerance of the inductor values and PWM control circuits. Once the BCM operation is lost, the converter operates in CCM and the input current is significantly distorted. The closed loop method can guarantee BCM operation of each converter regardless of the
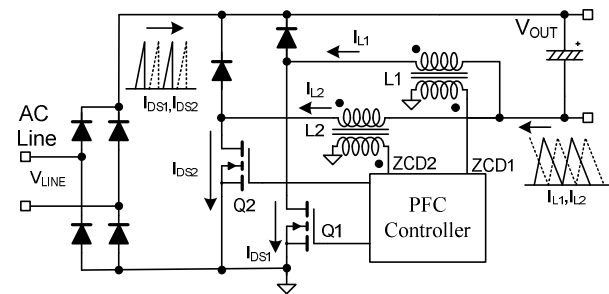

Fig. 1. Interleaved BCM buck PFC converter.

tolerance of the inductor value and PWM control circuits. However, the closed loop method responds to phase shift disturbances relatively slowly and it takes several tens of switching cycles to correct these disturbances. To alleviate the problem of the PLL based closed loop method, the cross-coupled master-slave method was proposed, which responds to disturbances very fast and guarantees a stable interleaving operation against any transient or disturbance ([18]-[20]).

This paper presents a thorough analysis of the interleaved BCM buck PFC converter along with a design optimization to meet the IEC61000-3-2 class D harmonic limits while maximizing efficiency.

II.   LINE CURRENT DISTORTION ANALYSIS

The cross-coupled master slave interleaving method was originally proposed for BCM boost PFC in [21], [22]. However, it can be utilized better when applied to BCM buck PFC since BCM buck converters inherently have abrupt operation transition around the line current zero crossing. Fig. 1 and Fig. 2 show a circuit diagram of the interleaved BCM buck PFC converter and its key waveforms. As can be seen in Fig. 2, a constant ON time is provided from the PFC controller, where the ON time is maintained constant for at least one half a mains cycle to achieve PFC functionality. The turn-on instant of the gate drive signal of the BCM buck converter is determined by the inductor current zero current detection (ZCD). However, while the instantaneous line voltage is smaller than the output voltage, the ZCD is lost since there is no inductor current. Then, the turn-on instant is typically determined by a clock signal given by the internal reset timer of the PFC controller. This introduces a sudden change in the switching frequency when BCM operation is resumed as the instantaneous line voltage rises above the output voltage.

When the instantaneous line voltage is smaller than the output voltage, the buck PFC draws no current from the AC mains since the bridge rectifier is reverse-biased. This introduces a dead angle (θ_Z) to the line current at around the line zero crossing, as shown in Fig. 2. The dead angle increases the total harmonic distortion (THD) and lowers the
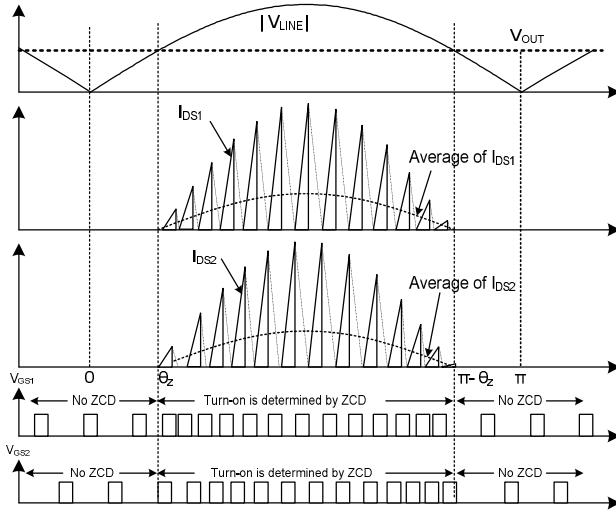
Fig. 2. Interleaved BCM buck PFC converter and key waveforms.

power factor. The dead angle is related to the ratio between the output voltage and the line voltage amplitude as:

$$\theta_Z = \sin^{-1}(K) \qquad (1)$$

where: $K = \dfrac{V_{OUT}}{\sqrt{2}V_{L.RMS}}$.

With the constant ON time given by the BCM PFC controller, the inductor peak current of a single PFC converter is proportional to the difference between the instantaneous line voltage and the output voltage. Then, the average inductor current that is locally averaged over the corresponding switching period can be obtained as:

$$< I_L(\theta) >_{Ts} = \frac{T_{ON}\sqrt{2}V_{L.RMS}(\sin(\theta)-K)}{2L}, \; for \; \theta_Z < \theta < \pi-\theta_Z \qquad (2)$$
$$= 0, otherwise$$

With a given ON time, the output power of a single PFC converter can be obtained as:

$$P_{OUT} = \frac{2}{\pi} \int_{\theta_z}^{\pi/2} V_{OUT} < I_L(\theta) >_{Ts} d\theta$$
$$= \frac{V_{OUT}T_{ON}\sqrt{2}V_{L.RMS}}{\pi L}[\cos(\theta_Z)-K(\frac{\pi}{2}-\theta_Z)] \qquad (3)$$

By rearranging (3), the ON time with a given output power can be obtained as:

$$T_{ON} = \frac{\pi L \cdot P_{OUT}}{V_{OUT}\sqrt{2}V_{L.RMS}[\cos(\theta_Z)-K(\frac{\pi}{2}-\theta_Z)]} \qquad (4)$$

From the power balance between the input and the output it can be seen that:

$$< I_L(\theta) >_{Ts} V_{OUT} \; = \; < I_{DS}(\theta) >_{Ts} \sqrt{2}V_{L.RMS} \sin(\theta) \qquad (5)$$

The average MOSFET current of a single converter that is locally averaged over the corresponding switching period is obtained as:

$$< I_{DS}(\theta) >_{Ts} = \frac{T_{ON}V_{OUT}(\sin(\theta)-K)}{2L\cdot\sin(\theta)}$$
$$= \frac{\pi \cdot P_{OUT}(\sin(\theta)-K)}{2\sqrt{2}\cdot V_{L.RMS}[\cos(\theta_Z)-K(\frac{\pi}{2}-\theta_Z)]\cdot\sin(\theta)} \qquad (6)$$
$$, for \; \theta_Z < \theta < \pi-\theta_Z$$
$$= 0 \qquad ,otherwise$$

The line current of the interleaved PFC converter which is twice the locally averaged MOSFET current is plotted in Fig. 3 with a given line voltage and output power for different values of K. Note that the input current is normalized to the current when K=0.2. As *K* increases the dead angle increases while the line current changes from a "U" shape to a crossover distorted sine shape. The line current also exhibits a higher peak as *K* increases.

To examine the impact of *K* on harmonic distortion, the current amplitude of the n-th order harmonic is calculated as:

$$I_H(n) = \frac{2}{\pi}\int_{\theta_z}^{\pi-\theta_z}[\frac{T_{ON}V_{OUT}(\sin(\theta)-K)}{2L\sin(\theta)}\sin(n\theta)]d\theta \qquad (7)$$

The amplitude of the current of the n-th order harmonic as a percentage of that of the fundamental current is given as:

$$\frac{I_H(n)}{I_1} = \frac{\int_{\theta_z}^{\pi-\theta_z}[\frac{(\sin(\theta)-K)}{\sin(\theta)}\sin(n\theta)]d\theta}{\int_{\theta_z}^{\pi-\theta_z}[(\sin(\theta)-K)]d\theta} \times 100\% \qquad (8)$$

Since the even harmonics are all zero, only the odd harmonics are numerically calculated and plotted in Fig. 4, Fig. 5 and Fig. 6 as percentages of the fundamental current for different values of *K* along with the IEC61000-3-2 class D limit. The original class D specification is a combination of the relative limit proportional to the input power and the absolute limit. To simply compare the specifications with the harmonics expressed as a percentage of the fundamental current, the class D harmonic specification is scaled to a percentage of the fundamental current under the 600W condition by multiplying the original relative limit by 230.

Fig. 4 shows that the 3rd through the 11th order harmonics are all below their limits when *K* is smaller than 0.83. Fig. 5 shows that the 13th through the 23rd order harmonics all meet their limits when *K* is smaller than 0.88. Fig. 6 shows that the 25th through the 39th order harmonics all comply to their limits regardless of *K*. It follows from Fig. 4, Fig. 5 and Fig. 6 that the BCM buck PFC converter employing constant ON time control can meet the IEC61000-3-2 class D harmonic current limit with *K* smaller than 0.83. For the universal line voltage (90 - 265V_AC), the output voltage can be set as high as 105V, while meeting the Japanese specification corresponding to the IEC61000-3-2 class D limit.

All of the harmonic current analysis done in this section is valid only for BCM operation where the switching frequency varies with the load and instantaneous line voltage. It is worth
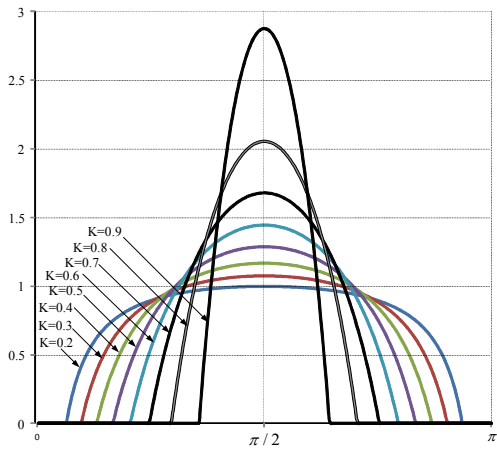
Fig. 3. Input current waveform with different voltage ratio K for a given load condition (Normalized to the input current when K=0.2).
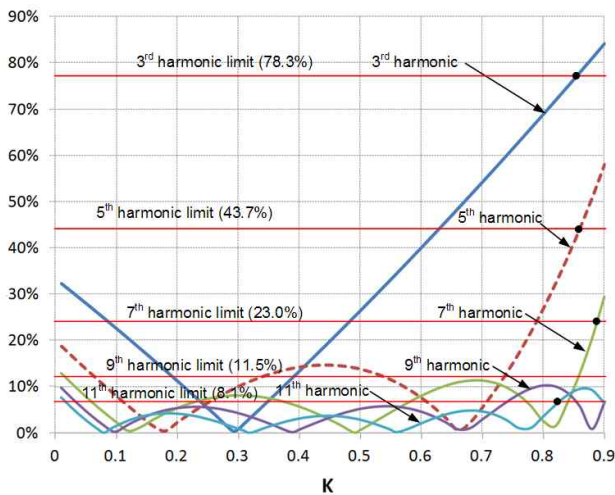

Fig. 4. Harmonic currents and their class-D limit for different K values (3rd through 11th).

Fig. 5. Harmonic currents and their class-D limit for different K values (13rd through 23rd).
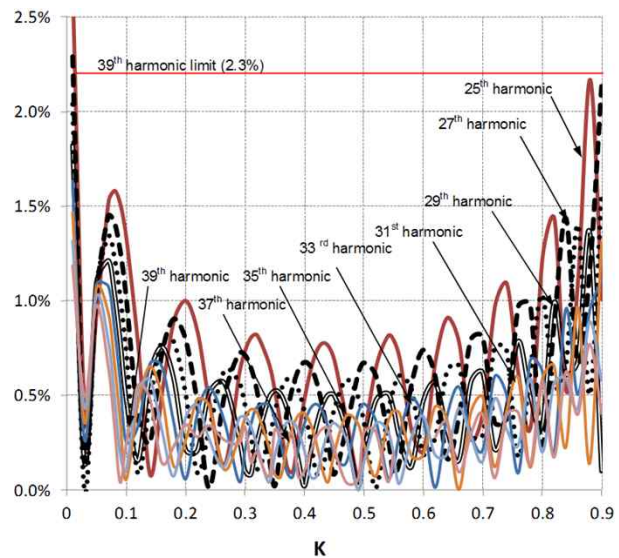
Fig. 6. Harmonic currents and their class-D limit for different K values (25th through 39th).

examining the frequency variation since the BCM buck converter operates in the DCM and does not conduct the PFC function properly when the switching frequency reaches the maximum that the controller allows.

The switching frequency to maintain the BCM operation can be obtained as:

$$f_{SW} = \frac{D(\theta)}{T_{ON}} = \frac{V_{OUT}^2[\cos(\theta_z) - K(\frac{\pi}{2} - \theta_z)]}{\pi L \cdot P_{OUT} \sin(\theta)}, for \ \ \theta_z < \theta < \pi - \theta_z \quad (9)$$

Fig. 7 shows how the switching frequency varies with the load and instantaneous line voltage by using (9) where the inductor is 100 µH and the output power per converter is 150 W. As observed, the switching frequency is extremely high under the light load condition especially for high line. To maintain a high efficiency under that condition, it is necessary to limit the switching frequency or to employ power management which shuts down one converter under light load so that the power that the remaining converter should handle is doubled halving the switching frequency.
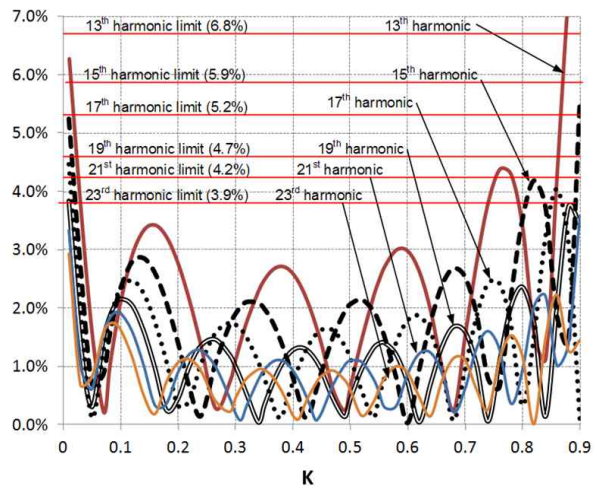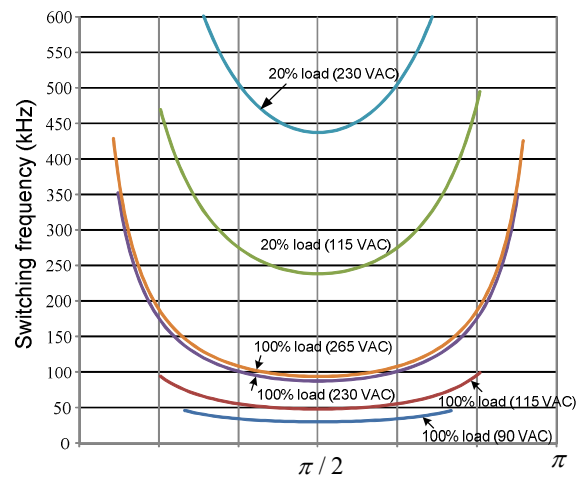

Fig. 7. Switching frequency variation for different line voltage and load condition (P_{OUT}=150W per converter, L=100 µH).

III. POWER STAGE DESIGN CONSIDERATIONS

To identify the optimal output voltage of the BCM buck PFC converter to maximize the efficiency, several currents that mainly contribute to the losses are analyzed in this section. The equivalent RMS value of the MOSFET current of a single buck PFC converter over the corresponding switching period can be obtained as:

$$
\begin{aligned}
< I_{DS}{}^{RMS}(\theta) >_{Ts} &= 2 < I_L(\theta) >_{Ts} \cdot \sqrt{\frac{D(\theta)}{3}} \\
&= \frac{\pi P_{OUT}}{\sqrt{3 V_{OUT} \sqrt{2} V_{L.RMS}}} \cdot \frac{[\sin(\theta) - K]/\sqrt{\sin(\theta)}}{\cos(\theta) - K(\frac{\pi}{2} - \theta_Z)} \\
&\quad , for \quad \theta_z < \theta < \pi - \theta_z \\
&= 0, \text{ } therwise
\end{aligned}
\tag{10}
$$

where $D(\theta)$ is the duty cycle ratio at a given angle θ defined as:

$$
D(\theta) = \frac{V_{OUT}}{\sqrt{2} V_{L.RMS} \sin(\theta)}
\tag{11}
$$

By root-mean-squaring (10) over half of a line cycle, the RMS value of the MOSFET current of a single buck PFC converter can be obtained as:

$$
\begin{aligned}
I_{DS}{}^{RMS} &= \sqrt{\frac{2}{\pi} \int_{\theta_z}^{\pi/2} [< I_{DS}{}^{RMS}(\theta) >_{Ts}]^2 \, d\theta} \\
&= \frac{\sqrt{2\pi} P_{OUT} \cdot \sqrt{\cos(\theta) - 2K(\frac{\pi}{2} - \theta_Z) - K^2 \ln(\tan(\theta_Z))}}{\sqrt{3 V_{OUT} \sqrt{2} V_{L.RMS}} \cdot [\cos(\theta) - K(\frac{\pi}{2} - \theta_Z)]}
\end{aligned}
\tag{12}
$$

The average line current of a single PFC converter is given as:

$$
\begin{aligned}
I_{LINE}{}^{AVG} &= \frac{2}{\pi} \int_{\theta_z}^{\pi/2} \frac{< I_L(\theta) >_{Ts} \cdot V_{OUT}}{2\sqrt{2} V_{L.RMS} \sin(\theta)} \, d\theta \\
&= \frac{P_{OUT}}{\sqrt{2} V_{L.RMS}} \cdot \frac{(\frac{\pi}{2} - \theta_Z) + K \cdot \ln(\tan(\theta_Z))}{\cos(\theta) - K(\frac{\pi}{2} - \theta_Z)}
\end{aligned}
\tag{13}
$$

The average diode current of a single buck PFC converter is obtained as:

$$
\begin{aligned}
I_{DIODE}{}^{AVG} &= \frac{2}{\pi} \int_{\theta_z}^{\pi/2} \frac{< I_L(\theta) >_{Ts} \cdot (\sqrt{2} V_{L.RMS} \sin(\theta) - V_{OUT})}{2\sqrt{2} V_{L.RMS} \sin(\theta)} \, d\theta \\
&= \frac{P_{OUT}}{V_{OUT}} \cdot \frac{\cos(\theta) - 2K(\frac{\pi}{2} - \theta_Z) - K^2 \ln(\tan(\theta_Z))}{\cos(\theta) - K(\frac{\pi}{2} - \theta_Z)}
\end{aligned}
\tag{14}
$$

Fig. 8 shows how the RMS current of the MOSFET varies with the output voltage and line voltages by using (12). It follow that the conduction loss at high line is reduced as the output voltage increases. However, the MOSFET conduction loss at the minimum line voltage of the universal range has its minimum when the output voltage is around 80V. Meanwhile, setting the output voltage higher than 80V results in severe conduction loss in the MOSFET at low line. It should be noted that the MOSFET RMS current of the buck PFC is significantly larger than that its boost counterpart. Therefore,
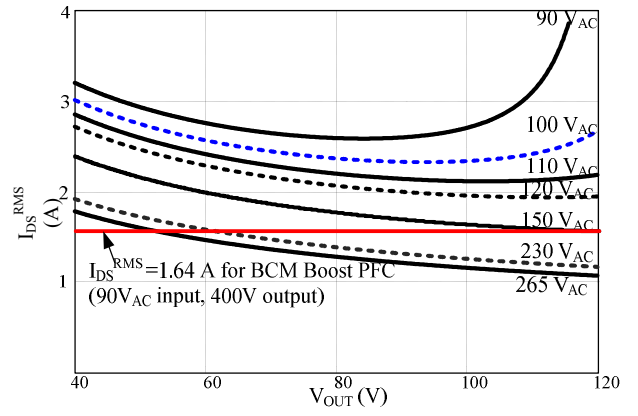

Fig. 8. RMS value of MOSFET current of a single buck PFC converter as a function of output voltage for different line voltages (P_{OUT}=150W)
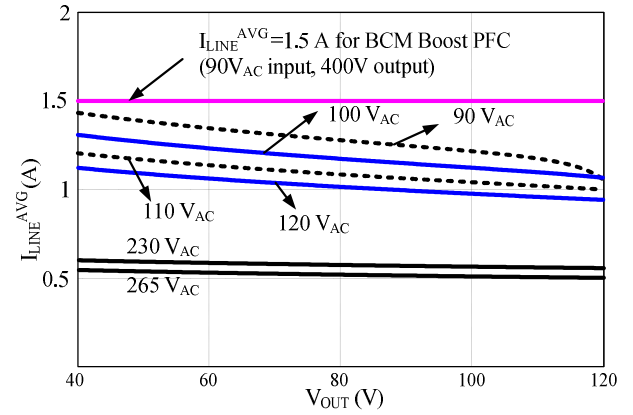

Fig. 9. Average line current of a single buck PFC converter as a function of output voltage for different line voltages (P_{OUT}=150W)

optimal selection of the output voltage is critical to maximize the efficiency.

Fig. 9 shows how the average line current varies with the output voltage and line voltages using (13). It can be observed that the average line current is smaller than that of the boost counterpart and decreases as the output voltage increases. It follows that the conduction loss in the bridge rectifier is smaller than that of the boost counterpart. Fig. 10 plots the average freewheeling diode current variation for different output and line voltages using (14). It can be observed that the average freewheeling diode current is larger than that of the boost counterpart and decreases as the output voltage increases. Since the average input current is much larger than the average freewheeling diode current and two diodes are involved in the conduction path of the bridge rectifier, the buck PFC has significantly lower conduction losses in the diodes than that of its boost counterpart in spite of the increased conduction loss of the freewheeling diode.

In summary, the conduction losses of the diodes can be minimized as the output voltage increases while the conduction loss of the MOSFET at the minimum line voltage
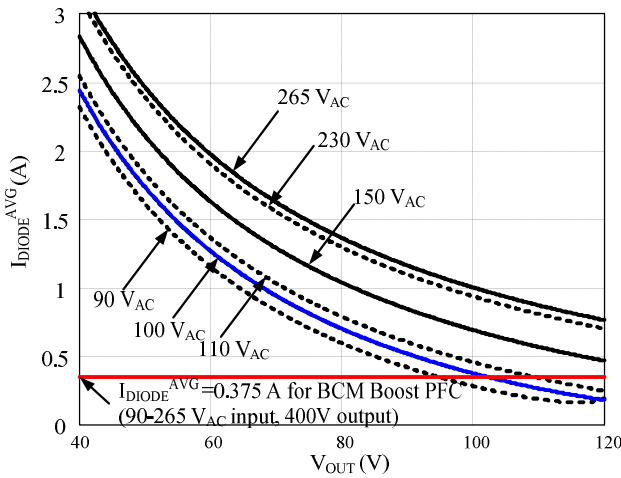
Fig. 10. Average freewheeling diode current of a single buck PFC converter as a function of output voltage for different line voltages (P_{OUT}=150W).

has its minimum value when the output voltage is around 80V.

IV. EXPERIMENTAL RESULTS

An interleaved BCM buck PFC prototype converter with 300 W of output power and a universal input range has been built using a BCM PFC controller (FAN9611), which was originally developed for interleaved BCM boost PFC converters [21], [22]. The output voltage is set at 80V so that the power dissipation of the MOSFET can be minimized. With a high voltage NPN transistor (Q3), a high voltage current source is implemented to level-shift the output voltage information to ground the referenced FB pin of the FNA9611. The schematic along with its key components is shown in Fig. 11. Fig. 12 and Fig. 13 show the key interleaving waveforms for the full load condition at 115V_{AC}. Fig. 14 shows the key interleaving waveforms for the full load condition at 230V_{AC}. To show the input current ripple cancellation by interleaving, the zoomed waveforms of Fig. 12 at around the peak of the line voltage are shown in Fig. 15. As can be observed, the ripple frequency of the sum of the two switch currents is doubled while the peak to peak of the ripple current is the same as that of one converter handling half of the output power.

Fig. 16 and 17 show the steady state operation waveforms under full load with 115 V_{AC} and 230 V_{AC} line input voltages, respectively. The measured waveform shows good agreement with the corresponding calculated line current waveform of Fig. 5. The line current is slightly distorted due to the circulating current through the line filter capacitor which leads the line voltage. The effect of the circulating current is more notable at high line where the input power is lower while the circulating current is larger than that of low line.
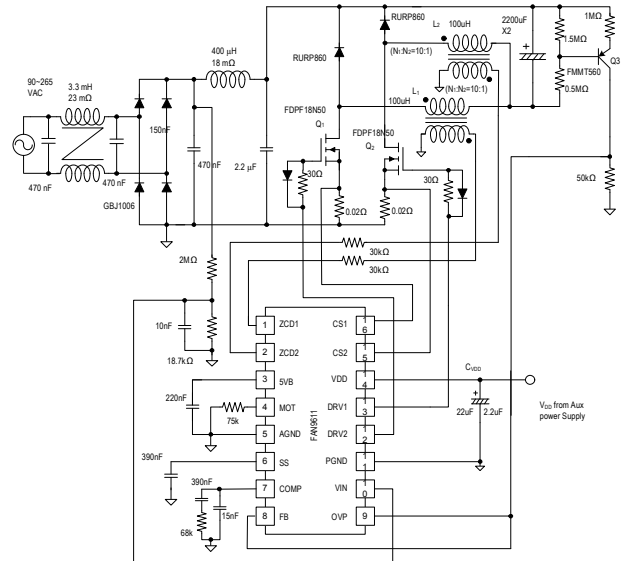

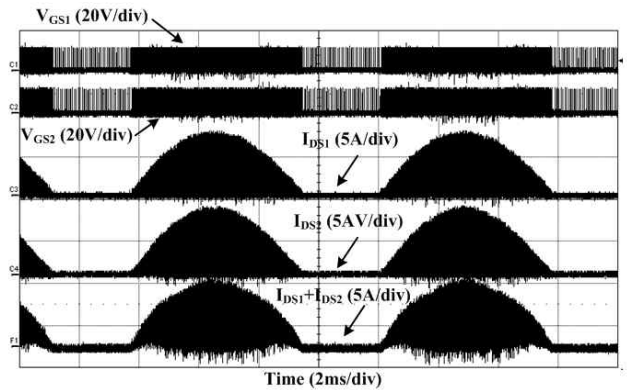Fig. 11. Schematic of prototype converter.

Fig. 12. Operation Waveforms at low line (P_{OUT}=300W, V_{IN}=115V_{AC}).

Fig. 18 shows how the efficiency varies with the line voltage for different load conditions. The measured efficiencies remain above 96% down to 25% of full load. Even at 10% of the full load condition, the efficiency remains above 94% across the entire line range due to the built-in phase management function of the FAN9611, which is designed to shut down one converter when the load drops below 15% of the full load. Without the phase management, the efficiency at a 10% load drops down to 90% at high line due to the high switching frequency. Fig. 19 shows the line current harmonics along with the IEC61000-3-2 (class D) standard, which shows a good agreement with the calculated harmonics shown in Fig. 4, Fig. 5 and Fig. 6 while meeting the IEC61000-3-2 specification. Fig. 20 shows the measured power factor. This shows that a high power factor above 96% is achieved under a full load for the entire line range with the proposed method.
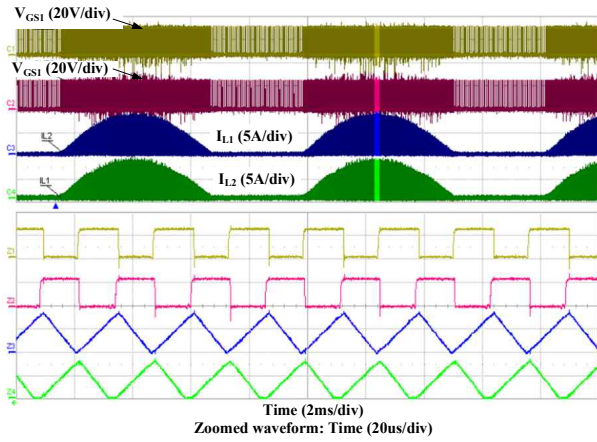
Fig. 13. Inductor Waveforms at low line (P$_{OUT}$=300W, V$_{IN}$=115V$_{AC}$).
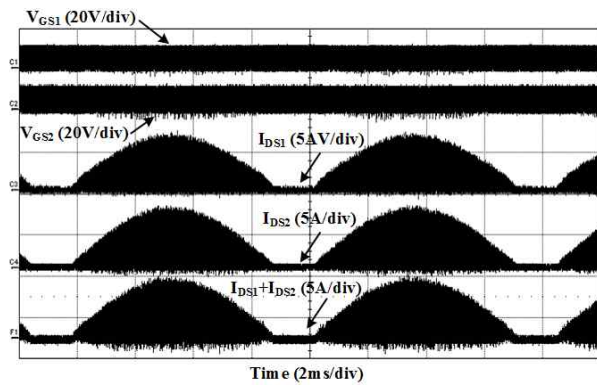

Fig. 14. Operation Waveforms at high line (P$_{OUT}$=300W, V$_{IN}$=230V$_{AC}$).
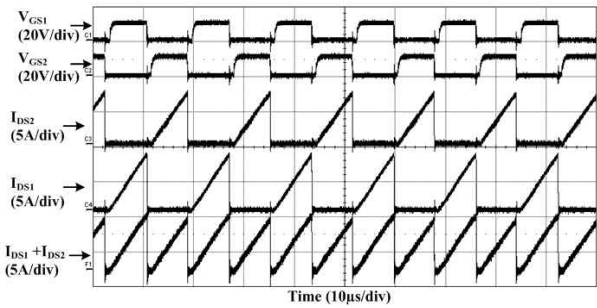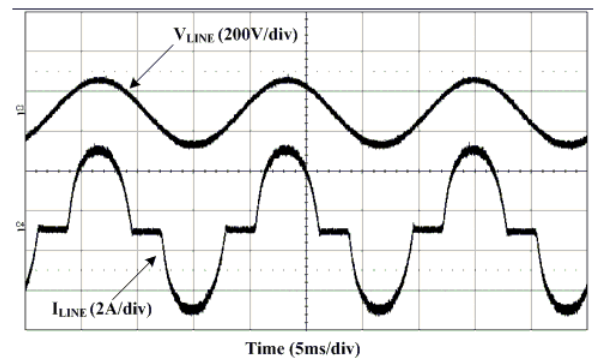

Fig.15. Current ripple cancellation by interleaving.

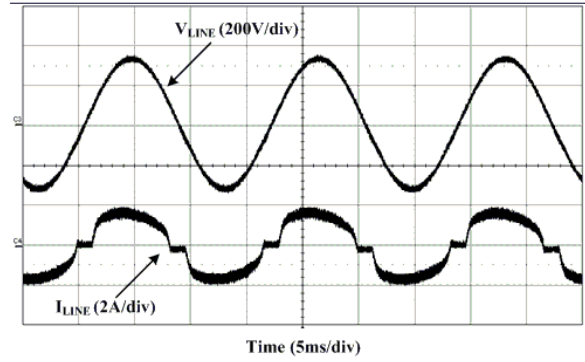Fig. 16. Line voltage and current waveforms (P$_{OUT}$=300W, V$_{IN}$=115V$_{AC}$).

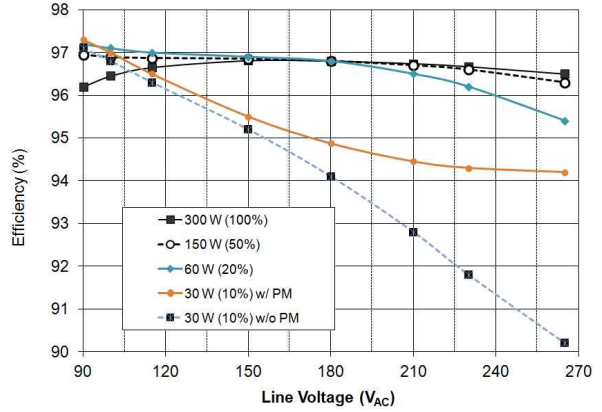Fig. 17. Line voltage and current waveforms (P$_{OUT}$=300W, V$_{IN}$=230V$_{AC}$).

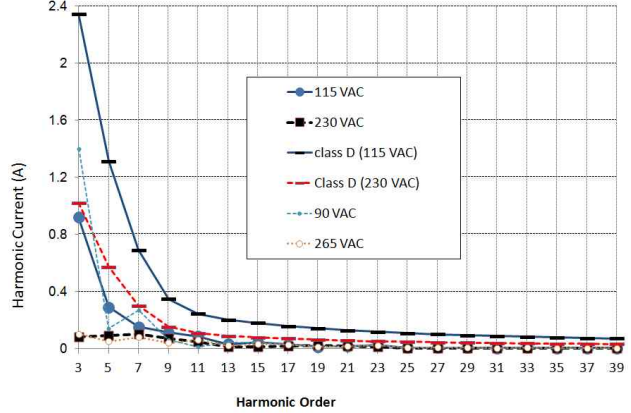Fig. 18. Measured efficiency .

Fig. 19. Measured line current harmonics and EN61000 class D limit.
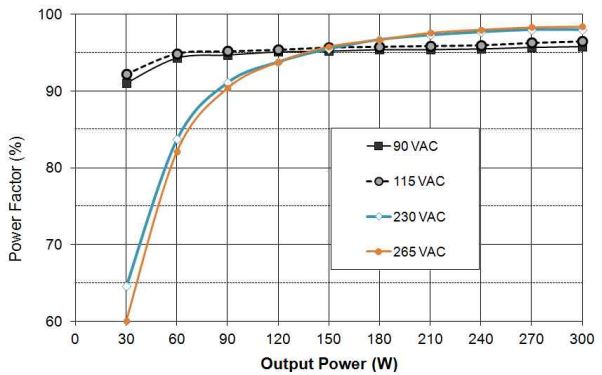

Fig. 20. Measured power factor.

V. CONCLUSIONS

This paper discussed the design consideration and conducted an in depth analysis for an interleaved boundary conduction mode power factor correction buck converter to examine the allowable voltage gain (K value) for meeting the EN61000-3-2, Class D standard while maximizing the efficiency. By interleaving two parallel connected buck converters, the input current ripple is halved while the ripple frequency is doubled, which leads to a smaller line filter. The smaller capacitor in the line filter also results in a smaller displacement factor of the line current which improves the power factor. The discussion about the optimal design meeting both the harmonic regulation and high efficiency was verified on a 300W, universal line experimental prototype with an 80V output. It exhibits a high efficiency above 96% down to 20% of the full load. Even at 10% of the full load, a high efficiency above 94% is achieved over the entire line range due to the phase management.

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