

# Non-isolated Bidirectional Soft-switching SEPIC/ZETA Converter with Reduced Ripple Currents

Min-Sup Song<sup>†</sup>, Young-Dong Son<sup>\*</sup>, and Kwang-Hyun Lee<sup>\*</sup>

<sup>†\*</sup>Central R&D Institute, Samsung Electro-Mechanics, Suwon, Korea

## Abstract

A novel non-isolated bidirectional soft-switching SEPIC/ZETA converter with reduced ripple currents is proposed and characterized in this study. Two auxiliary switches and an inductor are added to the original bidirectional SEPIC/ZETA components to form a new direct power delivery path between input and output. The proposed converter can be operated in the forward SEPIC and reverse ZETA modes with reduced ripple currents and increased voltage gains attributed to the optimized selection of duty ratios. All switches in the proposed converter can be operated at zero-current-switching turn-on and/or turn-off through soft current commutation. Therefore, the switching and conduction losses of the proposed converter are considerably reduced compared with those of conventional bidirectional SEPIC/ZETA converters. The operation principles and characteristics of the proposed converter are analyzed in detail and verified by the simulation and experimental results.

**Key words:** Bidirectional SEPIC/ZETA converter, Ripple current, Soft current commutation, Soft switching

## I. INTRODUCTION

Bidirectional DC–DC converters can manipulate bilateral power flow between two DC sources by using only a single-circuit structure. Therefore, the weight, volume, and cost of the overall system can be reduced by simplifying circuit composition [1]. These desirable features increased the use of bidirectional DC–DC converters in battery chargers/dischargers, fuel cell hybrid power systems, DC uninterruptible power supplies, and energy regenerative systems in automotive applications [2]–[9].

Non-isolated converters are simpler and more efficient than isolated converters and are thus preferred for use when galvanic isolation is unnecessary. The literature has reported on several non-isolated bidirectional DC–DC converters, such as bidirectional boost/buck-derived [10]–[13], Cuk [14], SEPIC/ZETA [15], multilevel [16], [17], and coupled-inductor type converters [18], [19]. Multiphase interleaved converters are often adopted to decrease voltage ripple and filter size by reducing the inductor current ripple components [20]–[22].

These converters can enhance circuit performance but may increase overall circuit system complexity. Control reliability may also deteriorate with increased interleaving phases.

Without using any interleaved techniques, unidirectional SEPIC and ZETA converters featuring reduced ripple currents have been proposed in [23], [24]. The converters consist of the original SEPIC or ZETA components in addition to an auxiliary diode and switch to form a new direct power delivery path between input and output. Inductor ripple currents and switching voltages of the main switch and diode can be reduced by shortening the duration of the original SEPIC or ZETA operation while extending the duration of the direct power link operation. However, these converters still possess hard-switching properties, and diodes particularly suffer from severe reverse recovery problem.

A new non-isolated bidirectional soft switching SEPIC/ZETA converter with reduced ripple currents is proposed to overcome these hard-switching problems. A small inductor is added to the auxiliary power delivery path, and diodes are replaced by active switches for bidirectional power flow control, as shown in the modified SEPIC topology in Fig. 1(a). With the use of a single-circuit structure, SEPIC and ZETA operations are implemented in the forward and reverse directions, respectively. Similar to the features of original bidirectional SEPIC/ZETA converters, both step-up and

Manuscript received Dec. 14, 2013; accepted May 21, 2014  
Recommended for publication by Associate Editor Dehong Xu.

<sup>†</sup>Corresponding Author: [minsung.song@samsung.com](mailto:minsung.song@samsung.com)

Tel: +82-31-300-4892, Samsung Electro-Mechanics

<sup>\*</sup>Central R&D Institute, Samsung Electro-Mechanics, Korea

step-down operations are available regardless of power conversion directions. A similar operation can be performed in the bilateral direction because of the duality between SEPIC and ZETA converters [23]–[25]. Through the use of constant frequency pulse-width modulation control, the proposed converter behaves in a manner similar to that of the original bidirectional SEPIC/ZETA converter when auxiliary switches are fully turned off. The converter can reduce inductor current ripples without employing interleaved methods. Thus, the DC resistive losses of inductors and capacitors, as well as the conduction and switching losses of switches, are reduced. The current rating of switches can be also reduced. Switches are operated at zero-current-switching (ZCS) turn-on and turn-off through soft current commutation between switches. Synchronous rectification and zero-voltage-switching (ZVS) are also achieved for synchronous rectifiers. Consequently, the overall power conversion efficiency of the proposed converter can be considerably increased compared with that of the original non-isolated bidirectional SEPIC/ZETA converter.

## II. OPERATION ANALYSIS OF THE PROPOSED CONVERTER

### A. Circuit Structure

The proposed converter can be divided into two parts, as shown in Fig. 2. The first part is the original non-isolated bidirectional SEPIC/ZETA converter consisting of inductors  $L_1$  and  $L_2$ , capacitors  $C_{in}$ ,  $C_s$ , and  $C_o$ , and switches  $S_1$  and  $S_2$ . The second part is an additional circuit consisting of switches  $S_3$  and  $S_4$ , as well as an inductor  $L_a$ . The additional circuit provides a new direct power delivery path between input and output. SEPIC and ZETA operations are implemented in the forward and reverse directions, respectively.

In SEPIC operation,  $S_1$  acts as the main switch,  $S_2$  is the synchronous rectifier, whereas  $S_3$  and  $S_4$  are the auxiliary switches. In ZETA operation,  $S_1$  conducts for the synchronous rectifier,  $S_2$  is the main switch, whereas  $S_3$  and  $S_4$  are the auxiliary switches.  $L_a$  induces the soft current transition between switches.

### B. Mode Analysis

In the proposed converter,  $L_a$  is considerably smaller than  $L_1$  and  $L_2$ . Therefore, following basic operation analysis ignores the effect of  $L_a$  and treats the proposed converter as a conventional hard-switching converter to simplify the analysis. The proposed converter has three distinct operation modes in SEPIC and ZETA operations during each switching cycle. The operation waveforms for the forward SEPIC mode are shown in Fig. 3.

**Mode 1** [ $t_0$ – $t_1$ ]: From  $t_0$  to  $t_1$ , only  $S_1$  conducts while the other switches are idle. The average inductor voltage is zero at steady state. Thus, the voltage of  $C_s$  is equal to the input voltage  $V_{in}$  [26]. Voltages across  $L_1$  ( $v_{L1}$ ) and  $L_2$  ( $v_{L2}$ ) are both

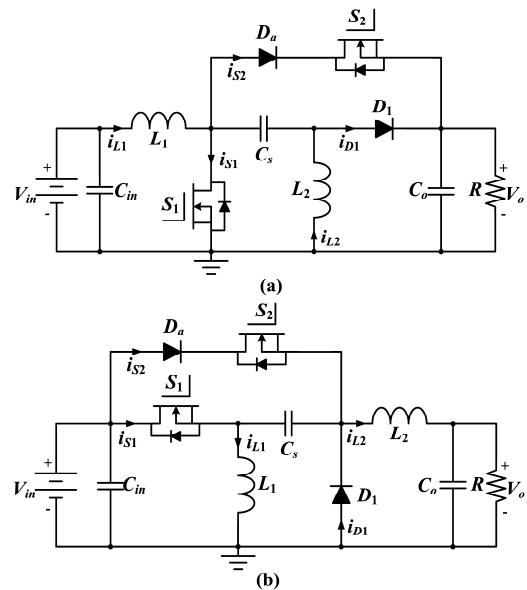


Fig. 1. Unidirectional (a) SEPIC and (b) ZETA converters with reduced ripple currents.

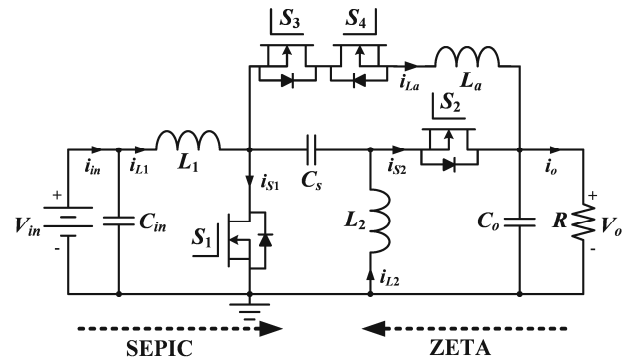


Fig. 2. Circuit structure of the proposed converter.

equal to  $V_{in}$ . Currents through  $L_1$  ( $i_{L1}$ ) and  $L_2$  ( $i_{L2}$ ) increase with slopes of  $V_{in}/L_1$  and  $V_{in}/L_2$ , respectively. The current flowing through  $S_1$  ( $i_{S1}$ ) is the sum of  $i_{L1}$  and  $i_{L2}$ . The drain-source voltages of  $S_1$  ( $v_{S1}$ ) and  $S_2$  ( $v_{S2}$ ) are 0 V and  $V_{in} + V_o$ , respectively, where  $V_o$  is output voltage. At the beginning of this mode, the capacitor charging current flows from the  $V_o$  terminal to  $S_1$  through the output capacitor of  $S_3$  and the body diode of  $S_4$ . Therefore, the drain-source voltages of  $S_3$  ( $v_{S3}$ ) and  $S_4$  ( $v_{S4}$ ) become  $V_o$  and 0 V, respectively.  $S_4$  should then be switched off after  $t_0$  to satisfy the continuity of inductor currents.

**Mode 2** [ $t_1$ – $t_2$ ]: From  $t_1$  to  $t_2$ , only  $S_2$  conducts and the other switches are idle. The source voltage of  $S_2$  is  $V_o$ . Thus,  $v_{L1}$  and  $v_{L2}$  are both  $-V_o$ .  $i_{L1}$  and  $i_{L2}$  decrease with slopes of  $-V_o/L_1$  and  $-V_o/L_2$ , respectively. The current through  $S_2$  ( $i_{S2}$ ) is the sum of  $i_{L1}$  and  $i_{L2}$ . At the beginning of this mode, the voltage difference between the drain voltage of  $S_1$  ( $V_{in} + V_o$ ) and the  $V_o$  terminal induces capacitor charging current to flow through the auxiliary current path. Assuming that output capacitances of  $S_3$  and  $S_4$  are the same, the voltage difference equally charges the

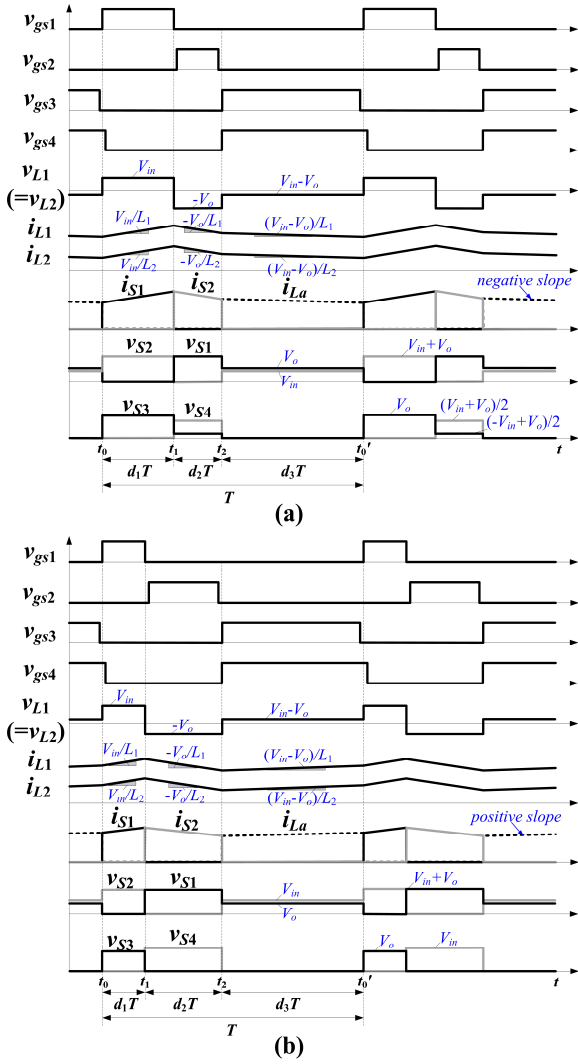


Fig. 3. SEPIC operation waveforms of the proposed converter in (a) step-up and (b) step-down operations.

output capacitors of  $S_3$  and  $S_4$  through  $V_{in}/2$ . Simultaneously,  $v_{S3}$ , which was  $V_o$  in the former Mode 1, also equally charges the output capacitors of  $S_3$  and  $S_4$ . Given the charging polarities, the overall  $v_{S3}$  and  $v_{S4}$  respectively become  $(-V_{in}+V_o)/2$  and  $(V_{in}+V_o)/2$  in the step-up operation and 0 V and  $V_{in}$  in the step-down operation.

$S_2$  can be switched on after  $t_1$  and switched off before  $t_2$ . Thus, synchronous rectification and ZVS can be achieved.

**Mode 3** [ $t_2-t_0'$ ]: Between  $t_2$  and  $t_0'$ ,  $S_3$  and  $S_4$  conduct, whereas  $S_1$  and  $S_2$  do not conduct. This mode is added to the conventional SEPIC/ZETA converter to provide an additional power delivery path between input and output. This path enhances the performance of the proposed converter. As  $v_{S1}$  is  $V_o$ ,  $v_{S2}$  becomes  $V_{in}$ . Therefore, both  $v_{L1}$  and  $v_{L2}$  are  $V_{in}-V_o$ , and both  $v_{S3}$  and  $v_{S4}$  are 0 V.  $i_{L1}$  and  $i_{L2}$  have slopes of  $(V_{in}-V_o)/L_1$  and  $(V_{in}-V_o)/L_2$ , respectively. These slope change values of inductors are considerably smaller than those of inductors in previous modes. Consequently, inductor ripple currents can

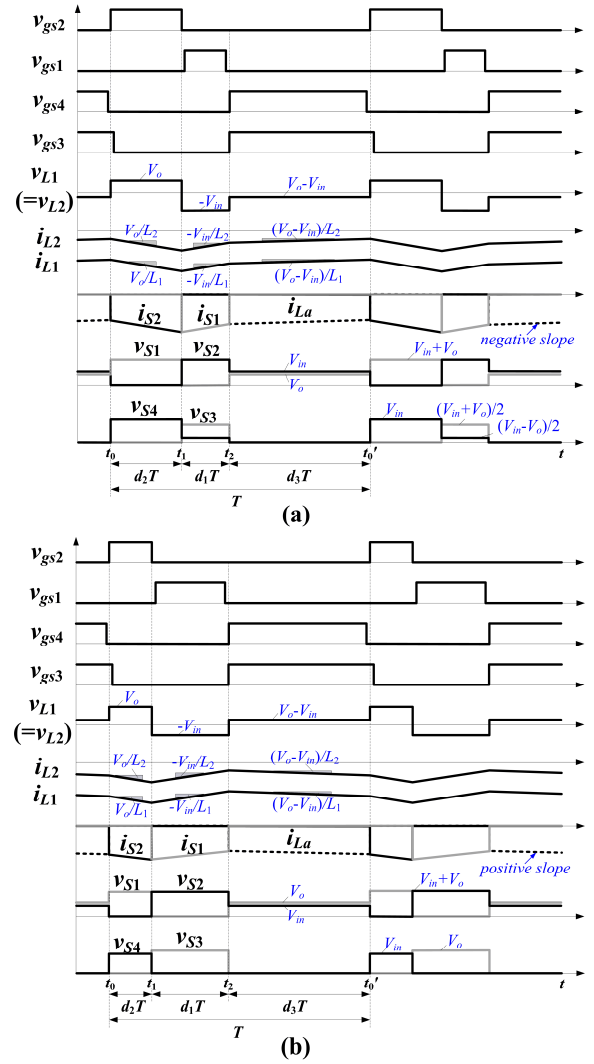


Fig. 4. ZETA operation waveforms of the proposed converter in (a) step-up and (b) step-down operations.

be considerably reduced. The current through  $S_3$  and  $S_4$  ( $i_{La}$ ) is the sum of  $i_{L1}$  and  $i_{L2}$ . Therefore,  $i_{L1}$ ,  $i_{L2}$ , and  $i_{La}$  have negative slopes during the step-up operation but positive slopes during the step-down operation.  $S_3$  should be switched off before  $t_0'$  to prevent the reverse short current from the  $V_o$  terminal to ground through the auxiliary current path and  $S_1$ .

Reverse ZETA operation waveforms are shown in Fig. 4.

The negative polarity of  $i_{L1}$  and  $i_{L2}$  indicates reverse power flow in ZETA operation. The principle of the ZETA operation of the proposed converter is similar to that of the SEPIC operation because of the duality between SEPIC and ZETA converters. Therefore, the specific analysis for ZETA operation is omitted in this study.

### C. Conversion Ratio

By using the voltage-time balance principle and assuming 100% power conversion efficiency, we can determine the voltage and current conversion ratios of the proposed converter as

$$M = \frac{V_o}{V_{in}} = \frac{I_{in}}{I_o} = \frac{T - t_{S2}}{T - t_{S1}} = \frac{1 - d_2}{1 - d_1} \quad (1)$$

where  $I_{in}$  and  $I_o$  refer to input and output currents, respectively; and  $t_{S1}$  and  $t_{S2}$  correspond to the duration of  $S_1$  and  $S_2$ , respectively. Switching duty ratios  $d_1$  and  $d_2$  are given by  $d_1 = t_{S1}/T$  and  $d_2 = t_{S2}/T$ , where  $T$  is repeated switching period;  $d_1$  must be larger than  $d_2$  to increase output voltage and vice versa. The power conversion efficiency of the proposed converter increases as  $d_1$  and  $d_2$  become smaller because the low ripple current effect of Mode 3 can be maximized with considerably reduced overall circulation currents. As a result, conduction and switching losses of switches and DC resistive losses of inductors and capacitors can be reduced.

### III. DESIGN PARAMETERS

Useful design parameters are presented in this section.  $L_a$  is ignored to simplify the design. To maximize the ripple reduction effect of the proposed converter,  $d_1$  and  $d_2$  should be minimized, whereas  $d_3$  has to be maximized. In this work,  $d_3$  ( $=1-d_1-d_2$ ) denotes the duty ratio of  $S_3$  and  $S_4$ . In SEPIC operation, duty ratios can be determined as

$$\begin{aligned} \text{step-up} : d_1 &= 1 - (1 - d_2)/M \quad (d_2 : \text{minimum}) \\ \text{step-down} : d_2 &= 1 - (1 - d_1) \cdot M \quad (d_1 : \text{minimum}) \end{aligned} \quad (2)$$

In ZETA operation, duty ratios are determined by

$$\begin{aligned} \text{step-up} : d_2 &= 1 - (1 - d_1) \cdot M \quad (d_1 : \text{minimum}) \\ \text{step-down} : d_1 &= 1 - (1 - d_2)/M \quad (d_2 : \text{minimum}) \end{aligned} \quad (3)$$

where  $M$  is voltage conversion ratio defined in (1).

For the proposed converter, inductor ripple current reaches the maximum value between  $V_{in}d_1T/L$  and  $V_o d_2 T/L$ , where  $L$  is  $L_1$  or  $L_2$ . This formula can be also applied to conventional SEPIC converters. However, the ripple value in the proposed converter is smaller than that of the conventional SEPIC converter because of the reduction in  $d_1$  and  $d_2$ . The inflection points of inductor currents, such as  $i_{L1}(t_0)$ ,  $i_{L1}(t_1)$ ,  $i_{L1}(t_2)$ ,  $i_{L2}(t_0)$ ,  $i_{L2}(t_1)$ , and  $i_{L2}(t_2)$  (Fig. 3), are defined as  $I_1$ ,  $I_2$ ,  $I_3$ ,  $I_4$ ,  $I_5$ , and  $I_6$ , respectively. These currents are related to one another as follows:

$$\begin{aligned} I_1 &= i_{L1}(t_0) \\ I_2 &= i_{L1}(t_1) = I_1 + \frac{V_{in}d_1T}{L_1} \\ I_3 &= i_{L1}(t_2) = I_1 + \frac{V_{in}d_1 - V_o d_2 T}{L_1} \\ I_4 &= i_{L2}(t_0) \\ I_5 &= i_{L2}(t_1) = I_4 + \frac{V_{in}d_1T}{L_2} \\ I_6 &= i_{L2}(t_2) = I_4 + \frac{V_{in}d_1 - V_o d_2 T}{L_2} \end{aligned} \quad (4)$$

$$\quad (5)$$

The average of  $i_{L1}$  is equal to  $I_{in}$  as

$$I_{in} = i_{L1,avg} = \frac{1}{2}((I_1 + I_2) \cdot d_1 + (I_2 + I_3) \cdot d_2 + (I_3 + I_1) \cdot d_3) \quad (6)$$

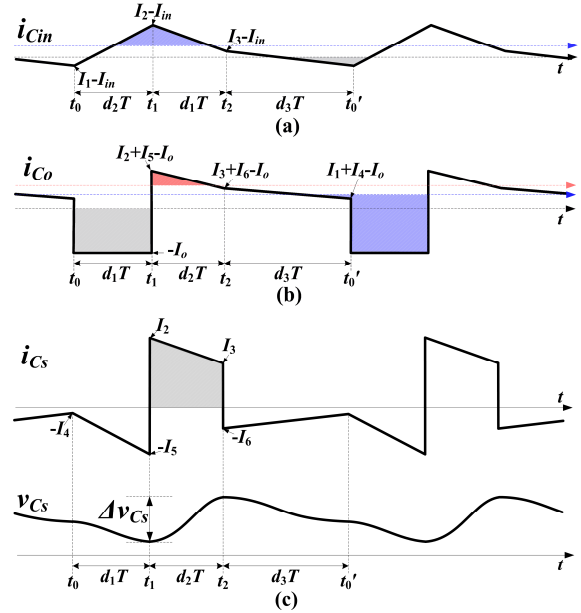


Fig. 5. Typical capacitor currents of the proposed converter in step-up mode (a)  $i_{Cin}$ , (b)  $i_{Co}$ , and (c)  $i_{Cs}$ .

By substituting (4) into (6) and using (1),  $I_1$  is obtained by

$$I_1 = I_{in} - (d_1 - d_2 d_3) \cdot \frac{V_{in} T}{2L_1} \quad (7)$$

The charge balance of  $C_s$  states is as follows:

$$-(I_4 + I_5) \cdot d_1 + (I_2 + I_3) \cdot d_2 - (I_6 + I_4) \cdot d_3 = 0 \quad (8)$$

Substituting (4) and (5) into (8) and using (1) and (7),  $I_4$  is obtained by

$$I_4 = \frac{d_2}{1 - d_2} I_{in} + \frac{d_1 d_2 d_3}{1 - d_1} \cdot \frac{V_{in} T}{2L_1} - \frac{d_1 d_2 + d_1 d_3 - d_2 d_3}{1 - d_1} \cdot \frac{V_{in} T}{2L_2} \quad (9)$$

All other inflection values in (4) and (5) can be determined by using (7) and (9). For the ZETA operation, the same method can be applied to derive the inflection points of inductor currents. Given these values, other design parameters, such as inductor average currents, switch peak and root-mean-square (rms) currents, capacitor ripple voltages, and rms currents, can be determined through simple algebra. Typical capacitor currents of the proposed converter in step-up mode are shown in Fig. 5, where  $i_{Cin}$ ,  $i_{Co}$ , and  $i_{Cs}$  are currents of  $C_{in}$ ,  $C_o$ , and  $C_s$ , respectively. To calculate the capacitor ripple voltage, the capacitor charge can be obtained from the local maximum area enclosed by the capacitor current and time axis, and then divided into its capacitance such as  $C_{in}$ ,  $C_o$ , or  $C_s$ . The capacitor ripple voltage can have several different values according to the operating conditions. The major design parameters of the proposed converter are summarized in Table I. The detailed derivations are omitted to save the space in this paper.

### IV. ACTUAL CONVERSION RATIO AND EFFICIENCY CONSIDERING RESISTIVE LOSSES

An equivalent circuit for the proposed converter containing

TABLE I  
 SEVERAL DESIGN PARAMETERS OF THE PROPOSED CONVERTER

	SEPIC mode	ZETA mode
<b>Conversion ratio</b>	$M = \frac{V_o}{V_{in}} = \frac{I_m}{I_o} = \frac{1-d_2}{1-d_1}$	
<b>Duty ratio selection</b>	$d_1 = 1 - (1-d_2)/M$ (where, $d_2$ is minimum) $d_2 = 1 - (1-d_1) \cdot M$ (where, $d_1$ is minimum)	$d_2 = 1 - (1-d_1) \cdot M$ (where, $d_1$ is minimum) $d_1 = 1 - (1-d_2)/M$ (where, $d_2$ is minimum)
<b>Inductor ripple current</b>	$\Delta i_L = \max\left(\frac{V_{in}d_1T}{L}, \frac{V_o d_2 T}{L}\right)$	
<b>Inflection points of inductor currents</b>	$I_1 = i_{L1}(t_0) = I_m - (d_1 - d_2 d_3) \cdot \frac{V_{in} T}{2L_1}$ $I_2 = i_{L1}(t_1) = I_1 + \frac{V_{in}}{L_1} d_1 T$ $I_3 = i_{L1}(t_2) = I_1 + \frac{(V_{in} d_1 - V_o d_2)}{L_1} T$ $I_4 = i_{L2}(t_0) = \frac{d_2}{1-d_2} I_m + \frac{d_1 d_2 d_3}{1-d_1} \cdot \frac{V_{in} T}{2L_1} - \frac{d_1 d_2 + d_1 d_3 - d_2 d_3}{1-d_1} \cdot \frac{V_{in} T}{2L_2}$ $I_5 = i_{L2}(t_1) = I_4 + \frac{V_{in}}{L_2} d_1 T$ $I_6 = i_{L2}(t_2) = I_4 + \frac{(V_{in} d_1 - V_o d_2)}{L_2} T$	$I_1 = i_{L1}(t_0) = I_m - (d_2 - d_1 d_3) \cdot \frac{V_o T}{2L_1}$ $I_2 = i_{L1}(t_1) = I_1 + \frac{V_o}{L_1} d_2 T$ $I_3 = i_{L1}(t_2) = I_1 + \frac{(V_o d_2 - V_{in} d_1)}{L_1} T$ $I_4 = i_{L2}(t_0) = \frac{d_2}{1-d_2} I_m + \frac{d_1 d_2 d_3}{1-d_1} \cdot \frac{V_{in} T}{2L_1} - \frac{d_1 d_2 + d_2 d_3 - d_1 d_3}{1-d_1} \cdot \frac{V_{in} T}{2L_2}$ $I_5 = i_{L2}(t_1) = I_4 + \frac{V_o}{L_2} d_2 T$ $I_6 = i_{L2}(t_2) = I_4 + \frac{(V_o d_2 - V_{in} d_1)}{L_2} T$
<b>Inductor average currents</b>	$\langle i_{L1} \rangle = I_m$ $\langle i_{L2} \rangle = I_m \frac{d_2}{1-d_2} = I_o \frac{d_2}{1-d_1}$ (approximation) $= \frac{1}{2}(d_1(I_4 + I_5) + d_2(I_3 + I_6) + d_3(I_6 + I_4))$ (real)	$\langle i_{L1} \rangle = I_m$ $\langle i_{L2} \rangle = I_m \frac{d_2}{1-d_2} = I_o \frac{d_2}{1-d_1}$ (approximation) $= \frac{1}{2}(d_2(I_4 + I_5) + d_1(I_3 + I_6) + d_3(I_6 + I_4))$ (real)
<b>Inductor rms currents</b>	$I_{L1,rms} = \sqrt{\frac{1}{3}[d_1(I_1^2 + I_1 I_2 + I_2^2) + d_2(I_2^2 + I_2 I_3 + I_3^2) + d_3(I_3^2 + I_3 I_4 + I_4^2)]}$ $I_{L2,rms} = \sqrt{\frac{1}{3}[d_1(I_4^2 + I_4 I_5 + I_5^2) + d_2(I_5^2 + I_5 I_6 + I_6^2) + d_3(I_6^2 + I_6 I_4 + I_4^2)]}$	$I_{L1,rms} = \sqrt{\frac{1}{3}[d_2(I_1^2 + I_1 I_2 + I_2^2) + d_1(I_2^2 + I_2 I_3 + I_3^2) + d_3(I_3^2 + I_3 I_4 + I_4^2)]}$ $I_{L2,rms} = \sqrt{\frac{1}{3}[d_2(I_4^2 + I_4 I_5 + I_5^2) + d_1(I_5^2 + I_5 I_6 + I_6^2) + d_3(I_6^2 + I_6 I_4 + I_4^2)]}$
<b>Switch peak currents</b>	$I_{S1,pk} = I_{S2,pk} = I_2 + I_5, \quad I_{S3,pk} = I_{S4,pk} = \max(I_1 + I_4, I_3 + I_6)$	
<b>Switch peak voltages</b>	$V_{S1,pk} = V_{S2,pk} = V_{in} + V_o, \quad V_{S3,pk} = V_{S4,pk} = \max(V_{in}, V_o)$	
<b>Switch rms currents</b>	$I_{S1,rms} = \sqrt{\frac{d_1}{3}[(I_1 + I_4)^2 + (I_1 + I_4) \cdot (I_2 + I_5) + (I_2 + I_5)^2]}$ $I_{S2,rms} = \sqrt{\frac{d_2}{3}[(I_2 + I_5)^2 + (I_2 + I_5) \cdot (I_3 + I_6) + (I_3 + I_6)^2]}$ $I_{S3,rms} = \sqrt{\frac{d_3}{3}[(I_3 + I_6)^2 + (I_3 + I_6) \cdot (I_1 + I_4) + (I_1 + I_4)^2]}$	$I_{S1,rms} = \sqrt{\frac{d_1}{3}[(I_2 + I_5)^2 + (I_2 + I_5) \cdot (I_3 + I_6) + (I_3 + I_6)^2]}$ $I_{S2,rms} = \sqrt{\frac{d_2}{3}[(I_1 + I_4)^2 + (I_1 + I_4) \cdot (I_2 + I_5) + (I_2 + I_5)^2]}$ $I_{S3,rms} = \sqrt{\frac{d_3}{3}[(I_3 + I_6)^2 + (I_3 + I_6) \cdot (I_1 + I_4) + (I_1 + I_4)^2]}$
<b>Capacitor ripple voltages</b>	$A_{V_{in}}$	$ZETA$ Step-up case ( $d_2 > d_1$ ) $\begin{cases} \frac{(1+d_3) \cdot (d_2 + d_1 d_3)^2 V_o T^2}{8L_1 C_{in} \cdot (1-d_1)} & \text{for } I_3 - I_m < 0 (d_2 d_3 < d_1) \\ \frac{(1-d_1) \cdot (d_2 - d_1 d_3)^2 V_o T^2}{8L_1 C_{in} \cdot (d_2 - d_1)} & \text{for } I_3 - I_m > 0 (d_2 d_3 > d_1) \end{cases}$
	$A_{V_o}$	$SEPIC$ Step-up case ( $d_1 > d_2$ ) $\begin{cases} \frac{I_o d_1 T}{C_o} & \text{for } I_1 + I_4 > I_o \\ \frac{I_o d_1 T}{C_o} + \frac{L_e}{2C_o V_o} \frac{1-d_2}{d_1 - d_2} \left( -\frac{d_1}{1-d_1} I_o + \frac{V_{in} T}{2L_e} \frac{d_1 d_2 + d_1 d_3 - d_2 d_3}{1-d_1} \right)^2 & \text{for } I_1 + I_4 < I_o < I_3 + I_6 \\ \frac{L_e}{2C_o V_o} \left( \frac{d_1}{1-d_1} I_o + \frac{V_{in} T}{2L_e} \frac{d_1 d_2 + d_2 d_3 + d_3 d_1}{1-d_1} \right)^2 & \text{for } I_3 + I_6 < I_o \end{cases}$
	$A_{V_{Cs}}$	$SEPIC$ Step-down case ( $d_1 < d_2$ ) $\begin{cases} \frac{I_o d_1 T}{C_o} & \text{for } I_3 + I_6 > I_o \\ \max \left[ \frac{L_e}{2C_o V_o} \left( \frac{d_1}{1-d_1} I_o + \frac{V_{in} T}{2L_e} \frac{d_1 d_2 + d_2 d_3 + d_3 d_1}{1-d_1} \right)^2, \frac{L_e(1-d_1)}{2C_o V_o (d_2 - d_1)} \left( -\frac{d_1}{1-d_1} I_o + \frac{V_{in} T}{2L_e} \frac{d_1 d_2 + d_2 d_3 - d_1 d_3}{1-d_1} \right)^2 \right] & \text{for } I_3 + I_6 < I_o < I_1 + I_4 \\ \frac{L_e}{2C_o V_o} \left( \frac{d_1}{1-d_1} I_o + \frac{V_{in} T}{2L_e} \frac{d_1 d_2 + d_2 d_3 + d_3 d_1}{1-d_1} \right)^2 & \text{for } I_1 + I_4 < I_o \end{cases}$ , where $L_e = \frac{L_1 L_2}{L_1 + L_2}$
	$A_{V_{Cs}}$	$\frac{1}{C_S} (I_m d_2 T + \frac{V_o T^2 d_1 d_2 d_3}{2L_1})$
<b>Capacitor rms currents</b>	$I_{C_{in},rms} = \sqrt{\frac{1}{3}[d_2(I_1^2 + I_1 I_2 + I_2^2) + d_1(I_2^2 + I_2 I_3 + I_3^2) + d_3(I_3^2 + I_3 I_4 + I_4^2)]} - I_m$ ( $I_1 - I_6$ for ZETA mode)	
	$I_{C_o,rms} = \sqrt{\frac{1}{3}[d_1(I_2 + I_5)^2 + (I_2 + I_5) \cdot (I_3 + I_6) + (I_3 + I_6)^2] + d_3[(I_3 + I_6)^2 + (I_3 + I_6) \cdot (I_1 + I_4) + (I_1 + I_4)^2]} - I_o$ ( $I_1 - I_6$ for SEPIC mode)	
	$I_{C_S,rms} = \sqrt{\frac{1}{3}[d_1(I_4^2 + I_4 I_5 + I_5^2) + d_2(I_5^2 + I_5 I_6 + I_6^2) + d_3(I_6^2 + I_6 I_4 + I_4^2)]}$	$\sqrt{\frac{1}{3}[d_2(I_1^2 + I_1 I_2 + I_2^2) + d_1(I_2^2 + I_2 I_3 + I_3^2) + d_3(I_3^2 + I_3 I_4 + I_4^2)]}$

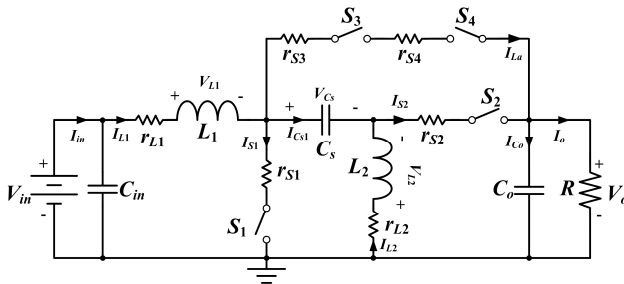


Fig. 6. Equivalent circuit of proposed converter containing resistive elements of inductors and switches.

resistive elements of inductors and switches is shown in Fig. 6.  $r_{L1}$  and  $r_{L2}$  represent the equivalent series resistance of  $L_1$  and  $L_2$ , respectively.  $r_{S1}$ ,  $r_{S2}$ ,  $r_{S3}$ , and  $r_{S4}$  denote the on-state drain-source resistance of  $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ , respectively. The conversion ratio and efficiency, with the resistive loss elements included, can be determined by using the methodology in [27]. The conversion ratio and efficiency of the proposed converter's forward SEPIC operation can be derived as follows: Because the average inductor voltage is zero, the average voltage of  $C_s$  ( $V_{Cs}$ ) is obtained by

$$V_{Cs} = V_{in} - I_{L1} \cdot r_{L1} + I_{L2} \cdot r_{L2} \quad (10)$$

where  $I_{L1}$  and  $I_{L2}$  are the average values of  $i_{L1}$  and  $i_{L2}$  over one switching period, respectively, at steady state. When  $S_1$  is turned on and the others are turned off, the average values of  $v_{L1}$ ,  $v_{L2}$ ,  $i_{Co}$ , and  $i_{Cs}$  are given by

$$V_{L1}^{d1} = V_{L2}^{d1} = V_{in} - I_{L1} \cdot r_{L1} - (I_{L1} + I_{L2}) \cdot r_{S1} \quad (11)$$

$$I_{Co}^{d1} = -\frac{V_o}{R} \quad (12)$$

$$I_{Cs}^{d1} = -I_{L2} \quad (13)$$

where  $R$  denotes load resistance. When  $S_2$  is turned on and the others are turned off, the average values of  $v_{L1}$ ,  $v_{L2}$ ,  $i_{Co}$ , and  $i_{Cs}$  are obtained as

$$V_{L1}^{d2} = V_{L2}^{d2} = -V_o - I_{L2} \cdot r_{L2} - (I_{L1} + I_{L2}) \cdot r_{S2} \quad (14)$$

$$I_{Co}^{d2} = I_{L1} + I_{L2} - \frac{V_o}{R} \quad (15)$$

$$I_{Cs}^{d2} = I_{L1} \quad (16)$$

When  $S_3$  and  $S_4$  are turned on and the others are idle, the average values of  $v_{L1}$ ,  $v_{L2}$ ,  $i_{Co}$ , and  $i_{Cs}$  are given as

$$V_{L1}^{d3} = V_{L2}^{d3} = V_{in} - V_o - I_{L1} \cdot r_{L1} - (I_{L1} + I_{L2}) \cdot (r_{S3} + r_{S4}) \quad (17)$$

$$I_{Co}^{d3} = I_{L1} + I_{L2} - \frac{V_o}{R} \quad (18)$$

$$I_{Cs}^{d3} = -I_{L2} \quad (19)$$

By applying ampere-time balance on  $C_o$  and  $C_s$ , the following equations are obtained:

$$I_{Co}^{d1} \cdot d_1 + I_{Co}^{d2} \cdot d_2 + I_{Co}^{d3} \cdot d_3 = 0 \quad (20)$$

$$I_{Cs}^{d1} \cdot d_1 + I_{Cs}^{d2} \cdot d_2 + I_{Cs}^{d3} \cdot d_3 = 0 \quad (21)$$

Substituting (12), (15), and (18) into (20),  $I_{L1} + I_{L2}$  is given by

$$I_{L1} + I_{L2} = \frac{V_o}{R} \cdot \frac{1}{1-d_1} \quad (22)$$

Substituting (13), (16), and (19) into (21),  $I_{L2}$  is related with  $I_{L1}$  as follows:

$$I_{L2} = I_{L1} \cdot \frac{d_2}{1-d_2} \quad (23)$$

Substituting (23) into (22),  $I_{L1}$  and  $I_{L2}$  are obtained as

$$I_{L1} = I_{in} = \frac{V_o}{R} \cdot \frac{1-d_2}{1-d_1} \quad (24)$$

$$I_{L2} = \frac{V_o}{R} \cdot \frac{d_2}{1-d_1} \quad (25)$$

By using the voltage-time balance principle on  $L_1$ ,

$$V_{L1}^{d1} \cdot d_1 + V_{L1}^{d2} \cdot d_2 + V_{L1}^{d3} \cdot d_3 = 0 \quad (26)$$

By substituting (11), (14), (17), (24), and (25) into (26), the actual voltage gain is given by

$$\frac{V_o}{V_{in}} = \frac{1-d_2}{1-d_1} \cdot \frac{R(1-d_1)^2}{R(1-d_1)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4}) \cdot d_3} \quad (27)$$

Efficiency is obtained by

$$\eta = \frac{P_o}{P_{in}} = \frac{V_o^2/R}{V_{in}I_{in}} = \frac{R(1-d_1)^2}{R(1-d_1)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4}) \cdot d_3} \quad (28)$$

The conversion ratio and efficiency of the reverse ZETA operation of the proposed converter can be also derived by using the same procedure as above. The results are summarized, and the actual voltage gain for the ZETA operation is given by

$$\frac{V_{in}}{V_o} = \frac{1-d_1}{1-d_2} \cdot \frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4}) \cdot d_3} \quad (29)$$

Efficiency is given as

$$\eta = \frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}d_1 + r_{S2}d_2 + (r_{S3} + r_{S4}) \cdot d_3} \quad (30)$$

The actual conversion ratio and efficiency of the conventional bidirectional SEPIC/ZETA converter can be obtained by removing the auxiliary current paths; thus,  $d_3 = 0$  and  $d_2 = 1-d_1$ . For a forward SEPIC operation of the conventional SEPIC/ZETA converter, the actual voltage conversion ratio is obtained as

$$\frac{V_o}{V_{in}} = \frac{d_1}{1-d_1} \cdot \frac{R(1-d_1)^2}{R(1-d_1)^2 + r_{L1}d_1^2 + r_{L2}(1-d_1)^2 + r_{S1}d_1 + r_{S2}(1-d_1)} \quad (31)$$

Efficiency is given by

$$\eta = \frac{R(1-d_1)^2}{R(1-d_1)^2 + r_{L1}d_1^2 + r_{L2}(1-d_1)^2 + r_{S1}d_1 + r_{S2}(1-d_1)} \quad (32)$$

For a reverse ZETA operation of the conventional SEPIC/ZETA converter, the actual voltage conversion ratio is obtained as

$$\frac{V_{in}}{V_o} = \frac{d_2}{1-d_2} \cdot \frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}(1-d_2) + r_{S2}d_2} \quad (33)$$

Efficiency is derived by

$$\eta = \frac{R(1-d_2)^2}{R(1-d_2)^2 + r_{L1}(1-d_2)^2 + r_{L2}d_2^2 + r_{S1}(1-d_2) + r_{S2}d_2} \quad (34)$$

To compare the actual voltage gains between the proposed converter and the conventional bidirectional SEPIC/ZETA converter, the following values of resistance are assumed and substituted into (27), (29), (31), and (33):

$$r_{L1}=r_{L2}=10\text{m}\Omega, r_{S1}=r_{S2}=r_{S3}=r_{S4}=5\text{m}\Omega, R=0.9\Omega.$$

The actual voltage gains calculated for the proposed converter and conventional SEPIC/ZETA converter in step-up and step-down modes are shown in Figs. 7(a) and 7(b), respectively. In the proposed converter, the selected duty ratio of the synchronous rectifier ( $d_2$  and  $d_1$  for SEPIC and ZETA operations, respectively) is as small as 0.1 for the step-up mode. For the step-down mode, the selected duty ratio of the main switch ( $d_1$  for SEPIC operation and  $d_2$  for ZETA operation) is sufficiently small by 0.1. These values are not dependent on the other duty ratios in contrast to the values of the conventional SEPIC/ZETA converter. As a result of such design freedom, the voltage gains of the proposed converter in both the step-up and step-down modes can be higher than those of the conventional SEPIC/ZETA converter at the same duty ratio. The duty ratios  $d_1$  and  $d_2$  can also be widely ranged in the proposed converter than in the conventional one.

The efficiencies of the proposed and conventional bidirectional SEPIC/ZETA converters are calculated, assuming the following parameters:

*Step-up:*  $r_{L1}=r_{L2}=10\text{ m}\Omega, r_{S1}=r_{S2}=r_{S3}=r_{S4}=5\text{ m}\Omega$ , voltage conversion from 14 V to 17.3 V

*Step-down:*  $r_{L1}=r_{L2}=10\text{ m}\Omega, r_{S1}=r_{S2}=r_{S3}=r_{S4}=5\text{ m}\Omega$ , voltage conversion from 21 V to 17.3 V

Substituting these parameters into (28), (30), (32), and (34), the calculated efficiencies are plotted in Fig. 8. The proposed converter is more efficient than the conventional SEPIC/ZETA converter, particularly in a higher power range, because it optimized selection of duty ratios is possible with respect to the conversion ratio.

## V. SOFT SWITCHING

The proposed converter has been treated as a hard switched type for simple analysis. However, the converter has

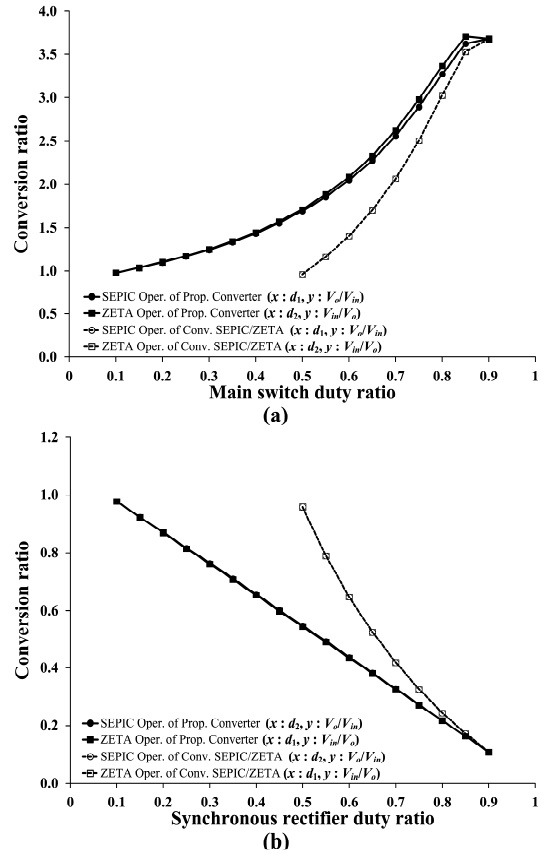


Fig. 7. Calculated voltage gains of the proposed converter and the conventional bidirectional SEPIC/ZETA converter in (a) step-up and (b) step-down modes.

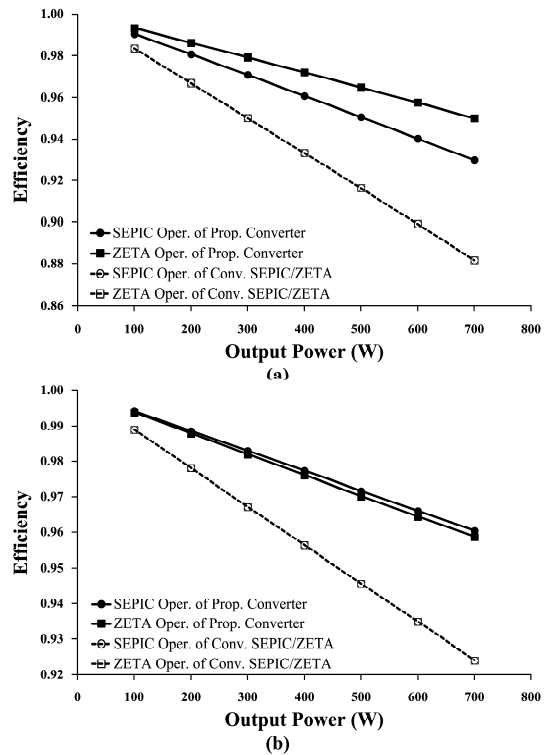


Fig. 8. Calculated efficiencies of the proposed converter and the conventional bidirectional SEPIC/ZETA converter in (a) step-up and (b) step-down modes.

soft-switching features because of the small inductor  $L_a$  on the auxiliary current path. The soft current commutation aspect of the proposed converter in SEPIC operation mode is shown in Fig. 9. As mentioned in the analysis of Section II,  $S_4$  is turned off after  $t_0$  at the beginning of Mode 1. During this overlapped time between  $S_1$  and  $S_4$ , the sum of  $i_{L1}$  and  $i_{L2}$  equals the sum of  $i_{S1}$  and  $i_{L_a}$ . The voltage of  $L_a$  becomes  $-V_o$  and  $i_{L1}+i_{L2}$  can be assumed constant during this short time interval; thus,

$$\frac{di_{S1}}{dt} = -\frac{di_{L_a}}{dt} = \frac{V_o}{L_a} \quad (35)$$

Therefore,  $S_3$  and  $S_4$  are switched off with the current slope of  $-V_o/L_a$ , and  $S_1$  is switched on with the current slope of  $V_o/L_a$ . This soft current commutation takes the time of  $L_a I_{L_a}(t_0)/V_o$ ; thus,  $S_4$  should be turned off after this time interval for soft switching. This commutation time should be shorter than the duration of the main switch to achieve ZCS; thus,

$$\frac{L_a I_{L_a}(t_0)}{V_o} < d_1 T \quad (36)$$

A similar phenomenon occurs at the beginning of Mode 3. After turning on  $S_3$  and  $S_4$ , the sum of inductor currents  $i_{L1}+i_{L2}$  is distributed to the  $S_2$  and auxiliary current path through  $S_3$  and  $S_4$ . During this commutation time,  $i_{L1}+i_{L2}$  can be assumed constant and the voltage of  $L_a$  becomes  $V_{in}$ ; therefore,

$$-\frac{di_{S2}}{dt} = \frac{di_{L_a}}{dt} = \frac{V_{in}}{L_a} \quad (37)$$

$S_2$  is turned off with the current slope of  $-V_{in}/L_a$  and thus the diode reverse recovery problem is alleviated.  $S_3$  and  $S_4$  are turned on with the current slope of  $V_{in}/L_a$ . This commutation process takes the time of  $L_a I_{L_a}(t_2)/V_{in}$ .  $S_2$  should be turned off before  $t_2$  for soft switching. This commutation time should be shorter than the duration of auxiliary switches to achieve ZCS; thus,

$$\frac{L_a I_{L_a}(t_2)}{V_{in}} < d_3 T \quad (38)$$

In summary, small inductor  $L_a$  induces soft current commutation between switches on the auxiliary current path and thereby achieves ZCS of all switches. The ZETA operation mode can accomplish the same in the proposed converter. Apart from the ZCS effect, ZVS turn-on and turn-off are also achieved at synchronous rectifiers, which are  $S_2$  in SEPIC and  $S_1$  in ZETA modes, respectively.

## VI. SIMULATIONS AND EXPERIMENTS

A forward SEPIC operation of step-down case (from 21 V to 17.3 V) and a reverse ZETA operation of step-up case (from 14 V to 17.3 V) are simulated to verify the operation of the proposed converter. The electric specifications are as follows: Output power  $P_o = 320$  W and switching frequency  $f_s = 100$  kHz. To obtain 10% and 50% ripples of  $i_{L1}$  and  $i_{L2}$ , respectively, the inductors are selected by  $L_1 = L_2 = 30$   $\mu$ H. For the ripple voltages of  $C_{in}$  ( $\Delta v_{in}$ ) and  $C_o$  ( $\Delta v_o$ ) to reach 1% and that of  $C_s$

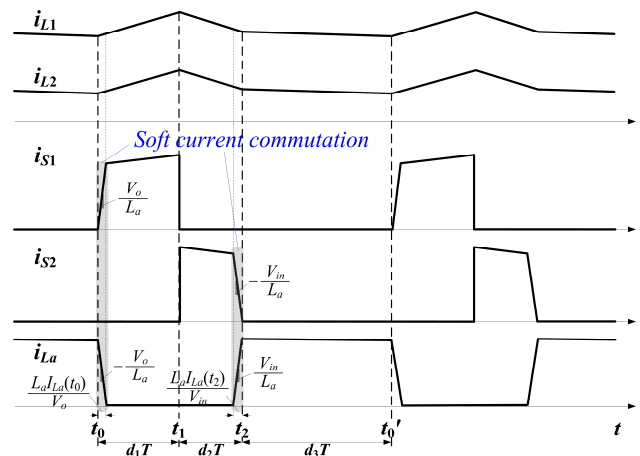


Fig. 9. Soft current commutation of the proposed converter in SEPIC operation.

( $\Delta v_{C_s}$ ) to reach 2%, the capacitors are chosen by  $C_{in} = 33$   $\mu$ F,  $C_s = 235$   $\mu$ F, and  $C_o = 440$   $\mu$ F, respectively. These inductors and capacitors are determined by formulas in Table I, with the actual switching duty ratios considered.  $L_a$  is set at 220 nH for the soft current commutation time of 200 ns, with  $S_1$ - $S_4 =$  IPP110N20N3 (200 V, 88 A, 10.7 m $\Omega$ ). In the simulation, a damping resistor of 50  $\Omega$  is added parallel to  $L_a$  to attenuate parasitic oscillations occurring from  $L_a$  and the output capacitances of the switches. The simulation results are shown in Fig. 10. Soft current commutation between the switches and ZCS turn on and/or turn off of switches are observed. With proper gating control, ZVS turn-on and turn-off, and synchronous rectifications are achieved in  $S_2$  and  $S_1$  for SEPIC and ZETA operations, respectively. The inductor current ripples are also highly reduced because the conduction time of the main switch and synchronous rectifier considerably decreased, thereby reducing the DC resistive losses of inductors and capacitors as well as the conduction and switching losses of switches.

A prototype circuit of the proposed converter (Fig. 11) is built to verify the performance of the proposed converter. The electric specifications and circuit component values are the same with simulation. For a fair comparison between the proposed converter and the conventional bidirectional SEPIC/ZETA converter, several experimental waveforms, such as inductor currents ( $i_{L1}$ ,  $i_{L2}$ ), switch currents ( $i_{S1}$ ,  $i_{S2}$ ,  $i_{L_a}$ ), and switch voltages ( $v_{S1}$ ,  $v_{S2}$ ,  $v_{S3}$ ,  $v_{S4}$ ), are measured under the same electric specifications and circuit parameters. These waveforms are shown in Figs. 12 and 13 for SEPIC step-down operation (from 21 V to 17.3 V) and shown in Figs. 14 and 15 for ZETA step-up operation (from 14 V to 17.3 V). Negative current polarity in ZETA operation indicates reverse power flow. In SEPIC operation, the inductor ripple current of the proposed converter (2.19 A) is reduced by 47% compared with that of the conventional converter (4.14 A). In ZETA operation, the inductor ripple current is reduced by 32% from the



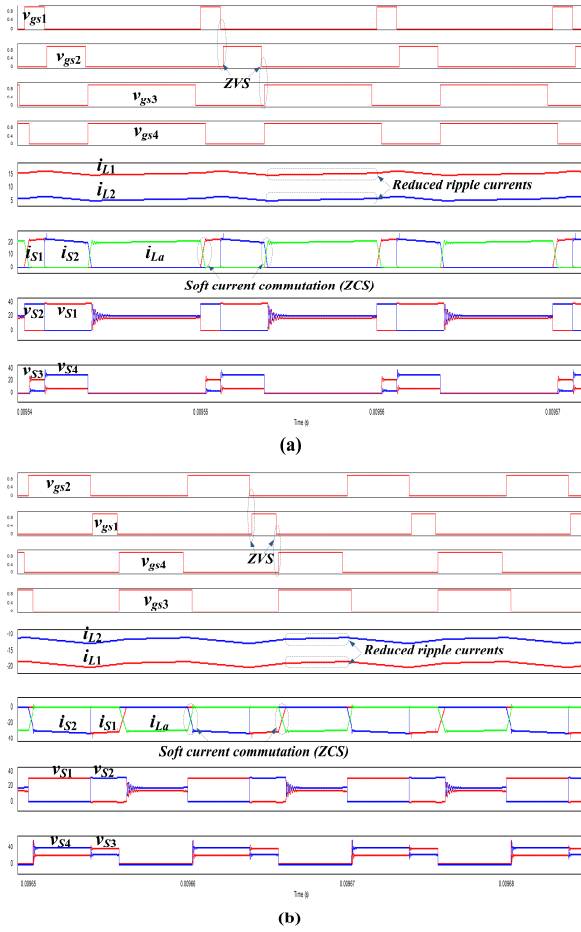


Fig. 10. Simulation results of the proposed converter in (a) SEPIC step-down and (b) ZETA step-up operations.

conventional SEPIC/ZETA (3.33 A) to the proposed converter (2.25 A). For the proposed converter, soft current commutations between switches are confirmed and all switches achieved good ZCS property. In contrast, the conventional SEPIC/ZETA converter showed hard-switching behavior. Based on the measured switching voltages and currents, the switching and conduction losses of switches are calculated in reference to [26]. The switching loss  $P_{sw}$  is given as

$$P_{sw} = (W_{on} + W_{off}) \cdot f_s \quad (39)$$

where  $W_{on}$  and  $W_{off}$  are energy lost during switching turn-on and turn-off transients, respectively, given by

$$W_{on} = \frac{1}{2} V_p I_p t_{on}, \quad W_{off} = \frac{1}{2} V_p I_p t_{off} \quad (40)$$

where  $V_p$  and  $I_p$  are the switching peak voltage and current during switching transients, respectively; and  $t_{on}$  and  $t_{off}$  are the time length of switching turn-on and turn-off transients, respectively. Conduction loss  $P_{cond}$  is given by

$$P_{cond} = I_{s,rms}^2 \cdot r_s \quad (41)$$

where  $I_{s,rms}$  is rms current of switch in Table I, and  $r_s$  is on state drain-source resistance. Assuming  $t_{on}$  and  $t_{off}$  are both 50 ns, the switch losses of the proposed and conventional converters are

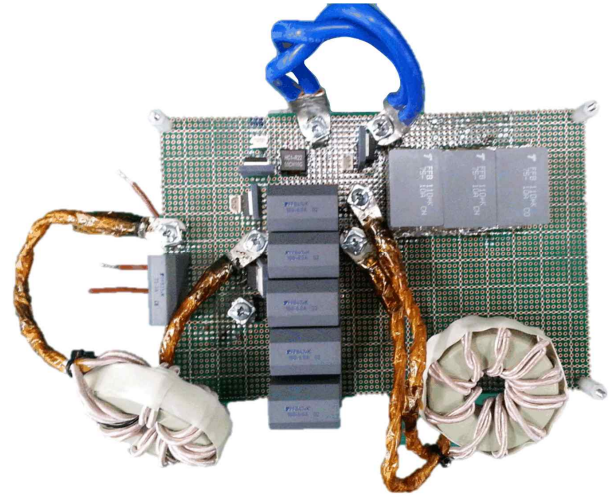


Fig. 11. Prototype circuit of the proposed converter.

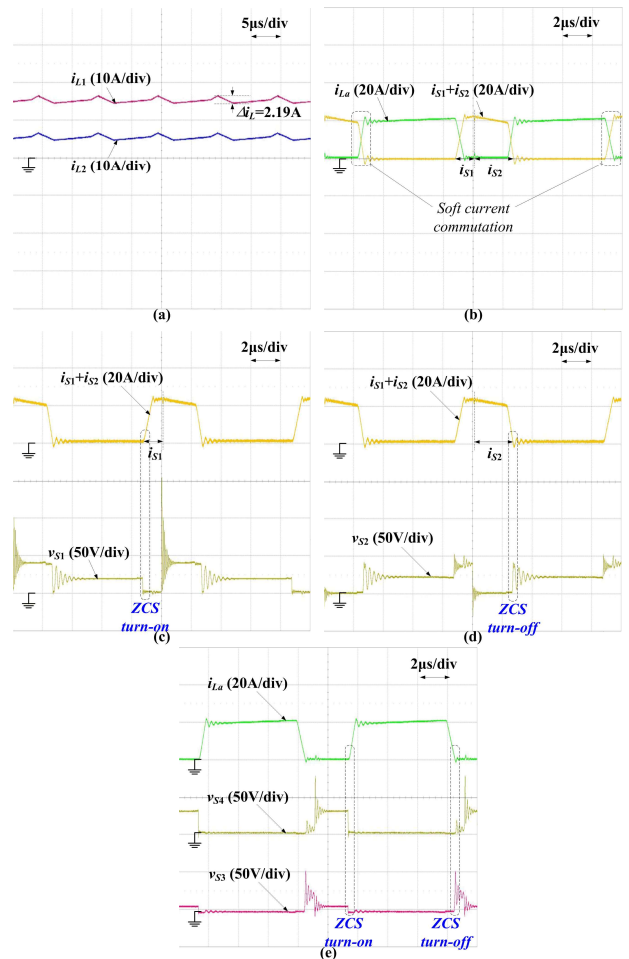


Fig. 12. Measured waveforms of the proposed converter in SEPIC step-down mode (a)  $i_{L1}$  and  $i_{L2}$ , (b)  $i_{S1}$ ,  $i_{S2}$  and  $i_{La}$ , (c)  $i_{S1}$  and  $v_{S1}$ , (d)  $i_{S2}$  and  $v_{S2}$ , and (e)  $i_{La}$ ,  $v_{S3}$ , and  $v_{S4}$ .

obtained in Table II. As a result, the overall conduction and switching losses of the proposed converter are lower by 41% than those of the conventional SEPIC/ZETA converter.

Large voltage spikes are observed at switching turn-off transient in the voltage measurements of both proposed and

TABLE II

CALCULATED SWITCH LOSSES OF THE PROPOSED AND CONVENTIONAL SEPIC/ZETA CONVERTERS AT  $P_o = 320$  W

Power loss	SEPIC step-down		ZETA step-up	
	Conventional	Proposed	Conventional	Proposed
Switching loss[W]	6.66	2.26	6.67	2.64
Conduction loss[W]	12.99	8.02	19.48	14.29
Total switch loss[W]	19.65	10.29	26.16	16.93

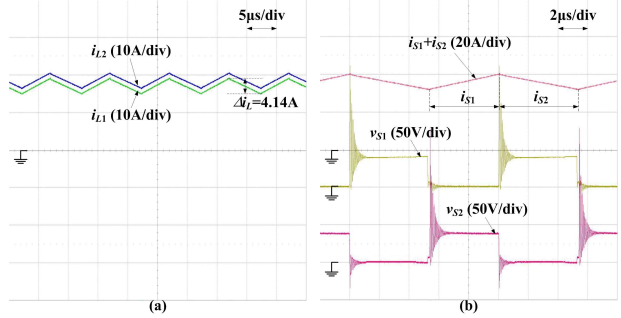


Fig. 13. Measured waveforms of the conventional bidirectional SEPIC/ZETA converter in SEPIC step-down mode (a)  $i_{L1}$  and  $i_{L2}$  and (b)  $i_{S1}$ ,  $i_{S2}$ ,  $v_{S1}$ , and  $v_{S2}$ .

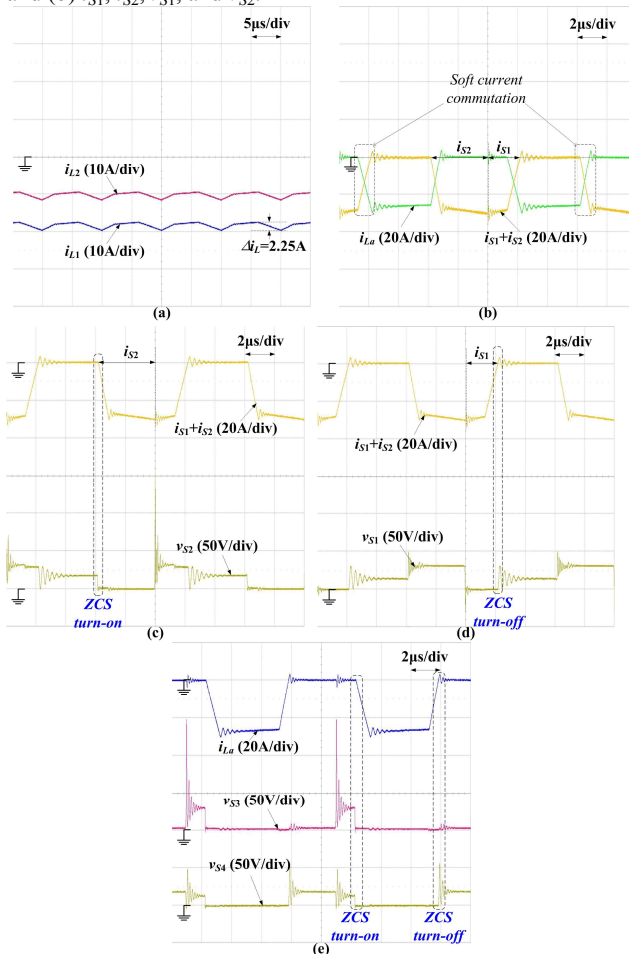


Fig. 14. Measured waveforms of the proposed converter in ZETA step-up mode (a)  $i_{L1}$  and  $i_{L2}$ , (b)  $i_{S1}$ ,  $i_{S2}$  and  $i_{La}$ , (c)  $i_{S2}$  and  $v_{S2}$ , (d)  $i_{S1}$  and  $v_{S1}$ , and (e)  $i_{La}$ ,  $v_{S3}$ , and  $v_{S4}$ .

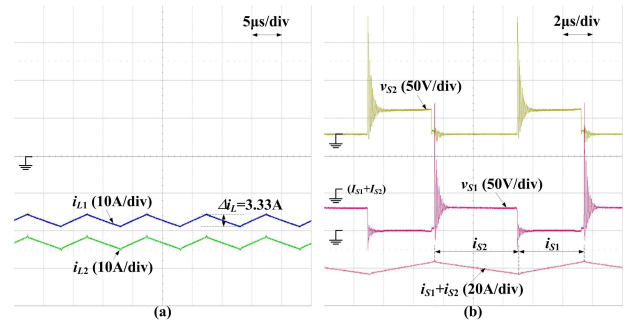


Fig. 15. Measured waveforms of the conventional bidirectional SEPIC/ZETA converter in ZETA step-up mode (a)  $i_{L1}$  and  $i_{L2}$  and (b)  $i_{S1}$ ,  $i_{S2}$ ,  $v_{S1}$ , and  $v_{S2}$ .

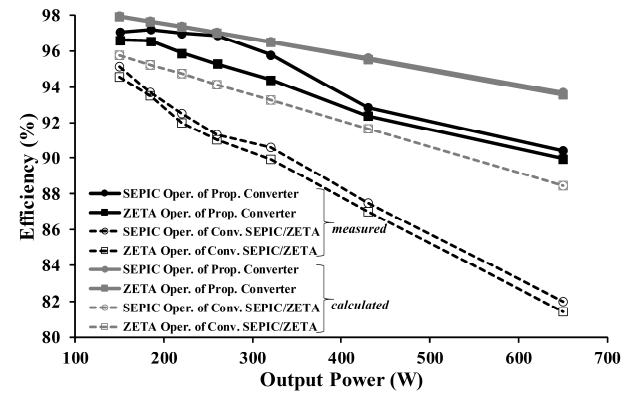


Fig. 16. Measured and calculated efficiencies of the proposed and conventional bidirectional SEPIC/ZETA converters.

conventional SEPIC/ZETA converters. The voltage spikes are caused by unclamped parasitic inductances of hardwired connectors in series with switches in prototype circuit that was built in breadboard. To eliminate these voltage spikes, the power stack has to be redesigned to reduce the series inductance, or certain snubber circuits, such as the RC voltage snubber in [28], are required to suppress them. However, such options are not considered in these experiments because the focus is on the performance comparison between the proposed and conventional converters. Nonetheless, when a properly designed RC voltage snubber is applied to the circuit, the voltage spike during turn-off transient would be effectively reduced, with efficiency dropping below 1%. To measure the switch currents  $i_{S1}$  and  $i_{S2}$ ,  $i_{S1}+i_{S2}$  is used instead of individual  $i_{S1}$  and  $i_{S2}$ . To place a current probe, an artificial wire should be inserted in series with switch. The artificial wire's small inductance induces unwanted parasitic oscillation with parasitic capacitances of circuit components and causes a high voltage spike during switching turn-off transient. These effects can be avoided by extracting switch currents  $i_{S1}$  and  $i_{S2}$  using the mathematical functions of oscilloscope, such as sum and subtraction, i.e.,  $i_{S1} + i_{S2} = i_{L1} + i_{L2} - i_{La}$ . In  $i_{S1} + i_{S2}$ ,  $i_{S1}$  and  $i_{S2}$  are easily distinguished from the current slope change.

The measured efficiencies of the two converters are shown as black lines in Fig. 16. The average efficiency of the proposed converter is 5% higher than that of the conventional

converter. The efficiency difference between the two converters is proportional to output power because of the increased conduction and switching losses of the circuit components in high current range. The thermal design for heat radiation of the switches and inductors is not considered in this prototype circuit because of laboratory limitations. The efficiency curve rapidly decreases in values in the high power range. Assuming that a proper thermal design is implemented and thus efficiency degradation from thermal-related issues are nonexistent, the ideal efficiency curve can be expected through loss analysis, including switching and conduction losses of switches and DC resistive losses of inductors. Switch losses can be calculated using (39), (40), and (41). DC resistive losses of inductors,  $P_L$ , are determined by

$$P_L = I_{L,rms}^2 \cdot r_L \quad (42)$$

where  $I_{L,rms}$  is rms current of inductor in Table I and  $r_L$  is DC resistance of inductors of 5 mΩ, shown as gray lines in Fig. 16. At  $P_o = 650$  W, the ideal calculated efficiency of the proposed converter is 3.5% higher than measured one.

## VII. CONCLUSIONS

A new non-isolated bidirectional soft switching SEPIC/ZETA converter that can reduce ripple currents in inductors is studied. The proposed converter has the following advantages:

- 1) Inductor currents have reduced ripple because the conduction time of the main switch and synchronous rectifier is reduced.
- 2) ZCS turn-on and/or turn-off are achieved in all switches with soft current commutation among them.
- 3) Synchronous rectification and ZVS turn-on and turn-off are achieved in the synchronous rectifier.
- 4) Voltage gains in both step-up and step-down modes can be higher than those of conventional bidirectional SEPIC/ZETA converter because of the optimized duty ratios of switches. As a result, conduction and switching losses in circuit components were considerably reduced. Lower current rated switches can be also utilized, and the filter size can be minimized. The experimental results of the prototype circuit shows that the operation waveforms and soft-switching properties well agree with theoretical analysis and simulation results. Measured inductor ripple currents are reduced by 40%, and the overall efficiency of the proposed converter is 5% higher than the conventional bidirectional SEPIC/ZETA converter, demonstrating the effectiveness of the proposed converter.

## REFERENCES

- [1] M. Jain, M. Daniele, and P. K. Jain, "A bidirectional DC-DC converter topology for low power application," *IEEE Trans. Power Electron.*, Vol. 15, No. 4, pp. 595-606, Jul. 2000.
- [2] R. Singh and S. Mishra, "A magnetically coupled feedback-clamped optimal bidirectional battery charger," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 1, pp. 422-432, Feb. 2013.
- [3] J. Cao and A. Emadi, "A new battery/ultracapacitor hybrid energy storage system for electric, hybrid, and plug-in hybrid electric vehicles," *IEEE Trans. Power Electron.*, Vol. 27, No.1, pp. 122-132, Jan. 2012.
- [4] Z. Zhang, Z. Ouyang, O. C. Thomsen, and M. A. E. Andersen, "Analysis and design of a bidirectional isolated DC-DC converter for fuel cells and supercapacitors hybrid system," *IEEE Trans. Power Electron.*, Vol. 27, No. 1, pp. 848-859, Feb. 2012.
- [5] A. K. Rathore and U. R. Prasanna, "Analysis, design, and experimental results of novel snubberless bi-directional naturally clamped ZCS/ZVS current-fed half-bridge DC/DC Converter for fuel cell vehicles," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 10, pp. 4482-4491, Oct. 2013.
- [6] N. M. L. Tan, T. Abe, and H. Akagi, "Design and performance of a bidirectional isolated DC-DC converter for a battery energy storage system," *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1237-1248, Mar. 2012.
- [7] H. Tao, J. L. Duarte, and M. A. M. Hendrix, "Line-interactive UPS using a fuel cell as the primary source," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 8, pp. 3012-3021, Aug. 2008.
- [8] C. G. Yoo, W.-C. Lee, K.-C. Lee, and B. H. Cho, "Transient current suppression scheme for bidirectional dc-dc converters in 42 V automotive power system," *Journal of Power Electronics*, Vol. 9, No. 4, pp.517 -525, Jul. 2009.
- [9] M. Kwon, J. Park, and S. Choi, "High gain soft-switching bidirectional DC-DC converters for eco-friendly vehicles," in *Proc. IEEE APEC*, pp. 1776-1782, 2013.
- [10] L. R. Chen, N. Y. Chu, C. S. Wang, and R. H. Liang, "Design of a reflex-based bidirectional converter with the energy recovery function," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 8, pp. 3022-3029, Aug. 2008.
- [11] D.-Y. Jung, S.-H. Hwang, Y.-H. Ji, J.-H. Lee, Y.-C. Jung, and C.-Y. Won "Soft-switching bidirectional DC/DC converter with a LC series resonant circuit," *IEEE Trans. Power Electron.*, Vol. 28, No. 4, pp. 1680-1690, Apr. 2013.
- [12] H. Wu, J. Lu, W. Shi, and Y. Xing, "Non-isolated bidirectional DC-DC converters with negative-coupled inductor," *IEEE Trans. Power Electron.*, Vol. 27, No. 5, pp. 2231-2235, May 2007.
- [13] H.-L. Do, "Non-isolated bidirectional zero-voltage-switching DC-DC converter," *IEEE Trans. Power Electron.*, Vol. 26, No. 9, pp. 2563-2569, Sep. 2011.
- [14] P. Jose and N. Mohan, "A novel ZVS bidirectional cuk converter for dual voltage systems in automobiles," *Proc. IEEE IECON Conf. Rec.*, pp. 117-122, 2003.
- [15] I. D. Kim, S. H. Paeng, J. W. Ahn, E. C. Nho, and J. S. Ko, "New bidirectional ZVS PWM sepic/zeta DC-DC converter," in *Proc. IEEE ISIE*, pp. 555-560, 2007.
- [16] K. Jin , M. Yang , X. Ruan, and M. Xu, "Three-level bidirectional converter for fuel-cell/battery hybrid power system," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 6, pp. 1976-1986, Jun. 2010.

- [17] W. Qian, H. Cha, Z. Fang, and L. M. Tolbert, "55-kW variable 3X DC-DC converter for plug-in hybrid electric vehicles," *IEEE Trans. Power Electron.*, Vol. 27, No. 4, pp. 1668-1678, Apr. 2012.
- [18] P. Das, S. A. Mousavi, and G. Moschopoulos, "Analysis and design of a non-isolated bidirectional ZVS-PWM DC-DC converter with coupled inductors," *IEEE Trans. Power Electron.*, Vol. 25, No. 10, pp. 2630-2641, Oct. 2010.
- [19] Y.-P. Hsieh, J.-F. Chen, L.-S. Yang, C.-Y. Wu, and W.-S. Liu, "High-conversion-ratio bidirectional DC-dc converter with coupled inductor," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 1, pp. 210-222, Jan. 2014.
- [20] O. Garcia, P. Zumel, A. de Castro, and J. A. Cobos, "Automotive DC-DC bidirectional converter made with many interleaved buck stages," *IEEE Trans. Power Electron.*, Vol. 21, No. 3, pp. 578-586, May. 2006.
- [21] L. Ni, D. J. Patterson, and J. L. Hudgins, "High power current sensorless bidirectional 16-phase interleaved DC-DC converter for hybrid vehicle application," *IEEE Trans. Power Electron.*, Vol. 27, No. 3, pp. 1141-1151, Mar. 2012.
- [22] J.-B. Baek, W.-I. Choi, and B.-H. Cho, "Digital adaptive frequency modulation for bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 11, pp. 5167-5176, Nov. 2013.
- [23] M. S. Song, E. S. Oh, and B. K. Kang, "Modified SEPIC having enhanced power conversion efficiency," *Electron. Lett.*, Vol. 48, No. 18, pp. 1151-1153, Aug. 2012.
- [24] E. Oh, M. S. Song, B. Kang, and Y. K. Park, "High-efficiency direct-linked zeta converter for LED backlight units," *SID Symposium Digest of Technical Papers*, pp. 1320-1323, 2011.
- [25] J. J. Jozwik and M. K. Kazimierczuk, "Dual sepic PWM switching-mode DC/DC power converter," *IEEE Trans. Ind. Electron.*, Vol. 36, No. 1, pp. 64-70, Feb. 1989.
- [26] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed., Springer, pp. 15-22, 2001.
- [27] L. S. Yang and T. J. Liang, "Analysis and implementation of a novel bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 1, pp. 422-434, Jan. 2012.
- [28] P. C. Todd, "Snubber circuits: Theory, design and application," *Unitrode-Power Supply Design Seminar*, pp. 2-1-2-17, 1993.



**Min-Sup Song** received his B.S., M.S., and Ph.D. in Electrical Engineering from Pohang University of Science and Technology, Pohang, Korea in 2005, 2007, and 2011, respectively. He is currently a Senior Research Engineer at Samsung Electro-Mechanics, Suwon, Korea. His research interests include power conversion and power control systems.



**Young-Dong Son** received his B.S. and M.S. degrees in Mechanical Engineering from Chonnam National University, Gwang-Ju, Korea in 2002 and 2006, respectively. He is currently a Senior Research Engineer at Samsung Electro-Mechanics, Suwon, Korea. His research interests are power electronics and electric machine control systems.



**Kwang-Hyun Lee** received his B.S. and M.S. degrees in Electrical Engineering from Ulsan University, Ulsan, Korea in 2009 and 2011, respectively. Since 2011, he has been with Samsung Electro-Mechanics as an Assistant Research Engineer. His research interests include the design and control of motors, as well as electric vehicle propulsion.