JPE 14-4-6

http://dx.doi.org/10.6113/JPE.2014.14.4.671
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A New Basic Unit for Cascaded Multilevel Inverters with the Capability of Reducing the Number of Switches

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Abstract

In this paper, a new basic unit is proposed. Then, a cascaded multilevel inverter basded on the series connection of n number of these new basic units is proposed. In order to generate all of the voltage levels (even and odd) at the output, three different algorithms to determine the magnitude of the dc voltage source are proposed. Reductions in the number of power switches, driver circuits and dc voltage sources in addition to increases in the numbr of output voltage levels are some of the advantages of the proposed cascaded multilevel inverter. These results are obtained through a comparison of the proposed inverter and its algorithms with an H-bridge cascaded multilevel inverter from the point of view of the number of power electronic devices. Finally, the capability of the proposed topology with its proposed algorithms in generating all of the voltage levels is verified through experimental results on a laboratorary prototype of a 49-level inverter.

Key words: H-Bridge Cascaded Multilevel Inverter, Multilevel Inverters, New Basic Unit

I. INTRODUCTION

Multilevel inverters have received more attention when compared with traditional two level inverters. There are three main topologies and several derivation topologies for multilevel inverters. The main topologies are the diode-clamped multilevel inverters, flying capacitor multilevel inverters and cascaded multilevel inverters [1], [2]. The cascaded multilevel inverter has received special attention due to its modularity, simplicity of control, reliability and lower power electronic devices for the generation a specific output voltage level [3]-[6]. Cascaded multilevel inverters are mainly classified into two groups: symmetric cascaded multilevel inverters and asymmetric cascaded multilevel inverters [4]. In the symmetric cascaded multilevel inverters the magnitudes of all of the dc voltage sources are equal, which results in a higher number of insulated gate bipolar transistors (IGBTs), power diodes and dc voltage sources to generate a high number of output levels. These features lead to increases in terms of the installation space and total cost of the inverter. These are the main disadvantages of the symmetric cascaded multilevel inverters while the same value for all of the dc voltage sources are their most significant advantage. Two symmetric cascaded multilevel inverters have been presented in [7], [8]. An H-bridge cascaded multilevel inverter has been presented in [9]. In [9], two different algorithms have been presented which leads to symmetric and asymmetric topologies. Asymmetric cascaded multilevel inverters have been presented in several studies in order to increase the number of output voltage levels. In asymmetric topologies, the magnitudes of the dc voltage sources are unequal. Therefore, there are different algorithms to determine the value of the dc voltage sources. In [10], [11] two other algorithms of asymmetric topologies have been presented for H-bridge cascaded multilevel inverters. In addition, two other topologies for asymmetric cascaded multilevel inverters have been presented in [4] and [12]. The major advantage of the asymmetric cascaded topology is a considerable increase in the number of output voltage levels by using a low number of dc voltage sources and power switches. However, high variability in the magnitude of the dc voltage sources is their most remarkable disadvantage.

In this paper, a cascaded multilevel inverter based on a new basic unit is proposed. This inverter increases the

Manuscript received Jan. 20, 2014; accepted Apr. 9, 2014
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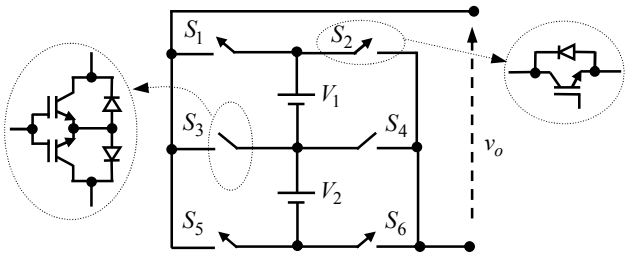


Fig. 1. The proposed basic unit.

number of output voltage levels by using a minimum number of power switches, driver circuits and dc voltage sources. Then, three different algorithms to generate all of the voltage levels are proposed. These advantages are confirmed by a comparison the proposed inverter and its algorithms with an H-bridge cascaded multilevel inverter. Finally, experimental results obtained from a 49-level inverter confirm the correct performance of the proposed topology in generating all of the voltage levels.

II. PROPOSED TOPOLOGY

The new proposed basic unit is shown in Fig.1. As Fig. 1 shows, the proposed basic unit consists of two dc voltage sources, two bidirectional switches (S_3 and S_4) and four unidirectional switches (S_1, S_2, S_5 and S_6) from voltage point of view. The bidirectional switches conduct current and voltage in two direction while the unidirectional switches conduct current in two directions and block voltage in one direction. In addition, each unidirectional switch consists of an IGBT with an anti-parallel power diode and a driver circuit. However, the bidirectional switches include two IGBTs with two anti-parallel power diodes and a driver circuits if a switch with a common emitter configuration is used. Therefore, the number of driver circuits for the bidirectional switches is as same as the unidirectional switches in the proposed basic unit. According to Fig. 1, the switches (S_1 and S_3), (S_1 and S_5), (S_3 and S_5), (S_2 and S_4), (S_2 and S_6) and (S_4 and S_6) should not be turned on simultaneously, because a short-circuit across the dc voltage sources will be produced. Table I shows the output voltage levels of the proposed unit based on different switching patterns. In this Table, 1 and 0 indicate the on and off states of the switches, respectively. As shown in Table I, the proposed basic unit is able to generate seven voltage levels (three positive levels, three negative levels and one zero level) at the output. It is also obvious that this basic unit is able to generate all of the positive and negative voltage levels at the output.

A new cascaded multilevel inverter can be made by a series connection of n number of basic units. This new proposed cascaded multilevel inverter is shown in Fig. 2. The

TABLE I

THE OUTPUT VOLTAGE OF THE PROPOSED BASIC UNIT BASED ON DIFFERENT SWITCHING PATTERNS

State	S_1	S_2	S_3	S_4	S_5	S_6	v_o
1	1	0	0	1	0	0	$+V_1$
2	0	0	1	0	0	1	$+V_2$
3	1	0	0	0	0	1	$+(V_1+V_2)$
4	1	1	0	0	0	0	0
	0	0	0	0	1	1	
5	0	1	1	0	0	0	$-V_1$
6	0	0	0	1	1	0	$-V_2$
7	0	1	0	0	1	0	$-(V_1+V_2)$

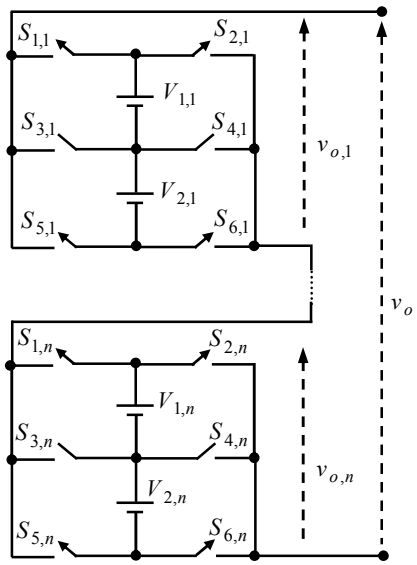


Fig. 2. Series connection of n number of the basic unit.

output voltage of the proposed inverter is equal to adding the output voltage of each unit and it can be written as follows:

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \cdots + v_{o,n}(t) \quad (1)$$

where n is the number of series connected basic units.

In the proposed cascaded multilevel inverter, the number of switches (N_{switch}), IGBTs (N_{IGBT}), driver circuits (N_{driver}) and dc voltage sources (N_{source}) are calculated as follows:

$$N_{switch} = 6n \quad (2)$$

$$N_{IGBT} = 8n \quad (3)$$

$$N_{driver} = 6n \quad (4)$$

$$N_{source} = 2n \quad (5)$$

It is important to note that in the basic proposed unit determination the magnitude of the dc voltage sources has the most significant influence in increasing the number of generated output voltage levels. It also influences the use of power electronic devices and so the amount of installation space and the total cost of the inverter. Therefore, to generate all of the voltage levels, three different algorithms to determine the value of the used dc voltage sources will be proposed.

A. First Proposed Algorithm (P_1)

In this sub-section, the amplitude of the two used dc voltage in the basic units is written as follows:

First unit:

$$V_{1,1} = V_{dc} \tag{6}$$

$$V_{2,1} = 2V_{dc} \tag{7}$$

n^{th} *unit:*

$$V_{1,n} = V_{dc} + 2\sum_{i=1}^{n-1}\sum_{j=1}^{2} V_{i,j} \tag{8}$$

$$V_{2,n} = 2V_{1,n} \tag{9}$$

In this algorithm, the number of output voltage levels (N_{level}) and the maximum amplitude of the producible output voltage ($V_{o,\max}$) are equal to:

$$N_{level} = 7^n \tag{10}$$

$$V_{o,\max} = V_{dc} \times \left(\frac{7^n - 1}{2}\right) \tag{11}$$

B. Second Proposed Algorithm (P_2)

In the second proposed algorithm, the magnitudes of the dc voltage sources are determined as follows:

$$V_{1,j} = 2^{j-1}V_{dc} \tag{12}$$

$$V_{2,j} = 2^{j}V_{dc} \tag{13}$$

Considering this proposed algorithm, the number of output voltage levels and the maximum magnitude of the output voltage are calculated as follows:

$$N_{level} = (3 \times 2^{n+1}) - 5 \tag{14}$$

$$V_{o,\max} = 3 \times (2^n - 1)V_{dc} \tag{15}$$

C. Third Proposed Algorithm (P_3)

In this sub-section, the values of the dc voltage sources are selected as follows:

$$V_{1,1} = V_{1,1} = V_{dc} \tag{16}$$

$$V_{1,j} = 3^{j-1}V_{dc} \qquad for \quad j = 2, 3, \cdots, n \tag{17}$$

$$V_{2,j} = 2 \times 3^{j-1}V_{dc} \tag{18}$$

In this condition, the number of output voltage levels and the maximum magnitude of the output voltage are written as follows:

$$N_{level} = 3^{n+1} - 4 \tag{19}$$

$$V_{o,\max} = \left(\frac{3^{n+1} - 5}{2}\right)V_{dc} \tag{20}$$

III. Comparing the Proposed General Topology with the H-Bridge Topology

The most important aim of introducing the new-cascaded multilevel inverter and its proposed algorithms is increasing the number of output voltage levels while using fewer power electronic devices such as switches, IGBTs, power diodes, driver circuits and so on. In this section, a comparison between the proposed topology and its algorithms with an H-bridge cascaded multilevel inverter is done to investigate the advantages and disadvantages of the proposed cascaded inverter.

The proposed topology based on the first, second and third proposed algorithms are considered as $P_1 - P_3$ in this investigation, respectively. In [9], an H-bridge cascaded multilevel inverter and two different algorithms have been presented. One of them is known as the symmetric cascaded inverter ($V_1 = V_2 = V_3 = \cdots = V_n = V_{dc}$) while the other one is known as the asymmetric cascaded inverter ($V_1 = V_{dc}$,$V_2 = 2V_{dc} \cdots, V_n = 2^{n-1}V_{dc}$). In this comparison, these two different algorithms are considered as R_1 and R_2, respectively. In order to increase the number of output voltage levels while using a minimum of H-bridges, two other algorithms were presented in [10-11]. They are considered by $R_3 - R_4$ in this comparison (R_3 for $V_1 = V_{dc}$, $V_2 = V_3 = \cdots = V_n = 2V_{dc}$ and R_4 for $V_1 = V_{dc}$, $V_2 = V_3 = \cdots = V_n = 3V_{dc}$). Fig. 3 indicates the H-bridge cascaded multilevel inverter.

Fig. 4 compares the number of power electronic switches in the proposed cascaded multilevel inverter based on its proposed algorithms with the H-bridge cascaded inverter. As shown in this figure, the number of power switches required in the proposed cascaded inverter based on the first proposed algorithm is lower than the H-bridge cascaded inverter. In addition, this proposed algorithm has even better performance than other presented algorithms for the proposed topology.

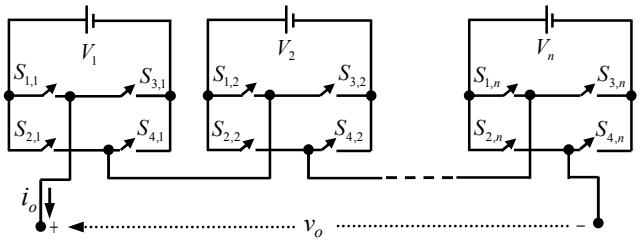


Fig. 3. The H-bridge cascaded multilevel inverter.

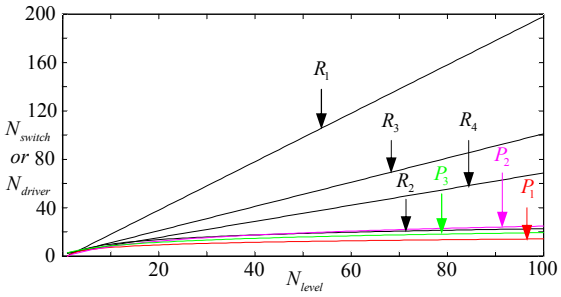


Fig. 4. Variation of N_{switch} or N_{driver} versus N_{level}.

As mentioned before and based on the power switches used in the proposed topology and the H-bridge cascaded inverter, the number of power switches in the proposed cascaded multilevel inverter is equal to the number of driver circuits. As a result, this topology needs fewer driver circuits than the H-bridge cascaded inverter.

Due to the use of bidirectional switches in the proposed topology, it is necessary to compare the number of required IGBTs in this topology with that of the H-bridge cascaded multilevel inverter. This comparison is shown in Fig. 5. As this figure shows, the proposed cascaded topology based on the first proposed algorithm uses fewer IGBTs than the H-bridge cascaded inverter. However, unidirectional switches are only used in the cascaded multilevel inverter. The first proposed algorithm also has the best performance among the other proposed algorithms in terms of the number of required IGBTs. As mentioned before, the number of power diodes is equal to the number of IGBTs. As a result, the number of power diodes in the proposed inverter is lower than the H-bridge cascaded inverter.

Fig. 6 compares the number of dc voltage sources in the proposed topology with that of the H-bridge cascaded multilevel inverter. It can be seen that the number of used dc voltage sources in the proposed topology, especially the one based on the first proposed algorithm, is lower than the H-bridge cascaded inverter and the other presented algorithms for the proposed topology.

Table II shows a comparison of the value of the blocked voltage on the power switches, IGBTs and driver circuits of the proposed topology with that of the H-bridge cascaded inverter. It can be seen that the value of the blocked voltage on the IGBTs depends entirely on the magnitude of the used dc voltage sources.

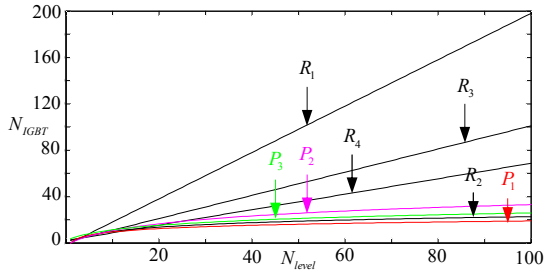


Fig. 5. Variation of N_{IGBT} versus N_{level}.

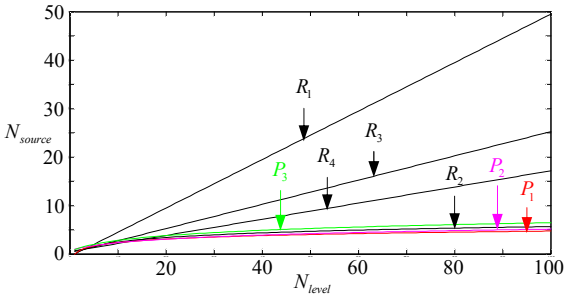


Fig. 6. Variation of N_{source} versus N_{level}.

TABLE II

THE COMPARISON OF THE BLOCKED VOLTAGE ON IGBT IN THE PROPOSED TOPOLOGY AND CASCADED MULTILEVEL INVERTER

Topology	Algorithms	V_{block}
H-bridge cascaded inverter	Presented in [9] (symmetric)	$4nV_{dc}$
	Presented in [9] (asymmetric)	$4(2^n-1)V_{dc}$
	Presented in [10] (asymmetric)	$4(2n-1)V_{dc}$
	Presented in [11] (asymmetric)	$4(3n-2)V_{dc}$
Proposed topology	First proposed algorithm (P_1)	$\frac{8}{3}V_{dc}\times(7^n-1)$
	Second proposed algorithm (P_2)	$16\times(2^n-1)V_{dc}$
	Third proposed algorithm (P_3)	$(8\times3^n-14)V_{dc}$

As the above comparisons indicates, the lower number of required power electronic switches, driver circuits, IGBTs, power diodes and dc voltage source is the most important advantage of the proposed cascaded multilevel inverter. This results in reductions in the installation space and total cost of the inverter.

IV. EXPERIMENTAL RESULTS

The correct performance of the proposed cascaded multilevel inverter in the generation of all of the voltage levels at the output is verified through experimental results on a 49-level inverter based on the basic proposed unit and shown Fig. 2. This inverter consists of two basic units, four dc voltage sources, four bidirectional switches and eight unidirectional switches. The magnitude of the dc voltage sources are determined by using the first proposed algorithm. Therefore, by assuming that the value of $V_{1,1}=10V$, the amplitudes of the dc voltage sources in the first and second units based on (7), (8) and (9) are equal to $V_{2,1}=20V$, $V_{1,2}=70V$, and $V_{2,2}=140V$, respectively. According to (10) and (11) this inverter is able to generate 49 levels (twenty-four positive levels, twenty-four negative levels and one zero level) with a maximum amplitude of 240V at the output. It is important to note that the IGBTs used in the prototype are HGTP10N40CID (with an internal anti-parallel diode). An 89C52 microcontroller by ATMEL Company has been used to generate all of the switching patterns. The connected load to the inverter is considered to be a resistive-inductive load with values of $R=60\Omega$ and $L=55mH$. In this paper, the fundamental frequency switching control method is used. The main reason for selecting this control method is its low switching frequency when compared with other control methods. This in turn leads to reductions in the switching losses

The experimental output voltage waveforms of the first and second units are shown in Fig. 7(a) and Fig. 7(b), respectively. As these figues show, each unit is able to generat a step waveform with pasitive and negative amplitudes. In addition, the maximum amplitude of the output voltage in each unit is equal to adding the magnitude of the used dc voltage surces.

Moreover, the experimental output voltage and current waveforms are indicated in Fig. 8. As it is obvious from Fig. 8, this inverter generates 49 levels with a maximum amplitude of 240V and 3.87A at the output. In addition, the step generated output voltage waveform consists of all of the pasitive and negative voltage levels and looks like a sinosuidal waveform. There are two differences between the voltage and current waveforms. The current waveform looks more like a sinosuidal waveform than the voltage waveform. In addition, there is a phase shift between the voltage and the current. These differences are due to the resistive-inductive load feature, which acts as a low pass filter.

As mentioned before, the basic proposed unit consists of two bidirectional switches and four unidirectional switches from a voltage point of view. In order to investigate these facts in the proposed cascaded multilevel inverter, the blocked voltages on each switch of the first basic unit are

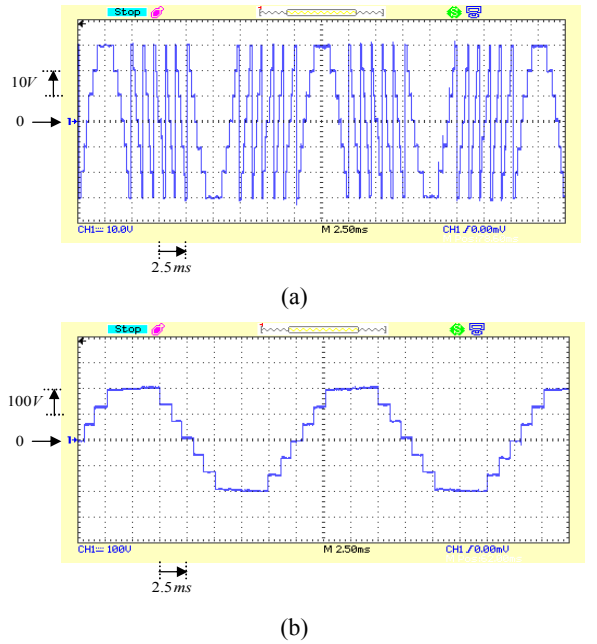


Fig. 7. The output voltages. (a) First bridge. (b) Second bridge.

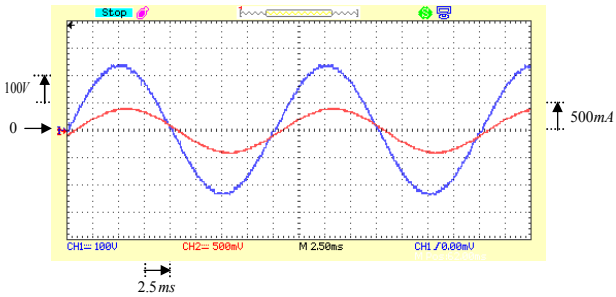
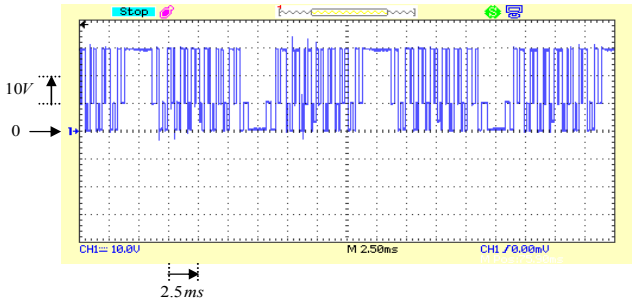
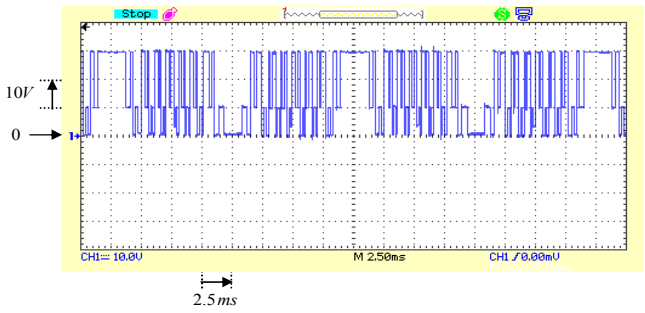


Fig. 8. Voltage and current output waveforms.

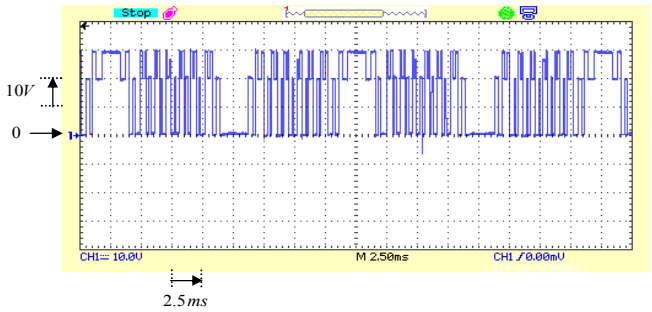
shown in Fig. 9. It is poited out that all of the obtained results are based on the first proposed algorithm. Fig. 9(a), 9(b), 9(c) and 9(d) show the blocked voltages on switches $S_{1,1}$, $S_{2,1}$, $S_{5,1}$ and $S_{6,1}$, respectively. As shown in Figs. 9(a) and 9(b), the values of the blocked voltages on switches $S_{1,1}$ and $S_{2,1}$ are 10V or 30V, depending on the switching pattern. Moreover, Fig. 9(c) and 9(d) show that the blocked voltages on switches $S_{5,1}$ and $S_{6,1}$ are either 20V or 30V. It is clear that the magnitudes of the blocked voltage on the switches are either positive or zero, so there is not a negative amount on them. In addition, the amount of blocked voltage is equal to the sum of the magnitudes of the used dc voltage sources in the first basic unit. As a result, the existence of four unidirectional switches is reconfirmed in the proposed cascaded multilevel inverter. Fig. 9(e) and Fig. 9(f) show the blocked voltages by switches $S_{3,1}$ and $S_{4,1}$, respectively. As shown in these figures, the values of the blocked voltages are either 10V or 20V, depending on the switching pattern.



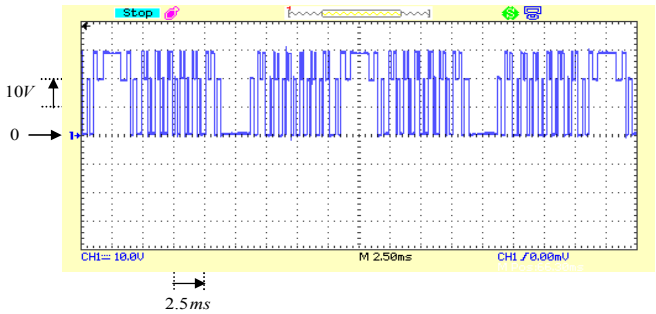
(a)



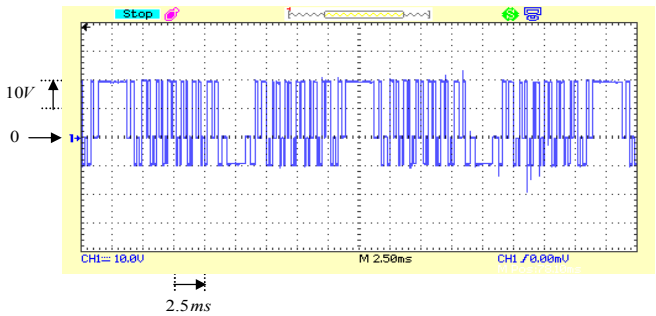
(b)



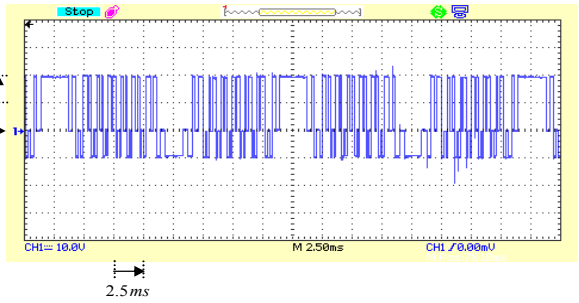
(c)



(d)



(e)



(f)

Fig. 9. The blocked voltage on the power switches in the first basic unit; (a) $S_{1,1}$; (b) $S_{2,1}$; (c) $S_{5,1}$; (d) $S_{6,1}$; (e) $S_{3,1}$; (f) $S_{4,1}$.

Moreover, there are positive and negative amount of voltages on the power switches. This fact verifies that switches $S_{3,1}$ and $S_{4,1}$ are bidirectional.

It is important to note that these values depend directly on the considered algorithm to determine the magnitude of the dc voltage sources. By changing the selected algorithms these magnitudes will be different but their positive and negative values will be the same.

V. CONCLUSIONS

In this paper, a new basic unit for cascaded multilevel inverters is proposed. Then, three different algorithms to determine the magnitude of the dc voltage sources are proposed. Comparisons between an H-bridge cascaded multilevel inverter and the proposed inverter show the significant advantages of the proposed topology in terms of the number of switches, driver cicuits, IGBTs, power diodes and dc voltage sources. In addition, it is determined that the first proposed algorithm has the best performance from all of the proposed algorithms and the H-bridge cascaded inverter. On the other hand, if it is necessary to generate a minimum of 49 levels at the output, the proposed topology based on the first proposed algorithm and equations (2) to (5) needs $N_{switch}=12$, $N_{IGBT}=16$, $N_{Driver}=12$ and $N_{source}=4$. However, under the same conditions, the H-bridge cascaded inverter based on the binary method shown by R_2 requires $N_{switch}=N_{IGBT}=N_{Driver}=24$ and $N_{source}=6$. Finally, in order to verify the capability of the proposed cascaded inverter in the generation of all of the voltage levels, experimental results on a 49-level inverter are used.

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