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Development of Multi-Cell Active Switched-Capacitor and Switched-Inductor Z-Source Inverter Topologies

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Abstract

This paper proposes new active switched-capacitor and switched-inductor Z-source inverter (ASC/SL-ZSI) topologies, which can provide a higher boost ability with a small shoot-through time. The proposed ASC/SL-ZSIs inherit all of the advantages of the classical ZSI, and have a stronger voltage boost inversion ability when compared with the classical ZSI. Thus, the output ac voltage quality is significantly improved. In addition, more cells can be cascaded in the impedance network in order to obtain a very high boost ability. The proposed topologies can be applied to photovoltaic or fuel-cell generation systems with low-voltage renewal sources due to their wide range of obtainable voltages. Both simulations and the experimental results are carried out in order to verify performance of the proposed topologies.

Key words: Active switched-capacitor, Boost inversion ability, Multi-cell, Switched-inductor, Z-source inverter

I. INTRODUCTION

In a traditional PWM inverter, the ac output voltage is limited to below the dc input voltage. Therefore, an additional dc-dc boost converter is required to obtain a desired ac output voltage. In order to overcome the limitations of a traditional inverter, a Z-source inverter (ZSI) was introduced in [1]. The ZSI has a unique feature that allows it to boost the dc voltage by using the shoot-through operating mode, which is forbidden in a traditional PWM inverters. The ZSI provides a simple single stage approach for applications to any dc sources. However, because the shoot-through state is only regulated within a zero voltage state, the practical boost factor of the ZSI is seriously restricted. This disadvantage may limit further applications of the ZSI in application areas which require a high voltage gain to obtain a desired ac output voltage for low-voltage energy sources such as photovoltaic arrays, fuel-cell stacks, and batteries [2]-[6].

In order to increase the boost factor, several approaches have been introduced. In [7]-[10], a high-voltage was achieved by adjusting the turn-ratio of the transformer or coupled inductor. The switched-capacitor (SC), switched-inductor (SL), and hybrid switched-capacitor/switched-inductor combined with the classical ZSI topology were applied to dc-dc conversion in [11]-[14]. They provided a high-boost in cascade and transformer-less structures. However, additional inductors and/or capacitors at the impedance network are required for further boosting of the voltage, and they increase both the circuit volume and cost. The ZSI topology is suggested in order to reduce the capacitor voltage stress and suppress the rush currents at start-up [15]. A topology with an active SC and SL impedance network for reducing the number of passive components in the impedance network was proposed in [16]. However, the boosting ability was limited due to its one-cell structure.

In this paper, three different topologies based on the active switched-capacitor and switched-inductor Z-source inverter (ASC/SL-ZSI) are proposed, in order to obtain a higher boost ability. The operating principles for the three topologies are analyzed. The boost ability and voltage stress of the proposed

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topologies are compared with those of the classical ZSI. Both simulations and experimental results are carried out to validate the performance of the proposed topologies.

II. Operation Analysis of the Proposed Topologies

The operation principles for the three different topologies, which are named as ASC/SL-ZSI with one-cell, ASC/SL-ZSI with two-cells, and multi-cell ASC/SL-ZSI, will be described, respectively.

A. ASC/SL-ZSI with One-Cell

Fig. 1 shows the proposed impedance network, which consists of two inductors (L_1 and L_2), one capacitor (C), five diodes (D_{in}, D_1, D_2, D_3, and D_0), and one active switch (S_7).

The combination of L_1 - L_2 - D_1 - D_2 - D_3 acts on an SL cell, This SL cell is used to transfer and store energy from the capacitor to the dc–link bus by the switching actions of the inverter. The proposed inverter has two operation modes: a shoot-through state and a non-shoot-through state, which includes six active states and two zero states.

Shoot-through state: In the shoot-through state, the load terminal is shorted by conducting the upper and lower switching devices of any of the phase legs, and switching device S_7 is turned on. Diodes D_1 and D_2 are on, whereas diodes D_{in}, D_o, and D_3 are off. Fig. 2(a) shows an equivalent circuit in the shoot-through state for an interval of DT_s, where D is the shoot-through duty ratio and T_s is a switching period. The two inductor voltages v_{L1} and v_{L2}, and the dc-link voltage v_{pn} can be expressed as, respectively,

$$v_{L1} = v_{L2} = V_c \tag{1}$$

$$v_{pn} = 0 . \tag{2}$$

Non-shoot-through state: In the non-shoot-through state, the circuit operates under a traditional PWM inverter, and switching device S_7 is turned off. Diodes D_{in}, D_o, and D_3 are on, whereas diodes D_1 and D_2 are off. Fig. 2(b) shows an equivalent circuit in the non-shoot-through state for an interval of (1-D)T_s. The two inductor voltages v_{L1} and v_{L2}, and the dc-link voltage v_{pn} can be expressed as, respectively,

$$v_{L1\_NST} = V_{in} - V_c - v_{L2\_NST} \tag{3}$$

$$v_{L2\_NST} = V_{in} - V_c - v_{L1\_NST} \tag{4}$$

$$v_{pn} = V_c \tag{5}$$

where V_{in} is the dc source voltage, and v_{L1_NST} and v_{L2_NST} are the corresponding voltages across the two inductors L_1 and L_2 in the non-shoot-through state, respectively.

By applying the volt-second balance principle to inductor L_1, the corresponding voltage across L_1 in the non-shoot-through state is derived as

$$v_{L1\_NST} = v_{L2\_NST} = -\frac{D}{1-D} V_c . \tag{6}$$

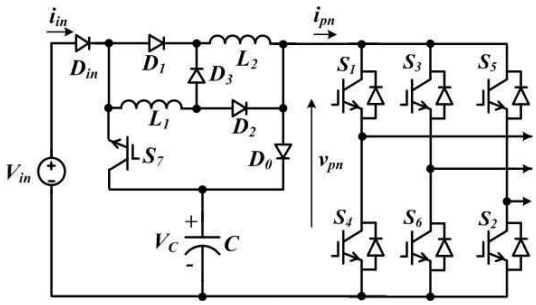


Fig. 1. Shematic circuit of the ASC/SL-ZSI with one-cell.

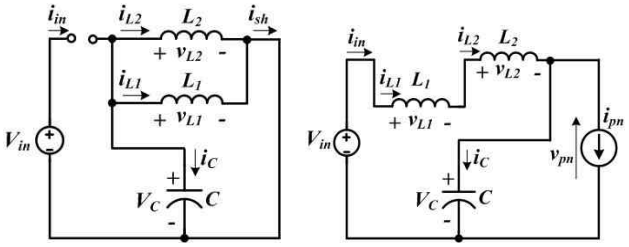


Fig. 2. Equivalent circuits of ASC/SL-ZSI with one-cell : (a) shoot-through state, (b) non-shoot-through state.

Since the average voltage across inductor L_2 is zero from (1), (3), and (4), the capacitor voltage is derived as

$$V_c = \frac{1-D}{1-3D} V_{in} . \tag{7}$$

Similarly, by applying the ampere-second balance principle to capacitor C, the two inductor currents can be derived as

$$i_{L1} = i_{L2} = \frac{1-D}{1-3D} i_{pn} . \tag{8}$$

The peak dc-link voltage across the inverter bridge is the same as V_C as in

$$\hat{v}_{pn} = V_c = \frac{1-D}{1-3D} V_{in} . \tag{9}$$

From (9), the boost factor B is expressed as the shoot-through duty ratio D.

$$B = \frac{\hat{v}_{pn}}{V_{in}} = \frac{1-D}{1-3D} \tag{10}$$

The shoot-through duty ratio D is limited to 1/3 by setting the denominator of (10) to be greater than zero.

Thus, the output peak phase voltage of the inverter is expressed by

$$\hat{v}_{ph} = M \cdot \frac{\hat{v}_{pn}}{2} = M \cdot B \cdot \frac{V_{in}}{2} \tag{11}$$

where M is the modulation index.

From (11), the voltage gain G can be defined and is derived as follows:

$$G = \frac{\hat{v}_{ph}}{V_{in}/2} = M \cdot B \tag{12}$$

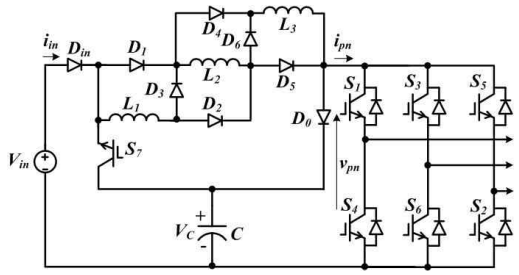
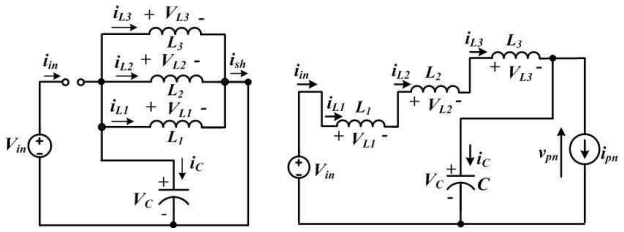


Fig. 3. Shematic circuit of the ASC/SL-ZSI with two-cells.



(a) (b)

Fig. 4. Equivalent circuits of ASC/SL-ZSI with two-cells: (a) shoot-through state, (b) non-shoot-through state.

B. ASC/SL-ZSI with Two-Cells

Fig. 3 shows the proposed ASC/SL-ZSI with two-cells. In order to increase the boost factor, one cell comprising one inductor and three diodes is added to the ASC/SL-ZSI with one-cell.

Fig. 4 shows equivalent circuits of the ASC/SL-ZSI with two-cells at the shoot-through state and the non-shoot-through state, respectively. By using a method similar to that used with the ASC/SL-ZSI with one-cell, the capacitor voltage, inductor currents, and peak dc-link voltage are derived as follows:

$$V_c = \frac{1-D}{1-4D} V_{in} \tag{13}$$

$$i_{L1} = i_{L2} = i_{L3} = \frac{1-D}{1-4D} i_{pn} \tag{14}$$

$$\hat{v}_{pn} = V_c = \frac{1-D}{1-4D} V_{in} = B \cdot V_{in} \tag{15}$$

From (15), the boost factor B is given by

$$B = \frac{\hat{v}_{pn}}{V_{in}} = \frac{1-D}{1-4D} \tag{16}$$

where D <1/4.

C. Multi-Cell ASC/SL-ZSI

A generalized multi-cell ASC/SL-ZSI is shown in Fig. 5. It can be extended to obtain a higher boost ability by cascading more cells, where the structure of one-cell is shown in the upper right corner. The n^{th} cell includes one inductor L_{n+1} and three diodes D_{3n-2}, D_{3n-1}, and D_{3n}.

In the shoot-through state, the inverter bridge is shorted, and switching device S_7 is turned on. During the shoot-through state, diodes D_{3n-2} and D_{3n-1} are on, whereas diodes D_{in}, D_o, and D_{3n} are off. All of the inductors from L_1 to L_{n+1} are connected in parallel. In the non-short-through state, switching device S_7 is turned off. During this state, diodes D_{in}, D_o, and D_{3n} are on, whereas diodes D_{3n-2} and D_{3n-1} are off. All of the inductors from L_1 to L_{n+1} are connected in series.

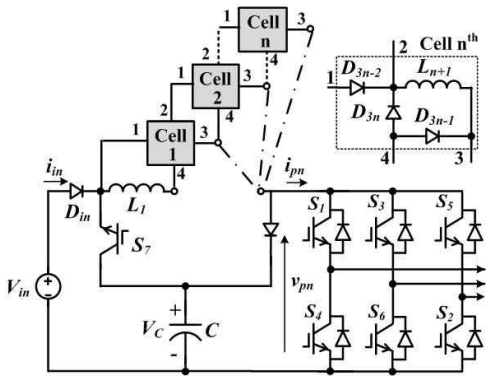


Fig. 5. Shematic circuit of the multi-cell ASC/SL-ZSI.

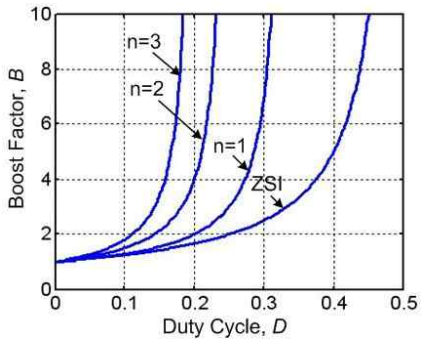


Fig. 6. Comparison of the boost ability for the multi-cell ASC/SL-ZSIs and ZSI.

By using a similar method to that used with the ASC/SL-ZSI with one-cell, the boost factor can be derived as

$$B = \frac{\hat{v}_{pn}}{V_{in}} = \frac{1-D}{1-(n+2)D}. \tag{17}$$

The boost factor can be easily increased by cascading more cells. Because the shoot-through duty ratio is limited to 1/(n+2) by setting the denominator of (17) to be positive, the multi-cell ASC/SL-ZSI uses a smaller shoot-through duty ratio at the same boost factor. Therefore, a higher modulation index is available for obtaining a better output voltage waveform.

In order to compare the boost ability of the proposed ASC/SL-ZSIs with that of the classical ZSI, Fig. 6 shows the boost factors of the classical ZSI and the ASC/SL-ZSIs when n is changed from 1 to 3. It can be seen that the boost factors of all the ASC/SL-ZSI topologies are higher than that of the ZSI. In addition, the boost factor can be easily increased by adding more cells.

III. PWM CONTROL TECHNIQUES

With the proposed topologies, the pulse width modulation (PWM) control has to be modified to effectively control the shoot-through state for boosting. The relationship between the modulation index M and the shoot-through duty ratio D depends on the PWM control method. Three PWM control methods such as the simple, maximum, and maximum constant boost control methods based on the traditional carrier based PWM technique are presented in [1], [17], [18]. In this paper, a simple boost control method is applied to the proposed topologies, because the shoot-through time per switching period is kept constant.

Fig. 7 shows the switching patterns of the simple boost control method. PWM signals are generated by comparing the three-phase reference voltages V_a^*, V_b^*, and V_c^* with a carrier signal. The shoot-through state is controlled by two shoot-through envelope signals V_p and V_n. When the carrier signal is higher than the upper shoot-through envelope V_p or lower than the lower shoot-through envelope V_n, the inverter operates in the shoot-through state. Switching devise S_7 is turned on during the shoot-through state. The obtainable shoot-through duty ratio D is limited to (1-M).

IV. COMPARISON WITH THE CLASSICAL ZSI

A. Comparison of the Number of Components

Table I shows the number of active and passive components used in the impedance networks of the ASC/SL-ZSI with one-cell and the classical ZSI without considering the common components used in the inverter bridge and output LC filter. As shown in Table I, the ASC/SL-ZSI with one-cell saves one capacitor. However, it requires more one active switch and more four diodes.

B. Comparison of the Voltage Stresses

From (11), the voltage stress across the switching devices of the inverter V_s for the ASC/SL-ZSI is the same as the peak dc-link voltage across the inverter bridge as $V_s = \hat{v}_{pn} = BV_{in}$. The voltage stress across the switching devices with the classical ZSI is expressed as $V_s = V_{in}/(1-2D)$ [1]. In order to properly compare the voltage stresses of the two inverters, an equivalent dc voltage is introduced [19]. The equivalent dc voltage is defined as the minimum dc voltage to produce an output voltage $\hat{v}_{ph}$, and it can be expressed as GV_{in} from (12). The ratio of the voltage stress across the switching devices to the minimum dc voltage for the classical ZSI and the ASC/SL-ZSI with one-cell can be derived as follows, respectively.

$$\frac{V_s}{G \cdot V_{in}} = \frac{B \cdot V_{in}}{G \cdot V_{in}} = 2 - \frac{1}{G} \quad \text{for classical ZSI} \quad (18)$$

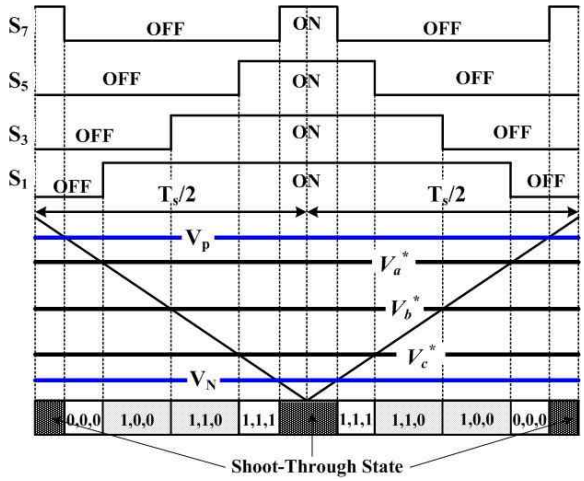


Fig. 7. Switching patterns under the simple boost control method.

TABLE I
NUMBER OF COMPONENT AT IMPEDANCE NETWORK

Component Type		Topology	
		ASC/SL-ZSI with one-cell	*Classical ZSI*
Switches	Active	1	0
	Passive	5	1
Passive components	Inductor	2	2
	Capacitor	1	2

$$\frac{V_s}{G \cdot V_{in}} = \frac{3G - \sqrt{9G^2 - 8G}}{G(9G - 4 - 3\sqrt{9G^2 - 8G})} \quad \text{for ASC/SL-ZSI} \quad (19)$$

Fig. 8 shows the voltage stress ratios for the classical ZSI and ASC/SL-ZSI with one-cell. It can be seen that the ASC/SL-ZSI with one-cell has a lower voltage stress across the switching devices than the classical ZSI.

In order to compare the capacitor voltage stresses of the two inverters, the ratios of the capacitor voltage stress to the input dc voltage for the classical ZSI and ASC/SL-ZSI with one-cell are derived as follows, respectively.

$$\frac{V_c}{V_{in}} = G \quad \text{for classical ZSI} \quad (20)$$

$$\frac{V_c}{V_{in}} = \frac{3G - \sqrt{9G^2 - 8G}}{9G - 4 - 3\sqrt{9G^2 - 8G}} \quad \text{for ASC/SL-ZSI} \quad (21)$$

The capacitor voltage stresses ratios for the two inverters are shown in Fig. 9. The capacitor voltage stress of the ASC/SL-ZSI with one-cell is higher than that of the classical ZSI, because the capacitor voltage is the same as the dc-link voltage with the ASC/SL-ZSIs.

V. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

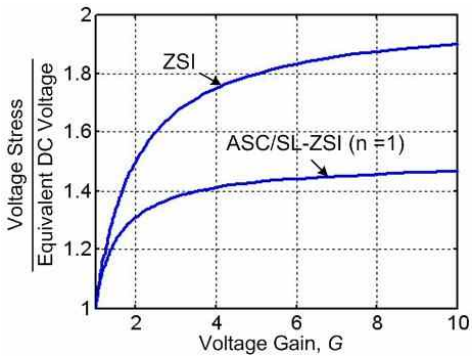


Fig. 8. Voltage stress ratios.

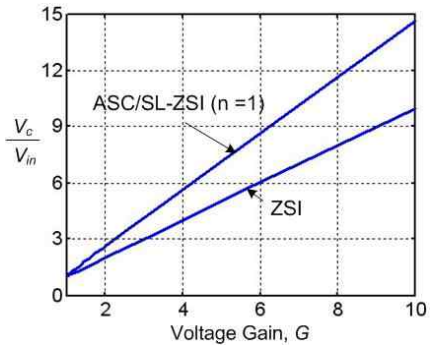


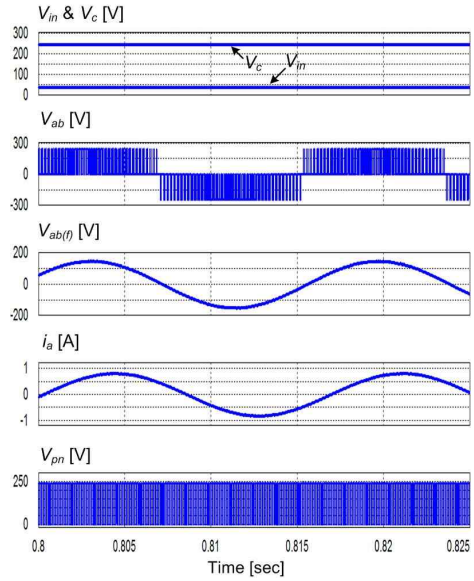
Fig. 9. Capacitor voltage stresses.

TABLE II
CIRCUIT PARAMETERS

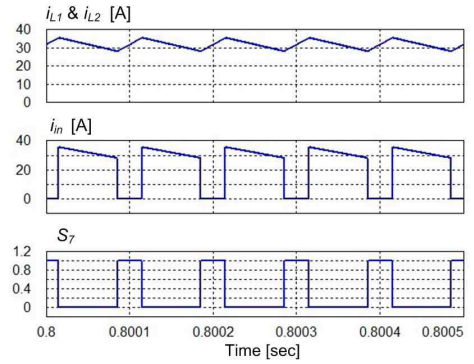
Input dc voltage, V_{dc}	40 V
Fundamental frequency, f	60 Hz
Switching frequency, f_s	5 kHz
Capacitor, C	500 μF
Inductor, $L_1 = L_2 = L_3$	1 mH
LC filter, L_f	0.6 mH
LC filter, C_f	100 μF
Load resistance, R_L	100 Ω

The circuit parameters used for the simulation and the experiment are shown in Table II. Fig. 10 shows the simulation results for the ASC/SL-ZSI with one-cell under the simple boost control when D = 0.295 and M = 0.705. From Fig. 10(a) it can be seen that the capacity voltage is boosted to 260 V from 40 V input dc voltage, and that a filtered peak line-to-line output voltage of 156 V can be produced. Fig. 10(b) shows the steady-state waveforms of the inductor and input currents, and the gating signal of switching device S_7. In the shoot-through state, the inductor current increases and the input current is zero. In the non-shoot-through state, the inductor current decreases and the input current is identical to the inductor current.

Fig. 11 shows the simulation results for the ASC/SL-ZSI



(a)



(b)

Fig. 10. Simulation results of ASC/SL-ZSI with one-cell. (a) Input and capacitor voltages, output voltage and current, and dc-link voltage. (b) Inductor and input currents and S_7 signal.

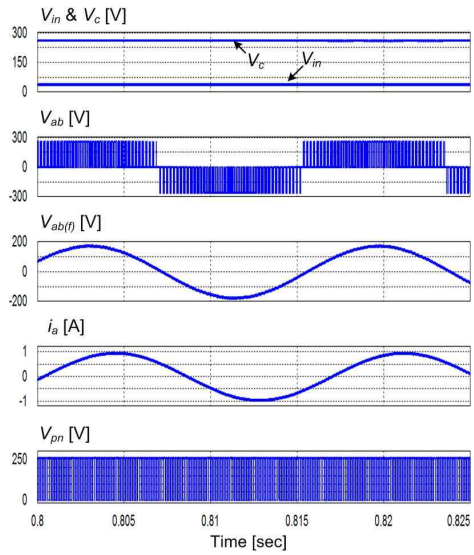


Fig. 11. Simulation results of ASC/SL-ZSI with two-cells.

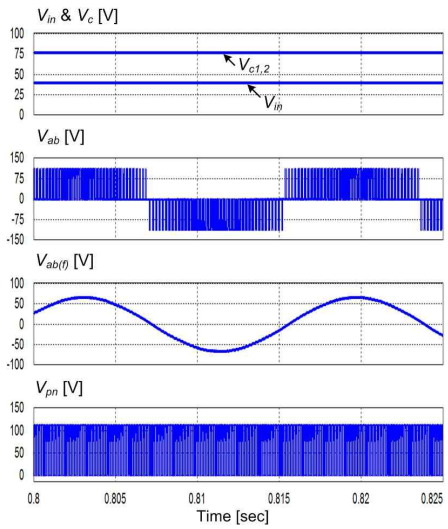


Fig. 12. Simulation results of classical ZSI.

Fig. 13. Photograph of experimental setup.

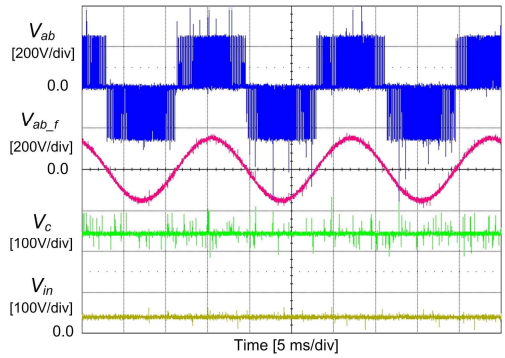
with two-cells, when $D = 0.22$ and $M = 0.78$. The capacitor voltage is boosted to 260 V and the peak line-to-line output voltage is 175 V. Compared with the simulation results shown in Fig. 10(a), the ASC/SL-ZSI with two-cells produces a higher output voltage when the capacitor voltage is identical, because a higher modulation index is available.

Fig. 12 shows the simulation results for the classical ZSI when $D = 0.295$ and $M = 0.705$. The capacity voltage is only boosted to 70 V from 40 V input dc voltage, and the filtered peak output line-to-line voltage is 69 V.

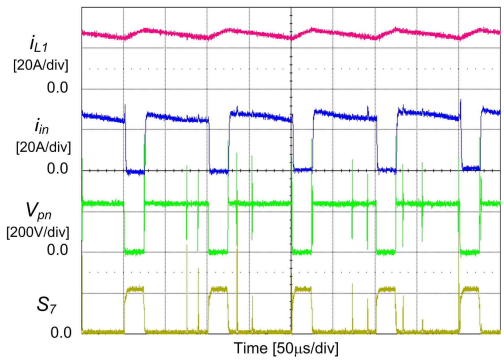
B. Experimental Results

A prototype of the ASC/SL-ZSI has been built in the laboratory for experiments. Fig. 13 shows a photograph of the experimental setup, which consists of an impedance network, a three-phase inverter, an LC filter, and a control board.

The control system is implemented by a 32-bit DSP-type TMS320F28335 operating at a clock frequency of 150MHz. The sampling period for the ASC/SC-ZSI control at the DSP is 100 μsec. The switching frequency of the inverter is determined to be 5 kHz, because the shoot-through duty ratio



(a)



(b)

Fig. 14. Experiments results of the ASC/SL-ZSI with one-cell at $M = 0.705$, $D = 0.295$, $V_{in} = 40$V: (a) output voltage, capacitor and input dc voltages, (b) inductor and input currents, dc-link voltage, and gating signal of S_7.

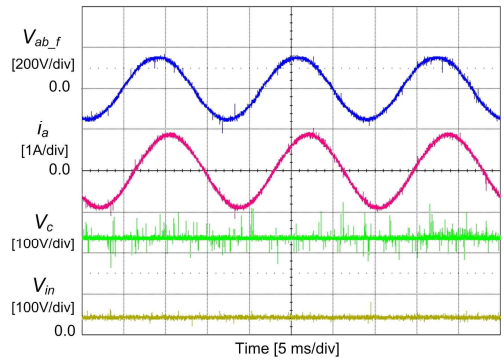


Fig. 15. Experiments results of the ASC/SL-ZSI with two-cells at $M = 0.78$, $D = 0.22$, $V_{in} = 40$V.

is controlled twice during one switching period T_s as shown in Fig. 7. The cut-off frequency of the LC filter is650 Hz, which is between the inverter frequency of 60 Hz and the switching frequency of 5 kHz. The parameters of the LC filter are described in Table II.

The experiment was performed with the same parameters and operating conditions as the simulation.

Fig. 14 shows the experimental results of the ASC/SL-ZSI with one-cell at $M = 0.705$, $D = 0.295$, and $V_{in} = 40$V, which are the same operating conditions used to obtain the

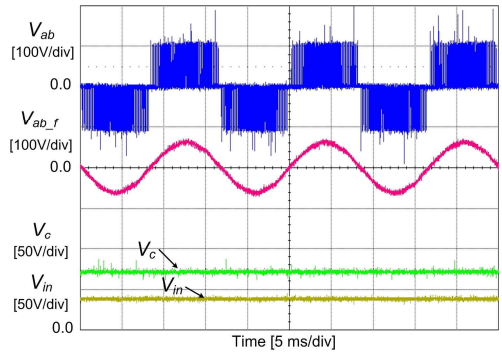


Fig. 16. Experiments results of the classical ZSI at M = 0.705, D = 0.295, V_{in} = 40V.

simulation result shown in Fig. 10. Fig. 14(a) shows the experimental waveforms of the line-to-line output voltage, the line-to-line output voltage filtered by an LC filter, the capacitor voltage, and the input dc voltage. The capacitor voltage is boosted to 250 V, which is slightly lower than the capacitor voltage in the simulation results due to both the forward voltage drop on the diodes and the parasitic resistance in the inductors. The peak line-to-line output voltage is 147 V, which is also slightly lower than the simulation results. Fig. 14 (b) shows the experimental waveforms of the inductor and input currents, the dc-link voltage, and the gating signal of switching device S_7.

Fig. 15 shows the experimental waveforms of the filtered line-to-line output voltage, the output current, the capacitor voltage, and the input dc voltage when M = 0.78, D = 0.22, and V_{in} = 40V. Compared with the experimental results shown in Fig. 14 (a), the capacitor voltage can be boosted to 250 V with a lower shoot-through duty ratio. In addition, the peak line-to-line output voltage is 164 V, which is higher than that of the ASC/SL-ZSI with one-cell. The a-phase output current lags to the line-to-line output voltage by 30° at the resistive load condition. Since a higher modulation index is available with the ASC/SL-ZSI with two-cells, a higher output voltage can be produced.

Fig. 16 shows the experimental results of the classical ZSI under the same operating conditions as those used to obtain the experimental results shown in Fig. 14. Compared with experiments results of the ASC/SL-ZSI with one-cell, both the boost factor and the ac voltage gain of the classical ZSI are 72% and 33% lower, respectively.

VI. CONCLUSIONS

This paper proposed three novel topologies with active switched-capacitor and switched-inductor impedance networks, which provide a high boost ability with a small shoot-through time. In comparison with the classical ZSI, the proposed ASC/SL-ZSI with one-cell provides a higher boost factor over the whole range of the shoot-through duty ratio. The voltage stress across the switching devices of the main inverter is lower at the same input dc voltage and output ac voltage. In addition, the proposed topology can be easily extended by cascading more cells in order to obtain a higher boost ability. However, the capacitor voltage stress is higher, because the capacitor voltage is identical to the peak dc-link voltage.

Both simulation studies and experimental results for the proposed ASC/SL-ZSIs and the classical ZSI are carried out, respectively, in order to verify the theoretical analysis. Through the experimental results, the capacitor voltage can be boosted to 250 V under 40 V input dc voltage. In addition, the output voltage of the ASC/SL-ZSI with two-cells is higher than that of the ASC/SL-ZSI with one-cell at the same capacitor voltage condition. Both the boost factor and the ac voltage gain of the ASC/SL-ZSI with one-cell are 350% and 150% higher than those of the classical ZSI, respectively, at the same modulation index, shoot-through duty ratio, and input dc voltage.

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