

Optimized Space Vector Pulse-width Modulation Technique for a Five-level Cascaded H-Bridge Inverter

Amarendra Matsa[†], Irfan Ahmed^{*}, and Madhuri A. Chaudhari^{*}

^{†*}Department of Electrical Engineering, Visvesvaraya National Institute of Technology, Nagpur, India

Abstract

This paper presents an optimized space vector pulse-width modulation (OSVPWM) technique for a five-level cascaded H-bridge (CHB) inverter. The space vector diagram of the five-level CHB inverter is optimized by resolving it into inner and outer two-level space vector hexagons. Unlike conventional space vector topology, the proposed technique significantly reduces the involved computational time and efforts without compromising the performance of the five-level CHB inverter. A further optimized (FOSVPWM) technique is also presented in this paper, which significantly reduces the complexity and computational efforts. The developed techniques are verified through MATLAB/SIMULINK. Results are compared with sinusoidal pulse-width modulation (SPWM) to prove the validity of the proposed technique. The proposed simulation system is realized by using an XC3S400 field-programmable gate array from Xilinx, Inc. The experiment results are then presented for verification.

Key words: Five-level cascaded H-bridge inverter, Optimized SVPWM, Power electronics, Space vector pulse-width modulation (SVPWM)

I. INTRODUCTION

The need for a high-power control apparatus has developed in various industrial applications in recent years. Thus, several multilevel converter structures have been introduced as alternatives to high-power and medium-voltage applications. Multilevel converters not only achieve high-power ratings but also achieve the integration of distributed generation (DG) sources. Multilevel converters have three principal topologies [1], [2]. Among which, the cascaded H-bridge (CHB) topology is the most suitable for DG sources [3]. Pulse-width modulation (PWM) techniques for multilevel converters have been studied extensively during the last few decades. A wide variety of methods, which are different in concepts and performances, have been developed to achieve one or more of the following objectives:

- wide linear modulation range
- less switching losses
- decreased total harmonic distortion (THD)

- easy implementation and less computational time [4], [5].

The space vector pulse width modulation (SVPWM) technique provides superior harmonics capacity and solves the problem of unbalanced capacitor voltages by using redundant states in the space voltage vector plane. Thus, many methods have been developed to implement SVPWM to drive voltage-source inverters [2]-[16]. SVPWM implementation generally involves identifying sectors, determining switching vectors, and selecting optimum switching sequences for inverters [6], [7]. Blasko provided a classical SVPWM technique with an equal duration of zero-state vector V_0 application, whereas V_7 was modified. A factor-variable K_o that is proportional to the time of application of vector V_7 was introduced. By changing K_o from zero to one, the duration of V_7 application can be changed from 0% to 100% of the combined application time for zero-state vectors. A correlation between the modified space-vector and triangle-comparison methods (with added zero sequence) was established [8]. Celanovic introduced a new and computationally efficient space vector modulation (SVM) algorithm for general n -level converters. This algorithm can be implemented on nearly any commercially available digital signal processor and is suited for execution in real time;

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[†]Corresponding Author: amarmeetsyou@gmail.com
 Tel: +91-9492904858, Visvesvaraya National Institute of Technology
^{*}Dept. of Electrical Eng., Visvesvaraya Nat'l Institute of Tech., India

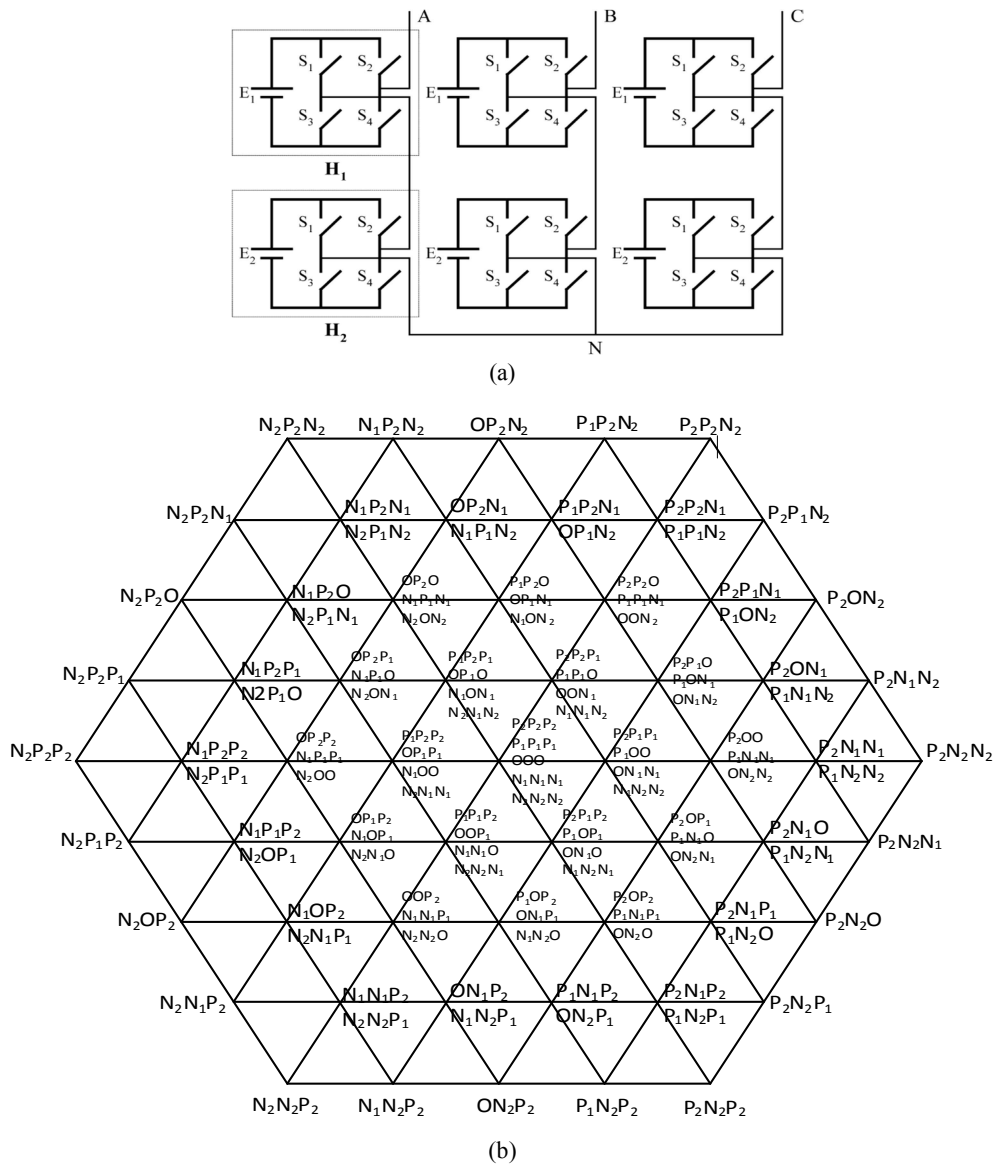


Fig. 1. (a) Five-level CHB inverter.(b) SVD of a five-level inverter.

however, this method is more complex than others[9].Seo proposed a simplified SVPWM method for a three-level inverter. This method is based on the simplification of the space vector diagram (SVD) of a three-level inverter into that of a two-level inverter [10].Perales developed a 3D space vector algorithm for a multilevel converter to compensate for the harmonics and zero-sequence components of the system. This algorithm is useful in systems with or without neutrality, unbalanced load, and triple harmonics, as well as for generating 3D control vectors[11].Ahmed also developed a new simplified SVPWM technique for a seven-level inverter. This technique can reduce the complexity of an SVD [12].

The schematic structure of a five-level CHB inverter is shown in Fig. 1(a) and its SVD is shown in Fig.1(b).

This inverter has five possible output voltage levels for each phase. The levels, which range from $+2E$ (corresponding to P_2) to $-2E$ (corresponding to N_2), result in $5^3 = 125$ possible space

vectors for the inverter. The number of independent space vectors is $(3n^2-3n+1) = 61$, where $n = 5$ for the five levels. $(n - 1) = 4$ layers and $(n - 1)^3 = 64$ triangles are found in the SVD.

This paper proposes an optimized technique for SVPWM (OSVPWM) of a five-level CHB multilevel inverter. This technique considerably reduces calculation time, complexity, and efforts involved in constructing the SVD of a five-level CHB inverter. Based on the geometric simplification of the SVD, the proposed method reduces the number of two-level hexagons that should be considered from 36 to 24 (18 outer + 6 inner) for a five-level inverter. A further OSVPWM (FOSVPWM) technique is also proposed in this paper which further reduces the number of two-level hexagons to 18.The simulation results of both techniques for a five-level CHB inverter are presented and compared with the results of the sinusoidal PWM technique (SPWM) to validate the proposed methods.

II. PROPOSED OSVPWM TECHNIQUE

The basic idea of OSVPWM is based on the concept of resolving a five-level SVD[Fig. 1(b)] into inner and outer two-level hexagons. The selectivity of the inner and outer regions depends on the magnitude of V_{ref} . If V_{ref} magnitude is less than $2E$, then the inner region is selected; otherwise, the outer region is selected as shown in Fig. 2. The hexagons in the outer or inner region are selected based on the angle θ of the original reference voltage. When V_{ref} is more than $2E$, the outer region hexagons are selected. Selecting a particular hexagon in the outer region depends on angle θ as shown in Table I.

When an outer hexagon is selected, a new reference vector V_{refo2} is generated, such that it originates from the center of the outer two-level hexagons. The tip of this new vector coincides with the tip of V_{ref5} . Consider the case of hexagon I(OH1) shown in Fig.3. Vector V_{refo2} is related to V_{ref5} based on the following relations:

$$V_{o2\alpha} = V_{5\alpha} - 3E, \quad (1)$$

$$V_{o2\beta} = V_{5\beta}, \quad (2)$$

where $V_{5\alpha}, V_{5\beta}$ and $V_{o2\alpha}, V_{o2\beta}$ are the components of V_{ref5} and V_{refo2} along the real and imaginary axes, respectively. The mapping of all V_{refo2} hexagons is described in Table II.

Vector V_{refo2} for each of the outer hexagons has a modulation index ranging from zero to unity and an angle θ_{o2} ranging from zero to 2π . Angle θ_{o2} is also applied to each of the outer hexagons. When the inner two-level hexagons (IH) are selected, reference vector V_{ref5} is mapped to the inner two-level hexagon center reference vector V_{refi2} as shown in Fig. 4. The appropriate selection of IH depends on angle θ_5 . The process of selecting an appropriate inner two-level hexagon is described in Table III. Consider the case of selecting an inner two-level hexagon1 (IH1) as shown in Fig. 5. Reference vectors V_{refi2} and V_{ref5} are related as follows:

$$V_{i2\alpha} = V_{5\alpha} - E, \quad (3)$$

$$V_{i2\beta} = V_{5\beta}, \quad (4)$$

where $V_{5\alpha}, V_{5\beta}$ and $V_{i2\alpha}, V_{i2\beta}$ are the components of V_{ref5} and V_{refi2} along the α and β axes, respectively. The computation V_{refi2} of all six inner two-level hexagons is described in Table 4.

III. DWELL TIME CALCULATION AND SWITCHING SEQUENCE DESIGN

Dwell time calculation and switching sequence generation for the selected two-level hexagon can be performed in a manner similar to that in the conventional two-level SVPWM technique. Each two-level hexagon is divided into six sectors.

The sector in reference vector V_{refo2} depends on its angle θ_{o2} . V_{refo2} can then be synthesized by the three stationary vectors of that sector. Dwell time calculation for the stationary vectors is performed based on the "volt-second-balancing" principle. The outer region two-level

TABLE I

SELECTION OF OUTER TWO-LEVEL HEXAGONS	
Range of θ	Hexagon number
-15° to +15°	OH1
+15° to +30°	OH2
+30° to +45°	OH3
+45° to +75°	OH4
+75° to +90°	OH5
+90° to +105°	OH6
+105° to +135°	OH7
+135° to +150°	OH8
+150° to +165°	OH9
+165° to -165°	OH10
-165° to -150°	OH11
-150° to -135°	OH12
-135° to -105°	OH13
-105° to -90°	OH14
-90° to -75°	OH15
-75° to -45°	OH16
-45° to -30°	OH17
-30° to -15°	OH18

hexagon OH1 and reference voltage V_{refo2} lie in Sector I as shown in Fig.5.

Vectors V_1 ($P_2N_2N_2$), V_2 ($P_2N_1N_2$) and $P_2N_1N_1, P_2N_2N_2$ are zero voltage vectors V_0 . The volt-second-balancing equation for this sector is given as follows:

$$V_{refo2}T_s = V_1T_a + V_2T_b + V_0T_0, \quad (5)$$

where T_s is the sampling interval; and T_a , T_b , and T_0 are the respective dwell times for vectors V_1 , V_2 , and V_0 .

The values of T_a , T_b , and T_0 are given as follows:

$$T_a = T_s \times m_a \sin\left(\frac{\pi}{3} - \theta\right), \quad (6)$$

$$T_b = T_s \times m_a \sin\theta, \quad (7)$$

$$T_0 = T_s - T_a - T_b, \quad (8)$$

where m_a is the modulation index defined as follows:

$$M_a = \sqrt{3} \frac{V_{ref}}{E}. \quad (9)$$

After calculating dwell time intervals, an appropriate design for the switching sequence is required. The typical seven-segment switching sequence is used in this scheme. The switching sequence should be designed, such that a change from one switching state to the next involves only one leg, and a change from one sector to the next involves zero or a minimum number of switching [1]. With these constraints, the seven-segment switching sequence for vector V_{refo2} Sector I shown in Fig.5 is given as follows:

$(P_1N_2N_2), (P_2N_2N_2), (P_2N_1N_2), (P_2N_1N_1), (P_2N_1N_2), (P_2N_2N_2), (P_1N_2N_2)$.

Similarly, the switching sequence for Sector II is given as follows:

$(P_1N_2N_2), (P_2N_2N_2), (P_2N_1N_2), (P_2N_1N_1), (P_2N_1N_2), (P_2N_2N_2), (P_1N_2N_2)$.

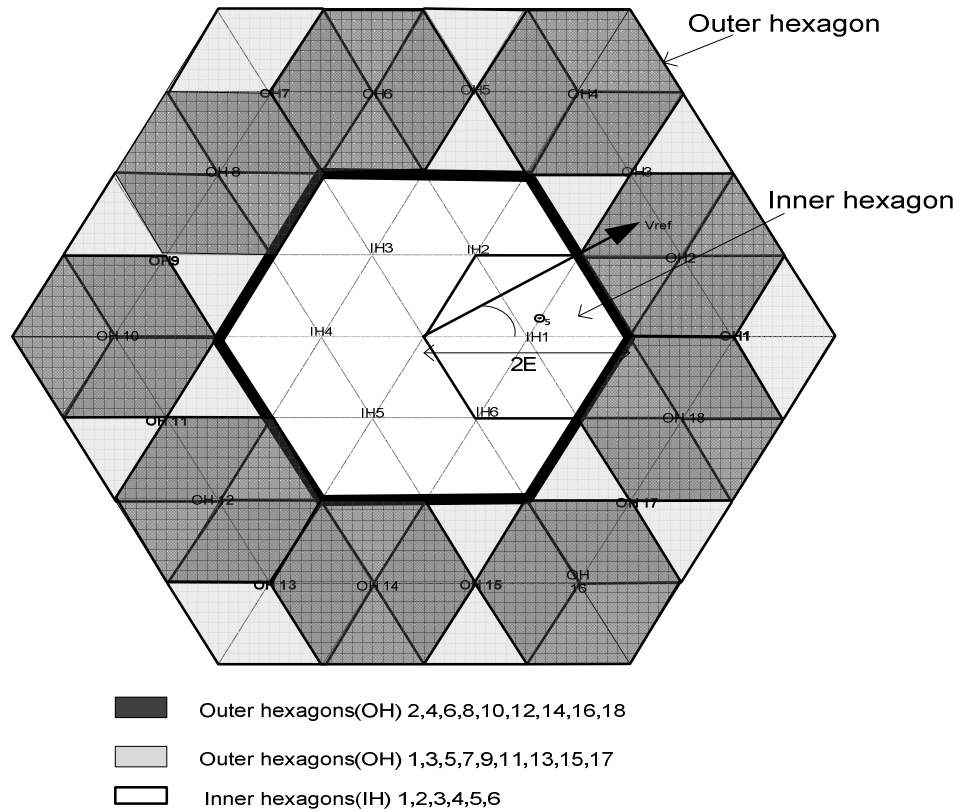


Fig. 2. Selection of inner and outer regions.

TABLE II
MAPPING OF V_{REF02} FROM V_{REF5}

Hexagon number	$V_{O2\alpha}$	$V_{O2\beta}$
OH1	$V_{5\alpha} - 3E$	$V_{5\beta}$
OH2	$V_{5\alpha} - 2.598076211E \cos\frac{\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{\pi}{9}$
OH3	$V_{5\beta} - 2.598076211E \sin\frac{\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{2\pi}{9}$
OH4	$V_{5\alpha} - 3E \cos\frac{\pi}{3}$	$V_{5\beta} - 3E \sin\frac{\pi}{3}$
OH5	$V_{5\alpha} - 2.598076211E \cos\frac{4\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{4\pi}{9}$
OH6	$V_{5\alpha} - 2.598076211E \cos\frac{5\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{5\pi}{9}$
OH7	$V_{5\alpha} - 3E \cos\frac{2\pi}{3}$	$V_{5\beta} - 3E \sin\frac{2\pi}{3}$
OH8	$V_{5\alpha} - 2.598076211E \cos\frac{7\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{7\pi}{9}$
OH9	$V_{5\alpha} - 2.598076211E \cos\frac{8\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{8\pi}{9}$
OH10	$V_{5\alpha} + 3E$	$V_{5\beta}$
OH11	$V_{5\alpha} - 2.598076211E \cos\frac{10\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{10\pi}{9}$
OH12	$V_{5\alpha} - 2.598076211E \cos\frac{11\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{11\pi}{9}$
OH13	$V_{5\alpha} - 3E \cos\frac{4\pi}{3}$	$V_{5\beta} - 3E \sin\frac{4\pi}{3}$
OH14	$V_{5\alpha} - 2.598076211E \cos\frac{13\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{13\pi}{9}$
OH15	$V_{5\alpha} - 2.598076211E \cos\frac{14\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{14\pi}{9}$
OH16	$V_{5\alpha} - 3E \cos\frac{5\pi}{3}$	$V_{5\beta} - 3E \sin\frac{5\pi}{3}$
OH17	$V_{5\alpha} - 2.598076211E \cos\frac{16\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{16\pi}{9}$
OH18	$V_{5\alpha} - 2.598076211E \cos\frac{17\pi}{9}$	$V_{5\beta} - 2.598076211E \sin\frac{17\pi}{9}$

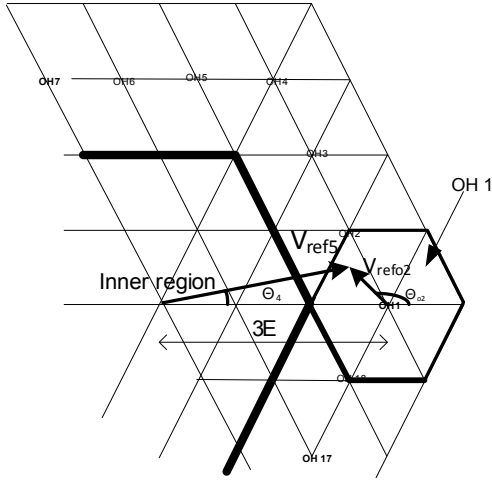


Fig. 3. Outer two-level hexagon reference point mapping.

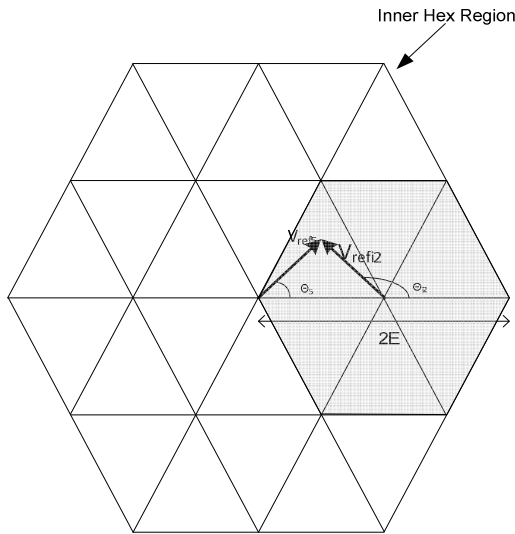


Fig. 4. Inner two-level hexagon reference point mapping.

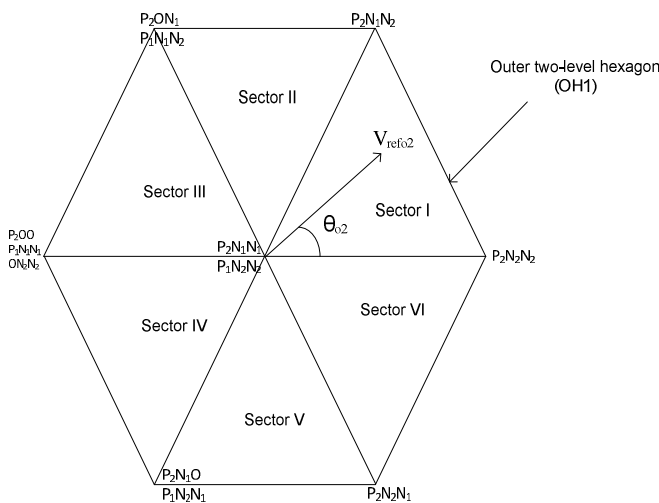


Fig. 5. Outer region two-level hexagon OH1.

TABLE III

SELECTION OF INNER TWO-LEVEL HEXAGONS	
Range of θ	Hexagon number
-30° to $+30^\circ$	IH1
$+30^\circ$ to $+90^\circ$	IH2
$+90^\circ$ to $+150^\circ$	IH3
$+150^\circ$ to -150°	IH4
-150° to -90°	IH5
-90° to -30°	IH6

TABLE IV

MAPPING OF V_{REFI2} FROM V_{REF5}		
Hexagon	$V_{i2\alpha}$	$V_{i2\beta}$
IH1	$V_{5\alpha} - E$	$V_{5\beta}$
IH2	$V_{5\alpha} - E \cos \frac{\pi}{3}$	$V_{5\beta} - E \sin \frac{\pi}{3}$
IH3	$V_{5\alpha} - E \cos \frac{2\pi}{3}$	$V_{5\beta} - E \sin \frac{2\pi}{3}$
IH4	$V_{5\alpha} + E$	$V_{5\beta}$
IH5	$V_{5\alpha} - E \cos \frac{4\pi}{3}$	$V_{5\beta} - E \sin \frac{4\pi}{3}$
IH6	$V_{5\alpha} - E \cos \frac{5\pi}{3}$	$V_{5\beta} - E \sin \frac{5\pi}{3}$

TABLE V

SELECTION OF THE OUTER TWO-LEVEL HEXAGONS IN THE FOSVPWM TECHNIQUE	
Range of θ	Hexagon number
$+0^\circ$ to $+30^\circ$	OH2
$+30^\circ$ to $+60^\circ$	OH3
$+60^\circ$ to $+90^\circ$	OH5
$+90^\circ$ to $+120^\circ$	OH6
$+120^\circ$ to $+150^\circ$	OH8
$+150^\circ$ to $+180^\circ$	OH9
-180° to -150°	OH11
-150° to -120°	OH12
-120° to -90°	OH14
-90° to -60°	OH15
-60° to -30°	OH17
-30° to -0°	OH18

IV. FOSVPWM

This technique further reduces the number of two-level hexagons that should be considered. Consequently, it decreases the complexity and efforts involved in the SVPWM of a five-level inverter. A five-level SVD for this technique is initially resolved into inner and outer regions, similar to in the OSVPWM technique. Thus, the number of two-level hexagons that should be considered for the FOSVPWM of a five-level inverter is reduced to 18. The modulation index M_a for SVM is defined as the maximum value ($M_a = 1$) that corresponds to the radius of the largest circle that can be inscribed in the SVD. The five-level SVD with such a circle is shown in Fig. 6.

If only 12 are considered (even for $M_a = 1$), then only the dark shaded portion of the SVD is left unattended. If this area is ignored, then the SVM of a five-level inverter involves only 18 two-level hexagons. Selecting the appropriate two-level hexagon depends on the magnitude and

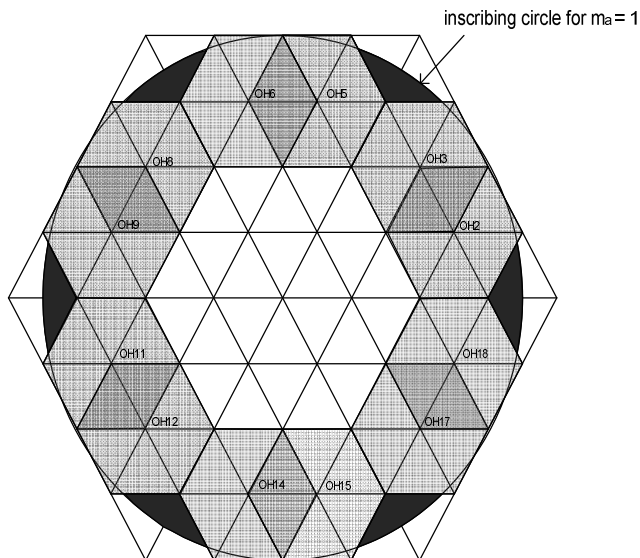


Fig. 6. Five-level SVD with an inscribing circle for $M_a = 1$.

TABLE VI

SIMULATION PARAMETERS USED FOR FIVE-LEVEL CHB INVERTER

H-bridge DC supply voltage	$E = 600 \text{ V}$
System frequency	$f = 50 \text{ Hz}$
Three-phase resistive load (star)	$R_L = 100 \Omega$

angle of reference vector V_{ref5} described in Table V.

The decrease in complexity is achieved at the cost of a slightly increased THD of the output voltage. This increase is only for $M_a > 0.75$, where M_a is the modulation index for the five-level SVD. If the tip of vector V_{ref5} lies in the dark unattended portion, then one of the OHs is selected depending on the angle θ_s of V_{ref5} . A new reference vector V_{refo2} is then generated, as in the case of the OSVPWM technique, with its origin located at the center of the selected two-level hexagon.

V. SIMULATION RESULTS

The proposed methods are simulated with MATLAB/SIMULINK. The simulation is conducted for a five-level CHB inverter at different values of the modulation index M_a . The results are compared with those of the conventional SPWM technique to validate the viability of the proposed techniques. The simulation parameters are shown in Table VI, and the simulation results are shown in Figs. 7 and 8 for the modulation indices $M_a = 1.0$ and $M_a = 0.8$, respectively.

The sampling frequency for the SVM schemes is generally preferred as $6N$ times the output frequency, where N is an integer. The sampling frequency for the SVM schemes is $f_s = 1.5 \text{ kHz}$, assuming a value of $N = 5$. For the SPWM schemes, the sampling frequency should be $[(2N + 1) \times 3]$ times the output frequency [17], [18]. Thus, $f_s = 1.65 \text{ kHz}$ for these

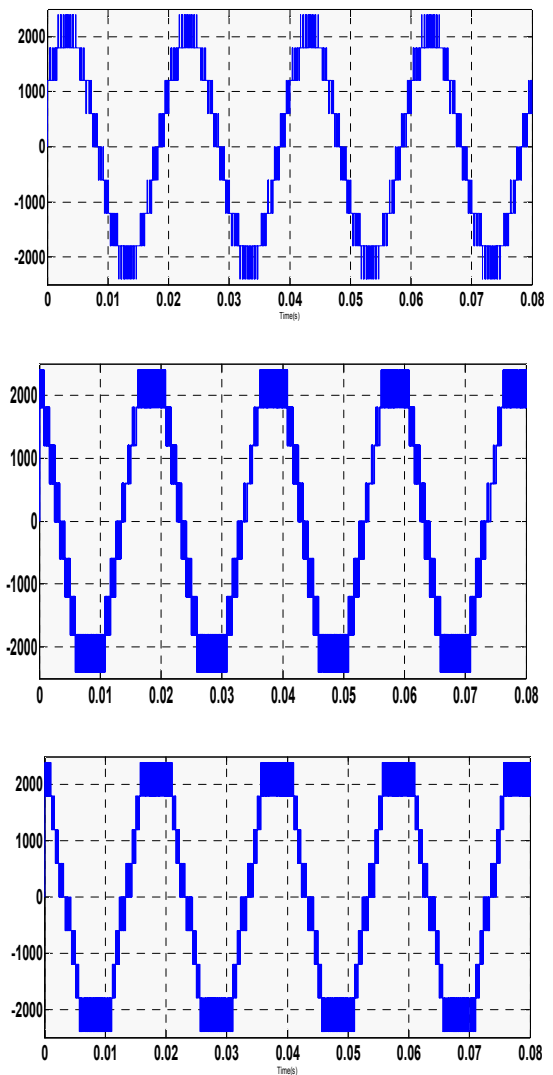


Fig. 7. Output line voltage waveforms at $M_a = 1$ for SPWM, OSVPWM and FOSVPWM. (b) OSVPWM. (c) FOSVPWM.

TABLE VII

THD AND PEAK VALUE OF FUNDAMENTAL COMPONENT (V1M) OF OUTPUT LINE VOLTAGE

Modulation Technique	SPWM	OSVM	FOSPWM
$M_a = 1.0$ THD, %	17.12	20.67	21.55
V1m, V	2106	2348	2265
$M_a = 0.8$ THD, %	21.71	22.99	24.09
V1m, V	1708	2216	2172
$M_a = 0.6$ THD, %	25.61	29.2	29.2
V1m, V	1321	1824.6	1824.6
$M_a = 0.4$ THD, %	42.15	38.58	38.58
V1m, V	1184.3	1688	1688
$M_a = 0.2$ THD, %	91.87	49.96	49.96
V1m, V	718	1326	1326

schemes. Table VII shows the THD of the output line voltage and the peak magnitude of the fundamental components at various M_a values.

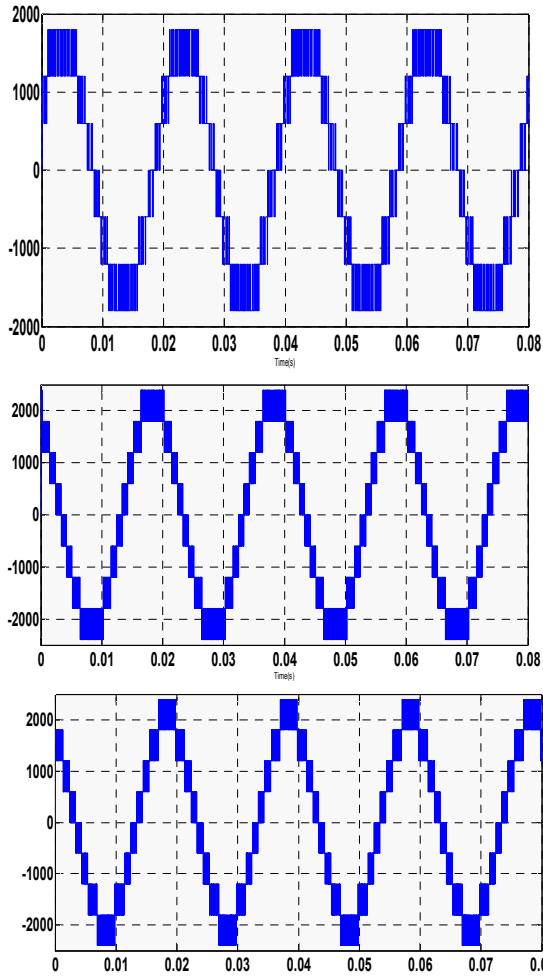
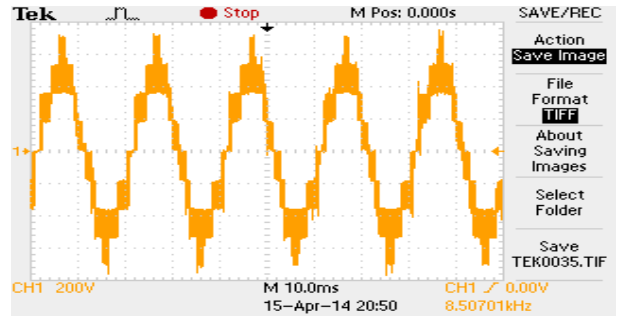


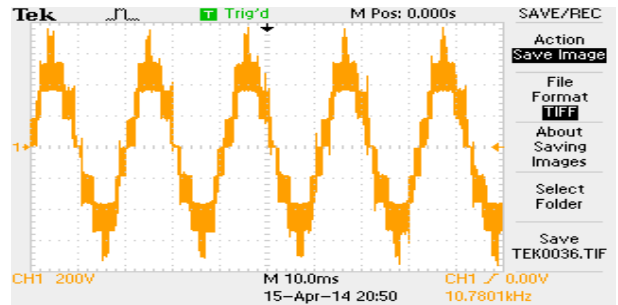
Fig. 8. Output line voltage waveforms at $M_a = 0.8$ for SPWM, OSVPWM and FOSVPWM. (a) SPWM. (b) OSVPWM. (c) FOSVPWM.



Fig. 9. Experimental setup of Five-level H-Bridge Inverter.

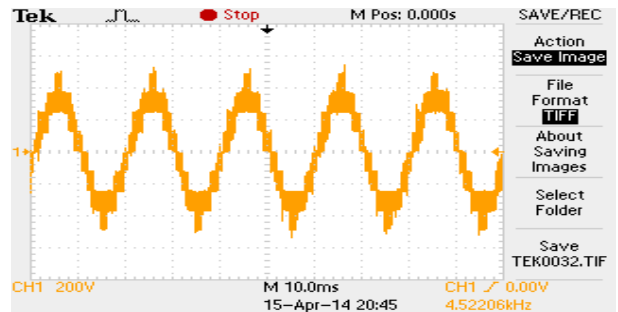


(a) OSVPWM.

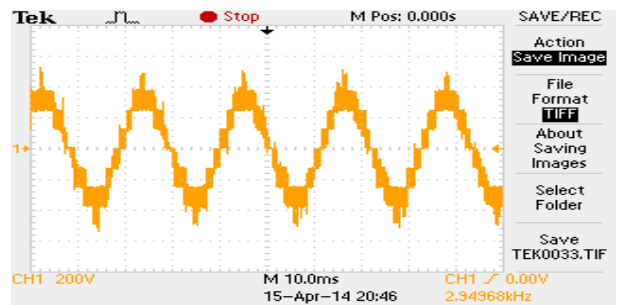


(b) FOSVPWM.

Fig. 10. Output line voltage waveforms at $M_a = 1$ for OSVPWM and FOSVPWM.



(a) OSVPWM.



(b) FOSVPWM.

Fig. 11. Output line voltage waveforms at $M_a = 0.8$ for OSVPWM and FOSVPWM.

TABLE VIII
EXPERIMENTAL PARAMETERS USED FOR FIVE-LEVEL CHB
INVERTER

H-bridge DC supply voltage	$E = 200 \text{ V}$
System frequency	$f = 50 \text{ Hz}$
Three-phase resistive load (star)	$R_L = 1.5 \text{ K}\Omega$

These results show that the proposed optimized techniques are comparable with the established SPWM schemes. The proposed techniques exhibit satisfactory performance for all values of the modulation index M_a . The THD obtained with these techniques is slightly higher than that obtained with the SPWM scheme. In addition, the fundamental components of the output voltage obtained with these schemes are higher than those obtained with the SPWM scheme. The proposed schemes also exhibit significant improvement over the SPWM scheme for low values of M_a . In particular, for $M_a \leq 0.2$, the FOSVPWM scheme presents remarkable improvement in performance over the SPWM scheme. This condition is advantageous in applications wherein the inverter may sometimes be required to operate at low modulation indices.

Thus, the proposed techniques perform comparably with the previously proposed SVM techniques for multilevel inverters while considerably optimizing the control algorithm.

VI. EXPERIMENT RESULTS

An experimental study was conducted to confirm the proposed control methods. Experimental set up as shown in Fig.9, in which two H-bridges are connected in series per phase. An XC3S400 field-programmable gate array (FPGA) from Xilinx, Inc. (California, USA) was used to realize the proposed control schemes. The experimental system parameters are listed in Table VIII.

VII. CONCLUSIONS

This study presents the OSVPWM technique that optimizes the SVPWM of multilevel inverters. The proposed technique is based on resolving the multilevel inverter SVD into inner and outer region two-level hexagons. This technique is general and can be applied to the SVPWM of all three principal topologies for multilevel converters at any number of levels. The advantage of applying this technique increases as the number of levels increases.

An FOSVPWM technique has also been presented for the SVM of a five-level inverter. This technique reduces the complexity and effort required for the SVPWM of a five-level inverter by nearly 50%. In particular, the OSVPWM technique reduces the five-level SVPWM to a SVPWM problem of 24 two-level hexagons. The FOSVPWM technique further reduces this number to 18.

The simulation results for both techniques are presented for a five-level CHB inverter. The results are compared with those of the SPWM technique, which proves the validity of the proposed techniques for different values of the modulation index. The experiment results are then provided for the proposed methods to verify the correctness of the real-time simulation system. The FPGA-based real-time

emulation will be a popular component of real-time simulation. The application of these techniques significantly reduces the complexity and efforts involved in the SVPWM of higher level inverters.

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Amarendra Matsa was born in Andhra Pradesh, India on August 23, 1984. He received his B.Tech and M.Tech degrees from Jawaharlal Nehru Technological University, Hyderabad, India in 2006 and 2009, respectively. He is currently pursuing his Ph.D. at Visvesvaraya National Institute of Technology (VNIT), Nagpur, India. His current research interests include power electronics, new control algorithm techniques for grid-integrated distributed generation, and microgrids.



Irfan Ahmed received his B.E. (Electrical Engineering) from Nagpur University, India, in 2001, and M.Tech (Power Electronics, machines, and drives) from the Indian Institute of Technology, Roorkee, India, in 2004. From 2004 to 2011, he worked as a faculty member at Anjuman College of Engineering and Technology, Nagpur, India. He is currently pursuing his Ph.D. at the Department of Electrical and Electronics Engineering, VNIT, Nagpur, India. His research interests include power electronics and its applications to power systems and drives



Madhuri A. Chaudhari was born in Maharashtra, India on January 28, 1968. She received her B.E. from Amaravati University, Amaravati, India; M.Tech from Visvesvaraya Regional College of Engineering, Nagpur University, Nagpur, India; and Ph.D. from VNIT, Nagpur, India (all in electrical engineering). She is currently an associate professor at the Department of Electrical Engineering, VNIT. Her research interests are in the areas of power electronics, FACTS, and AC-DC drives. Dr. Chaudhari is a member of the IEEE, the Institution of Engineers (India), and the Indian Society for Technical Education.