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A Canonical Small-Signal Linearized Model and a Performance Evaluation of the SRF-PLL in Three Phase Grid Inverter System

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Abstract

Phase-locked loops (PLL) based on the synchronous reference frame (SRF-PLL) have recently become the most widely-used for grid synchronization in three phase grid-connected inverters. However, it is difficult to study their performance since they are nonlinear systems. To estimate the performances of a SRF-PLL, a canonical small-signal linearized model has been developed in this paper. Based on the proposed model, several significant specifications of a SRF-PLL, such as the capture time, capture rang, bandwidth, the product of capture time and bandwidth, and steady-state error have been investigated. Finally, a noise model of a SRF-PLL has been put forward to analyze the noise rejection ability by computing the SNR (signal-to-noise ratio) of a SRF-PLL. Several simulation and experimental results have been provided to verify and validate the obtained conclusions. Although the proposed model and analysis method are based on a SRF-PLL, they are also suitable for analyzing other types of PLLs.

Key words: Noise model, Noise rejection ability, Performance evaluation, Small-signal linearized model, SRF-PLL

I. INTRODUCTION

A grid-connected inverter perfectly matches the philosophy of a phase-locked loop (PLL), since it should operate in harmony with the utility voltage. It should phase-lock its internal oscillator to the positive sequence voltage at the fundamental frequency in three phase systems to produce an amplitude and phase-coherent utility voltage that is applied to control grid-connected inverters or micro-grid inverters, such as distributed generation and storage systems, flexible ac transmission systems (FACTS), power line conditioners and uninterruptible power supplies (UPS) [1], [2]. Regardless of the detection approach used, it should work as quickly and accurately as possible, even if the utility voltage is distorted and unbalanced.

There are three main detection approaches in the literature. They are the zero-cross phase detection method, the stationary reference frame phase detection method, and the synchronous reference frame phase detection method [3]. A conversional grid-connected inverter offers a low degree of control and is synchronized to the utility by detecting the zero-crossing of the utility voltage. This assumes that the magnitude of the utility is well known and that the frequency is kept constant. This technique suffers from some drawbacks, such as inaccuracy and the detection of multiple zero-crossings in the case of a distorted grid voltage. To overcome these drawbacks, some modified methods based on comparators circuits with dynamic hysteresis [4], curve-filters [5] or predictive digital filtering algorithms [6] have been proposed. Since these methods employ a comparator as phase detector (PD) for detecting changes in the polarity of the grid voltage, the phase sensitivity should be U_g/π for a single phase system, and $3U_g/\pi$ for three phase voltages, where U_g is the phase magnitude of the utility voltage. A PI controller is used as a loop filter. More importantly, it has a small-signal linearized model that is identical to that of the conventional SRF-PLL.

The most popular and essential technique is a three-phase locked loop based on the synchronous reference frame [7].

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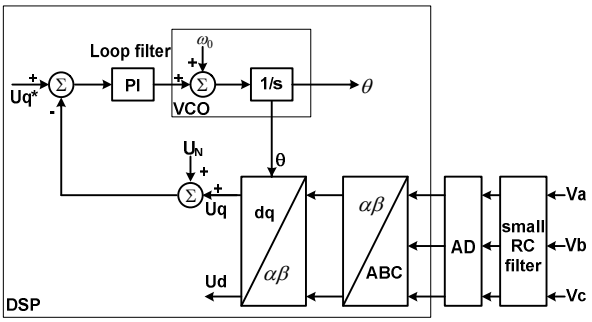


Fig. 1. General structure of conventional SRF-PLL.

This is often referred as the conventional SRF-PLL [8]. Since a PLL contains a phase detector, it is a nonlinear system, which is difficult for one to predict the electrical properties. Based on the operational principle of the conventional SRF-PLL, a canonical small-signal linearized model has been developed in Section II.

Based on this model, several significant specifications of the SRF-PLL, such as the capture time, capture rang, bandwidth, the product of capture time and bandwidth have been investigated in Section III. Then, the steady-state errors under various operation conditions, such as phase step, frequency step, amplitude step, amplitude ramp and so on, have also been discussed. These various operation conditions correspond to some practical cases, such as the phase jump of the utility voltage, low-voltage ride-through, and micro-grid inverters working in the island condition by employing the frequency droop control.

In Section IV, a noise model of the SRF-PLL has been put forward to estimate its performance in the presence of noise. By applying the proposed noise model, the noise rejection ability by computing the SNR of the SRF-PLL has been investigated. Several simulation and experimental results have been provided to verify and validate the obtained conclusions.

Although the proposed model and analysis method comes from the SRF-PLL, they are also suitable for analyzing other types of PLLs.

II. CONVENTIONAL SRF-PLL AND ITS SMALL–SIGNAL LINEARIZED MODEL

Fig. 1 shows the general structure of the conventional SRF-PLL. It can be seen that this structure needs a coordinate transformation form $a,b,c \rightarrow dq$, and the lock is realized by setting the reference U_q* to zero. A regulator, usually a *PI*, is used to control this variable, and the output of this regulator is the grid frequency. After the integration of the grid frequency, the utility voltage angle is obtained, which is fed back into the $\alpha\beta \rightarrow dq$ transformation module to transform it into the synchronous rotating reference frame [8]. If the utility voltage is unbalanced, such as the presence of an asymmetrical fault or distortion, it contains a positive-sequence and negative-sequence as well as high order harmonics. It is well known that the fundamental component of the positive-sequence is uniquely useful and the other components will affect the performance of the SRF-PLL. Therefore, a noise source U_N is added which represents all of the harmonics except for the fundamental component of the positive-sequence.

If the utility voltage is balanced and non-distortion, the coordinate transformation form can be expressed as:

$$u_{dq} = \begin{bmatrix} u_d \\ u_q \end{bmatrix} = T[dq] \cdot T[\alpha\beta] \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = U^+ \begin{bmatrix} \cos(\omega t - \theta) \\ \sin(\omega t - \theta) \end{bmatrix}$$

$$T[\alpha\beta] = \frac{2}{3} \begin{bmatrix} -1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (1)$$

$$[T_{dq}] = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix}$$

$$\begin{bmatrix} u_a & u_b & u_c \end{bmatrix}^T = U^+ \begin{bmatrix} \cos\omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix}^T$$

In the steady state, the input voltage of the *PI* controller, u_q, is equal to zero, and $\hat{\theta} = \omega t$. Substituting this condition into Eq. (1) yields:

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = U^+ \begin{bmatrix} \cos(\omega t - \hat{\theta}) \\ \sin(\omega t - \hat{\theta}) \end{bmatrix} = U^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} \quad (2)$$

It can be observed from Eq. (2) that the *d* component represents the amplitude of the three phase voltage v_a, v_b, and v_c, and its phase angle can be detected by the output of the PLL, $\hat{\theta}$, if the utility voltage is balanced and non-distortion.

A. Operational Principle of the SRF-PLL and the Proposed Small-Signal Linearized Model

The *q* component u_q in Eq. (2) is used to form a PLL, referred as a simplified model of the SRF-PLL, as shown Fig. 2. It consists of phase detector (*PD*), a *PI* controller and *VCO*. The operational principle of the PLL is as follows: according to the phase difference θ_e ($=\theta - \hat{\theta}$), the *PD* produces the voltage u_q. It is sent to the *PI* controller to suppress its high-frequency component, thus a DC output voltage uf is developed. This voltage adjusts the frequency $\hat{\omega}$ to tend toward the incoming frequency ω, where $\hat{\omega}$ =ko×uf (ko=1).Until $\hat{\omega} = \omega$, $\hat{\theta} = \theta$ and $u_q = 0$, the PLL reaches the steady state and maintains the output frequency and phase angle.

It should be noted that the PD is a nonlinear device due to its sinusoidal function. However, if the phase error, θ_e is very small, less than π/6, the output of the PD can be approximated by:

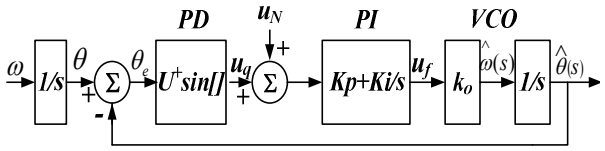


Fig. 2. Simplified model of SRF-PLL.

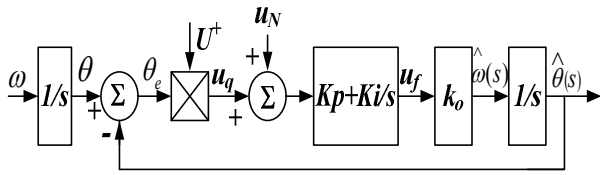


Fig. 3. Small-signal linearized model of SRF-PLL.

$$\sin(\theta-\hat{\theta})\approx\theta-\hat{\theta} \tag{3}$$

where $\left|\theta-\hat{\theta}\right|\le\frac{\pi}{6}$.

Therefore, when the PLL is locked or tends to lock, a small-signal linearized model of the PD can be given by:

$$u_q=U^+\sin\theta_e\approx U^+(\theta-\hat{\theta}) \tag{4}$$

Thus, a small-signal linearized model of the SRF-PLL is proposed, as depicted in Fig. 3.

Based on the proposed small-signal linearized model of the SRF-PLL, some typical transfer functions of the SRF-PLL can be derived as follows.

The open-loop transfer function of the SRF-PLL is

$$T(s)=\frac{\hat{\theta}(s)}{\theta_e(s)}=U^+\frac{(k_ps+k_i)}{s^2} \tag{5}$$

The closed-loop transfer function of the SRF-PLL is

$$H_\theta(s)=\frac{\hat{\theta}(s)}{\theta(s)}=\frac{U^+k_ps+U^+k_i}{s^2+U^+k_ps+U^+k_i} \tag{6}$$

The input-to-error transfer function of the SRF-PLL is

$$E_\theta(s)=\frac{\theta_e(s)}{\theta(s)}=\frac{s^2}{s^2+U^+k_ps+U^+k_i} \tag{7}$$

The noise-to-error transfer function the SRF-PLL is

$$E_u(s)=\frac{\theta_e(s)}{U_N(s)}=\frac{k_ps+k_i}{s^2+U^+k_ps+U^+k_i} \tag{8}$$

B. Stability Consideration

The open-loop transfer function, Eq. (5), can be rewritten as:

$$\frac{\hat{\theta}(s)}{\theta_e(s)}=T(s)=U^+k_i\frac{(s/\omega_z+1)}{s^2} \tag{9}$$

where $\omega_z=\frac{k_i}{k_p}$.

The substitution of $s=j\omega$ into Eq. (9) yields the frequency repose. Fig. 4 illustrates a Bode plot of the magnitude frequency response of *T(s)*.

In Fig. 4, let the crossover frequency f_c be f_z so that the phase margin is about 45 degrees. Using the identity $f_c=f_z$ yields:

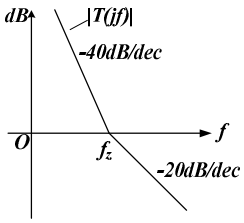


Fig. 4. Magnitude frequency response of *T(s)*.

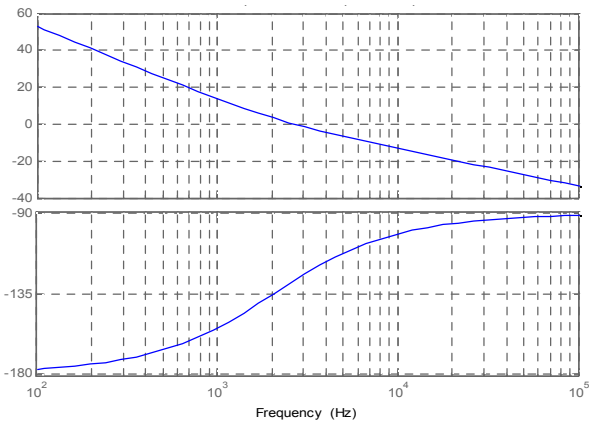


Fig. 5. The simulation results of the frequency response T(s), the parameters are: U+=466.62, fc=2.7kHz, kp=28.277 and ki=3.73*103.

$$\begin{aligned}k_i&=\frac{4\pi^2f_c^2}{U^+}\\ k_p&=\frac{k_i}{\omega_z}\end{aligned} \tag{10}$$

The substitution of U^+=466.62 and f_c=2.7kHz yields k_p=28.277 and k_i=3.73*10^3. The simulation results are demonstrated in Fig. 5. It can be seen that the crossover frequency is about 2.71kHz and that the phase margin is about 53 degree to ensure stability and a fast dynamic response.

III. PERFORMANCE ANALYSIS OF THE SRF-PLL

The performance of the SRF-PLL is estimated in this section, including the capture time, the capture range, and the steady-state error.

A. Capture Time of SRF-PLL

The normalized transfer function of (6) can be rewritten as:

$$H_\theta=\frac{2\varsigma\omega_ns+\omega_n^2}{s^2+2\varsigma\omega_ns+\omega_n^2} \tag{11}$$

where $\omega_n^2=U^+k_i$, $\varsigma=\frac{1}{2}\sqrt{U^+k_p/\omega_z}$, $\omega_z=\frac{k_i}{k_p}$.

By ignoring the LHP (left half plane) zero in Eq. (11), it can be approximated by a standard second order transfer function $\frac{\omega_n^2}{s^2+2\varsigma\omega_ns+\omega_n^2}$.

The dynamic analysis of a standard second-order system

has been studied in many textbooks. The following approximated formulas are present in reference [9]. The settling time t_s can be calculated by the formula in [10],

$$t_s = 4.6\tau \tag{12}$$

where $\tau = 1/\varsigma\omega_n$.

It is noted that the settling time is usually called the capture time in a PLL.

According to the parameters k_i=3.73×10^3 and k_p=28.277 in Section II, the damping factor, natural frequency and capture time can be calculated, yielding ω_n=1.139×10^{4}rad/s, ς=0.5 and t_s=0.8ms, respectively.

The bandwidth of the PLL is:

$$\omega_{-3dB} = \omega_n\sqrt{1\text{-}2\varsigma^2 + \sqrt{(1\text{-}2\varsigma^2)^2 + 1}} \tag{13}$$

For $\varsigma = 0.7$, the ω_{-3dB} is:

$$\omega_{-3dB} = 2.06\omega_n \tag{14}$$

According to Eq. (12), Eq. (13) and Eq. (14), an important formula can be derived that the product of the capture time t_s and the bandwidth ω_{-3dB} is constant, and the value of the product is $\omega_{-3dB}t_s \approx 2.3$ under the condition of ς=0.7 and a 1% steady-state error for the step response. In other words, the capture time t_s is inversely proportional to the bandwidth ω_{-3dB}.

Experimental results are shown in Fig. 6. In Fig. 6(a), *CH1*, *CH2* and *CH3* are the three-phase utility voltages, and *CH4* is a control signal. The phase of the utility voltage jumps forward 180 degree while the control signal *CH4* has a step change at a triggering time point. In Fig. 6(b), *CH1* is the estimated output phase $\hat{\theta}$ of the SRF-PLL, and *CH2* is the control signal. The vicinity waveforms of Fig. 6(b) at the triggering time point are enlarged as illustrated in Fig. 6(c) to measure the capture time, t_s≈1ms. The steady-state error θ_e is denoted by *CH1* shown in Fig. 6(d).

Note that the capture time displays a considerable error between the theoretical result t_s=0.8ms from Eq. (12) and the experimental result t_s=1ms. Therefore, the expression result from Eq. (12) should be taken only as a guide rather than precise formula. This formula provides a rough estimate of the time response of the system since the time taken by the coordinate transformation in the SRF-PLL and the influence of the ignored zero $-\frac{\omega_n}{2\xi}$ of Eq. (11) are not yet considered in this formula [11]. This should be checked, usually by simulation, in order to verify whether the time specification has been properly met or not.

B. Capture Range of SRF-PLL

Another significant parameter of the PLL, called the capture range $\Delta\omega_H$, is the frequency range at which a PLL is able to keep statically phase-locked. This parameter can be calculated by:

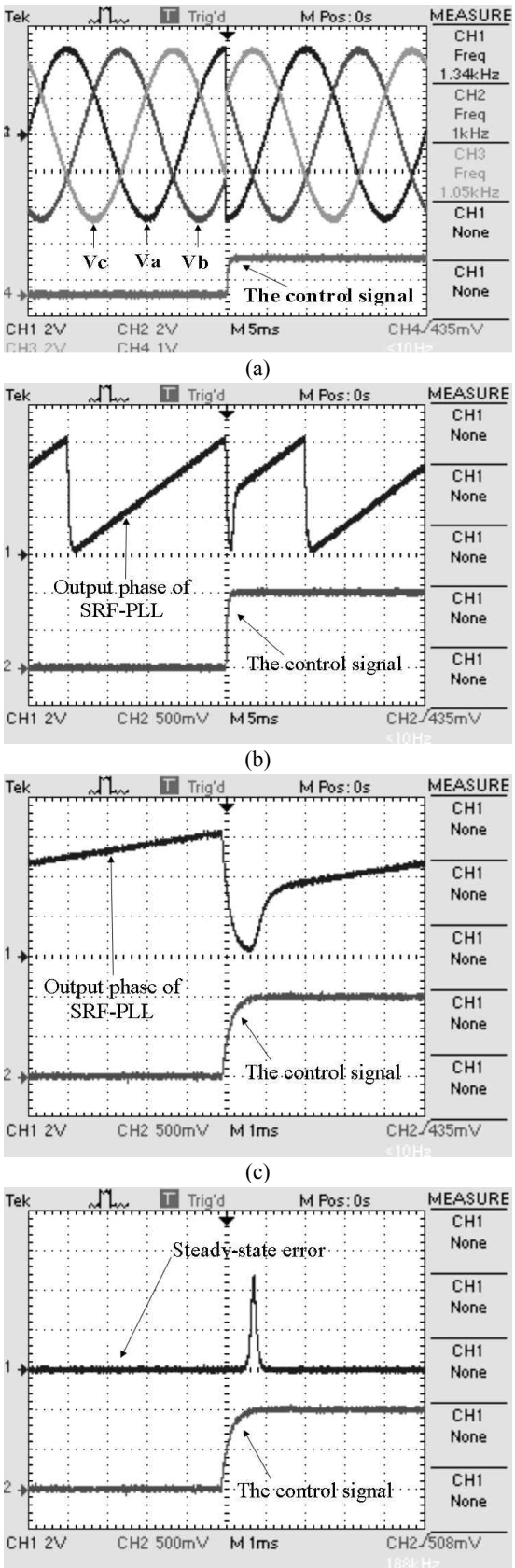


Fig. 6. Experimental waveforms of SRF-PLL when phase jumps. (a) Three-phase utility voltage. (b) Estimated phase of SRF-PLL. (c) Enlarged waveform of (b), (d) steady-state error.

$$\Delta\omega_H = U^+F(0) = \infty \quad \text{for PI controller} \tag{15}$$

where F(0) is the DC gain of the controller in Fig. 3.

If a PI controller is selected, the capture range $\Delta\omega_H$ is infinite because PI controller has an infinite DC gain. Therefore, the capture range $\Delta\omega_H$ is only limited by the maximum value of the integrator output. An infinite capture rang implies that the PLL has no ability to reject any noise since it can lock all of the frequency signals. Therefore, a PI controller is not a good choice to suppress the noise present in a PLL.

C. Steady-state Error of the SRF-PLL

In this section it is investigated how the PLL responds under various conditions: phase step, frequency step, frequency ramp, and magnitude step as well as magnitude ramp.

In practice, when a PLL is used for synchronization with the grid voltage in a grid-connected inverter, and a set of micro-grid inverters working in the island condition by employing the frequency droop control strategy [12]. The phase step, frequency step and ramp of the PCC voltage are always encountered. Moreover, the magnitude step and ramp always occur when the inverter is controlled to ride through the grid fault [13].

1) Case 1, Steady-state error in the case of variations in the phase and frequency of utility voltage: By applying Eq. (7), the steady-state error of the SRF-PLL can be expressed as:

$$\begin{aligned}&\lim_{t\to\infty} e_\theta(t)\\ &= \lim_{s\to 0} s\theta_e(s) = \lim_{s\to 0} sE_\theta(s)\theta(s)\\ &= \lim_{s\to 0} s\frac{s^2}{s^2+2\varsigma\omega_n s+\omega_n^2}\theta(s)\end{aligned} \tag{16}$$

If a phase step is applied to the utility voltage as a reference signal, then θ(s)=1/s and:

$$\lim_{t\to\infty} e_\theta(t) = 0 \tag{17}$$

This conclusion has already been proved in Fig. 6(d).

Similarly, since θ(s)=ω(s)/s, the steady state error formula of the frequency variation applied to a reference input gives:

$$\begin{aligned}&\lim_{t\to\infty} e_\omega(t)\\ &= \lim_{s\to 0} s\theta_e(s)/s = \lim_{s\to 0} E_\theta(s)\omega(s)\\ &= \lim_{s\to 0}\frac{s^2}{s^2+2\varsigma\omega_n s+\omega_n^2}\omega(s)\end{aligned} \tag{18}$$

If a frequency step of the utility voltage is used as an input, then *ω(s)=1/s* and:

$$\lim_{t\to\infty} e_\omega(t) = 0 \tag{19}$$

If a frequency ramp of the utility voltage acts on the input, then ω(s)=1/s^2 and:

$$\lim_{t\to\infty} e_\omega(t) = 1/\omega_n^2 \tag{20}$$

The open-loop transfer function of (5) shows that this PLL is a type II system, with two poles at the origin. This means that it is able to track the utility voltage phase step, frequency step and phase ramp (change slowly in a constant slop) without any steady-state errors.

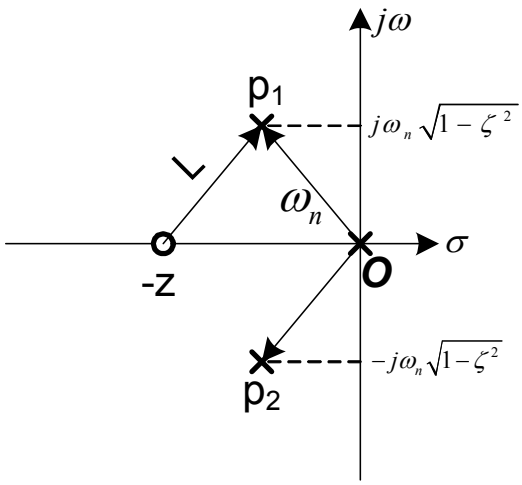


Fig. 7. Diagrams of the poles and zeros location of the closed-loop transfer function H_ω.

Moreover, the normalized closed-loop transfer function from ω to $\hat{\theta}$, shown in Fig. 3, can be written as:

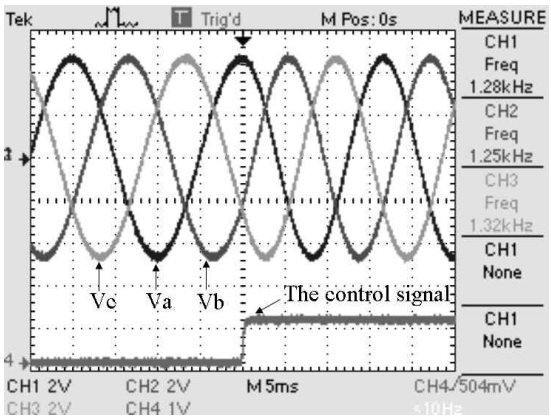
$$H_\omega = \frac{\omega_n^2(s+z)}{zs(s^2+2\varsigma\omega_n s+\omega_n^2)} \tag{21}$$

Compared with the expression of H_θ, as shown in Eq. (11), a pole at the origin is added in H_ω. A diagram of the poles and zeros location of the closed-loop transfer function H_ω is illustrated in Fig. 7.

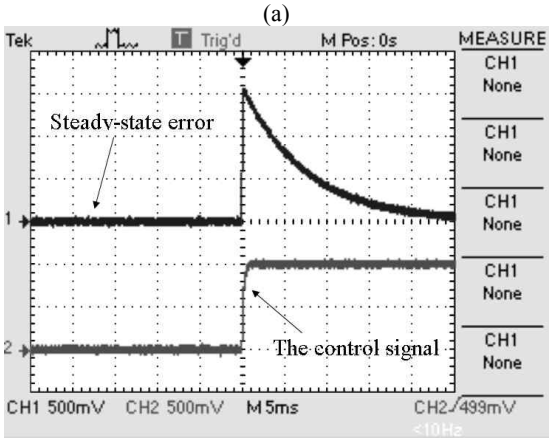
As show in Fig. 7, the dominant pole is at the origin, rather than the pair of complex poles, p_1 and p_2. Thus, the system presents first-order system features so that its dynamic performance is not as good as the pervious closed system defined by Eq. (12). Experimental results are shown in Fig. 8. In Fig. 8(a), *CH1*, *CH2* and *CH3* are three-phase utility voltages, and *CH4* is a control signal. A frequency jump of the utility voltage occurs from 50Hz to 60Hz, while the control signal of *CH4* has a step change at a triggering time point. In Fig. 8(b), *CH1* shows a steady-state error for the SRF-PLL. It can be observed that its steady-state error is zero, but the capture time t_s is about 25ms.

In addition, a constant steady state error should exist in a conventional SRF-PLL when it is used in a set of micro-grid inverters working in the isolation island condition by adopting the frequency droop control strategy.

2) Case 2, steady-state error analysis of the magnitude variation of the utility voltage applied to an input signal: When the magnitude of the utility voltage fluctuates, and the phase is kept constant, the equivalent model is shown in Fig. 9. There are two parts in this model. One is the linear



(a)



(b)

Fig. 8. Experimental waveforms of SRF-PLL when frequency jumps. (a) Utility voltage. (b) Waveform of steady-state error.

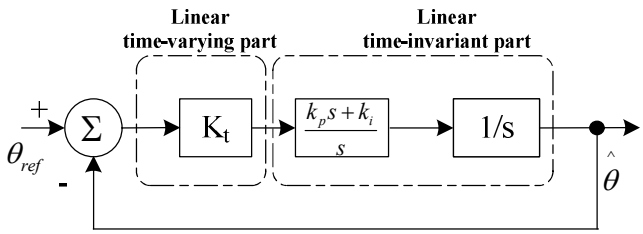


Fig. 9. The equivalent model when the magnitude of the utility voltage fluctuates, and phase is kept constant.

time-varying part, and the other is the linear time-invariant part. The system performance of the magnitude variation is analyzed in the Bode diagram shown in Fig. 10. The nonlinear system is analyzed by using the method of describing function.

When the magnitude of the utility voltage is normal, k_t is equal to k_{t1}. When the magnitude of the utility voltage drops at time=t_2, the gain k_t is equal to k_{t2}, and the amplitude frequency response curve moves downward. However, the phase frequency response curve remains unchanged.

In summary, as shown in Fig. 10, when the magnitude of the utility voltage drops, the gain-crossover frequency and phase margin decrease, but the system remains stable for the PI controller. Variations in the magnitude have no effect on the steady-state error.

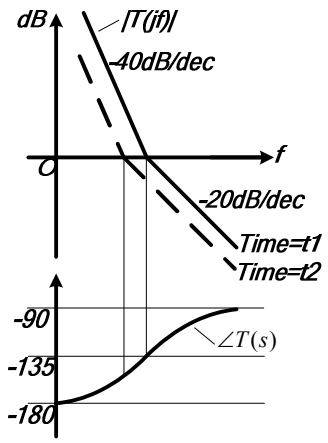


Fig. 10. The Bode diagram when the amplitude of the utility voltage fluctuates.

Experimental results are shown in Fig. 11 and Fig. 12. In Fig. 11(a), *Ch1*, *Ch2* and *CH3*, are three-phase utility voltages, and CH4 is a control signal. The amplitude of the utility voltage drops from 466V to 233V while the control signal steps. As shown in Fig. 11(b), *CH1* displays the steady-state error for the SRF-PLL, and *CH2* is a control signal. It can be seen that the magnitude step has no effect on the steady-state error.

As shown in Fig. 12(a), the amplitude ramp of the utility voltage is applied, and Fig. 12(b) shows that the amplitude ramp has no effect on the steady-state error.

It can be seen from the above analysis that if the amplitude of the utility voltage fluctuates, the conventional SRF-PLL has no steady-state error. It only decreases the crossover frequency and phase margin of the system.

The performance of the conventional SRF-PLL has been summarized and listed in Table I.

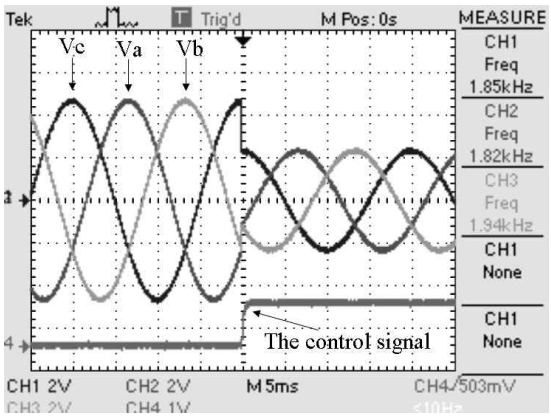
IV. PERFORMANCE IN THE PRESENCE OF NOISE

Noise is an extremely important issue when a PLL is employed to detect the fundamental component of the positive-sequence voltage in the control systems of grid-connected inverters or micro-grid inverters.

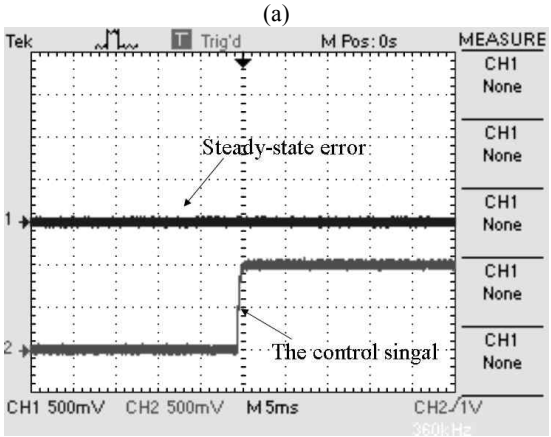
A. Noise Model of SRF-PLL

If the utility is unbalanced and its output voltage contains some high order harmonics, such as the 3rd, 5th, 7th…, then the voltage vector expression in the *dq* plane in Eq.(1) may be modified as follows:

$$u_{dq}^{N}=\begin{bmatrix}u_d^N\\u_q^N\end{bmatrix}=U^{+}\begin{bmatrix}\cos[\omega_0 t-\hat{\theta}]\\\sin[\omega_0 t-\hat{\theta}]\end{bmatrix}+\sum_{n=2}^{\infty}U_{2n-1}^{+}\begin{bmatrix}\cos[(2n-1)\omega_0 t-\hat{\theta}]\\\sin[(2n-1)\omega_0 t-\hat{\theta}]\end{bmatrix}+\sum_{n=1}^{\infty}U_{2n-1}^{-}\begin{bmatrix}\cos(-(2n-1)\omega_0 t-\hat{\theta})\\\sin(-(2n-1)\omega_0 t-\hat{\theta})\end{bmatrix} \quad (22)$$

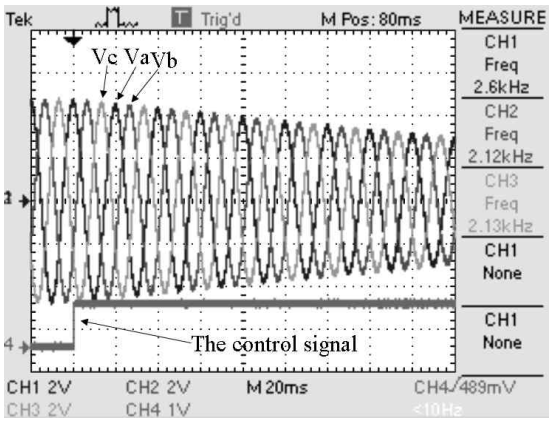


(a)

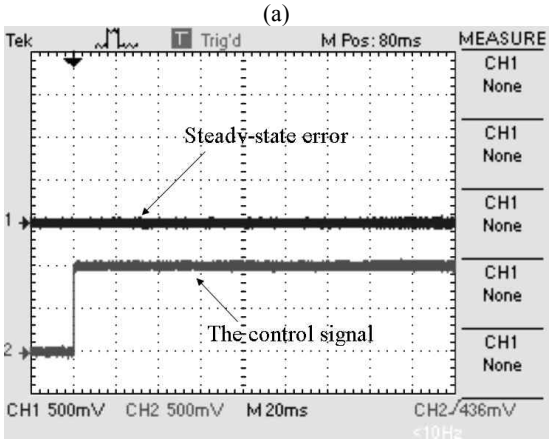


(b)

Fig. 11. Experimental waveforms of SRF-PLL when a amplitude step of the utility voltage is applied. (a) Utility voltage. (b) Waveform of steady-state error.



(a)



(b)

Fig. 12. Experimental waveforms of SRF-PLL a amplitude ramp of utility voltage is applied. (a) Utility voltage. (b) Waveform of steady-state error.

The formula of (22) can be rewritten in the following compact form:

$$u_q^N = U_q + U_N \tag{23}$$

where

$$U_q = U^+ \sin[\omega_0 t - \hat{\theta}]$$

$$U_N = \sum_{n=2}^{\infty} U_{2n-1}^+ \sin[(2n-1)\omega_0 t - \hat{\theta}] + \sum_{n=1}^{\infty} U_{2n-1}^- \sin(-(2n-1)\omega_0 t - \hat{\theta})$$

Assuming that the positive-sequence component is locked in the steady state, and then the formula of (22) becomes:

$$\begin{aligned} u_{dq}^N &= \begin{bmatrix} u_d^N \\ u_q^N \end{bmatrix} = U^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} \\ &+ \sum_{n=2}^{\infty} U_{2n-1}^+ \begin{bmatrix} \cos 2(n-1)\omega_0 t \\ \sin 2(n-1)\omega_0 t \end{bmatrix} \\ &+ \sum_{n=1}^{\infty} U_{2n-1}^- \begin{bmatrix} \cos 2n\omega_0 t \\ -\sin 2n\omega_0 t \end{bmatrix} \end{aligned} \tag{24}$$

The first term of Eq. (24) is the fundamental component of the positive-voltage, the summation term is the high order harmonic components and the third is the negative-voltage component.

The q component of Eq. (24) can be expressed as:

$$u_q^N(t) \approx \sum_{n=2}^{\infty} U_{2n-1}^+ \sin 2(n-1)\omega_0 t - \sum_{n=1}^{\infty} U_{2n-1}^- \sin 2n\omega_0 t = U_N \tag{25}$$

Hence, the noise source is represented by U_N, as illustrated in Fig. 1.

The small-signal linearized model of the SRF-PLL, shown in Fig. 3, can be modified to achieve the noise model of the SRF-PLL, shown in Fig. 13. Here, k_o is the sensitivity of the voltage-controlled frequency oscillator (VCO), and it is equal to 1.

B. Noise Performance

By applying the Mason formula to the block diagram of the noise model shown in Fig. 13, the input-to-output transfer function $H_N(s)$ is given by:

$$H_N(s) = \frac{U_{eN}(s)}{U_N(s)} = \frac{1}{U^+ k_o} \times \frac{s(s/Q+1)}{(s/\omega_n)^2 + s/\omega_n Q + 1} \tag{26}$$

where $\omega_n^2 = U^+ k_i$, $\varsigma = \sqrt{U^+ k_p / 4k_i}$, $Q = 1/2\varsigma$.

If a PI controller is used, and the parameters are: U^+=466.62, k_p=28.277 and k_i=3.73*10^3, frequency response of $H_N(s)$ is depicted in Fig. 14.

The following conclusions can be drawn form Fig. 14. The frequency response of $H_N(s)$ exhibits a high-pass characteristic

TABLE I
THE PERFORMANCE OF CONVENTIONAL SRF-PLL

title	Formula
normalized second-order closed-loop transfer function	$H_\theta = \dfrac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$
natural frequency and damping factor	$\omega_n^2 = U^+ k_i$, $\varsigma = \sqrt{U^+ k_p / \omega_z}\,/2$
capture time	$t_s = 4.6/\varsigma\omega_n$
-3dB bandwidth	$\omega_{-3dB} = \omega_n\sqrt{1+2\varsigma^2+\sqrt{(1+2\varsigma)^2+1}}$ $\omega_{-3dB} = 2.06\omega_n$,for $\varsigma = 0.7$
product of capture time and bandwidth	$\omega_{-3dB} t_s \approx 2.3$, for $\varsigma = 0.7$
capture range	$\Delta\omega_H = \infty$ for PI Controller
steady-state error	
phase step	$\lim_{t\to\infty} e_\theta(t) = 0$
frequency step	$\lim_{t\to\infty} e_\omega(t) = 0$
frequency ramp	$\lim_{t\to\infty} e_\omega(t) = 1/\omega_n^2$
amplitude step	$\lim_{t\to\infty} e_u(t) = 0$
amplitude ramp	$\lim_{t\to\infty} e_u(t) = 0$

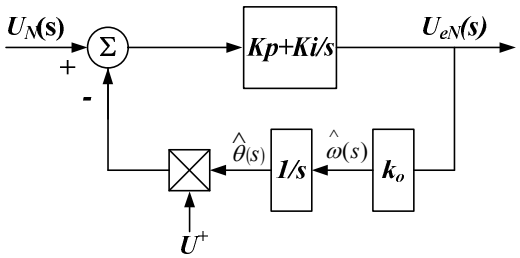


Fig. 13. Noise model of SRF-PLL.

with a cutoff frequency $f_c = \sqrt{U^+ \dfrac{k_i}{k_p}}$. The cutoff frequency f_c is smaller than the grid frequency f_o. In other words, according to Eq. (25), the all components of U_N can pass through the controller directly without any attenuation and reach to the input terminal of the VCO. Therefore, the SRF-PLL does not have the ability to reject noise.

Usually, a low-pass filter is included in the loop to alleviate noise as shown in Fig. 15. Since $1/T_L << 2\omega_0$ is satisfied, and the noise cannot reach the terminal of the VCO, the SRF-PLL has the ability to reject noise.

The open-loop transfer function *T(s)* is modified as:

$$T(s) = U^+ k_i \frac{(s/\omega_z + 1)}{s^2(s/\omega_p + 1)}, \omega_z = \frac{k_i}{k_p}, \omega_p = \frac{1}{T_L} \qquad (27)$$

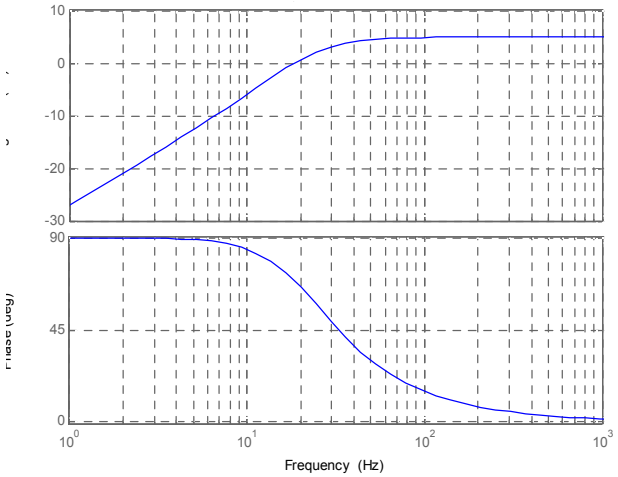


Fig. 14. Frequency response of the noise transfer function $H_N(s)$, the parameters are: U^+=466.62, f_c=2.7kHz, k_p=28.277 and k_i=3.73*10^3.

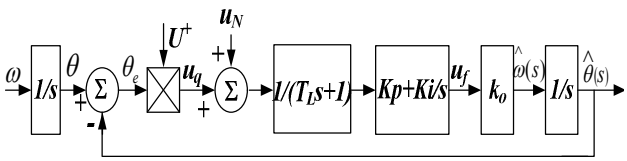


Fig. 15. Small-signal linearized model of SRF-PLL with low-pass filter.

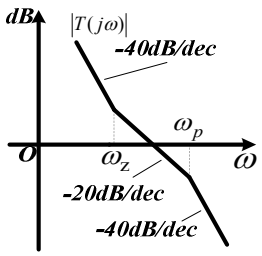


Fig. 16. The bode diagram of the open-loop transfer function T(s) of SRF-PLL with low pass filter.

The zero of the PI controller ω_z should be selected to be lower than ω_p , and the amplitude frequency response of *T(s)* can be plotted, as shown in Fig. 16. The phase margin is determined by the middle-frequency-band of ($\omega_p - \omega_z$). Usually, let $\omega_p/\omega_z \approx 5-10$ so that the phase margin is about 30-60 degrees, and the crossover frequency is equal to $\omega_p/3$.

A low-pass filter is added into the loop to alleviate noise. However, the above analysis indicated that the crossover frequency is rather low, and the fast dynamic response is not satisfied.

Fig. 17 shows a simulation result using MATLAB with the following parameters: ω_p =314rad/s, ω_z = 40rad/s, and $\omega_p/\omega_z = 7.8$. The simulation result demonstrates that the

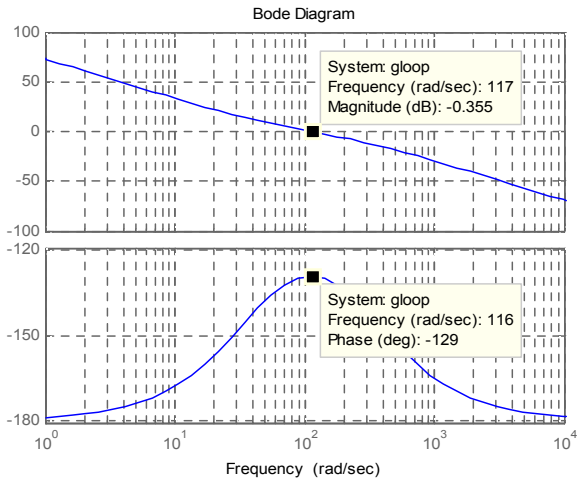


Fig. 17. Frequency response of the open-loop transfer function T(s) of SRF-PLL with low pass filter.

crossover frequency is only 18Hz, and phase margin is about 50 degrees.

The experimental results are shown in Fig. 18. In Fig. 18(a), *CH1, CH2* and *CH3*, are three-phase utility voltage, and *CH4* is a control signal. A phase step of 180 degrees is applied, and a 3th harmonic component with a value of five percent is injected into the grid. As shown in Fig. 18(b), *CH1* and *CH2* represent the input and output signals of the low-pass filter. This shows that the harmonic component is eliminated with the low-pass filter, but the capture time t_s is about 50ms. In sum, the ability to suppress noise and the dynamic response are mutually contradictory for the SRF-PLL.

C. SNR (signal-to-noise ratio) of the SRF-PLL

Based on the noise model of the SRF-PLL shown in Fig. 13 and Eq. (26), the input noise voltage of the VCO is given by:

$$U_{eN}(s) = H_N(s)U_N(s) = \frac{1}{U^+ k_o} \times \frac{s(s/Q+1)}{(s/\omega_n)^2 + s/\omega_n Q + 1} U_N(s) \quad (28)$$

Eq. (25) shows that the noise contains two parts: unbalance noise and high harmonic noise. For grid-connected inverters, unbalance noise is dominant. However, the high order harmonic noises should be considered for micro-grid inverters.

1) Case 1, SNR for unbalance noise: For grid-connected inverters, unbalanced noise is dominant. Therefore, Eq. (28) is employed to compute the unbalance noise response, such as:

$$U_{eN}(jf)\big|_{f=2f_0} = \frac{1}{U^+ k_o} \times \frac{j2f_o(j2f_o/Q+1)}{1-(2f_o/f_n)^2 + j2f_o/f_n Q} \times U_N(j2f_o) \quad (29)$$

It can be seen from Fig. 14 that the amplitude is 4.88dB, and the phase is 14 degree at f=100Hz. If the noise voltage is $U_N(t) = U_N \sin(2\omega t)$, the input voltage of the VCO is:

$$U_{eN}(t) = 1.75U_N \sin(2\omega t + 14^\circ) = U_{NB} \sin(2\omega t + 14^\circ) \quad (30)$$

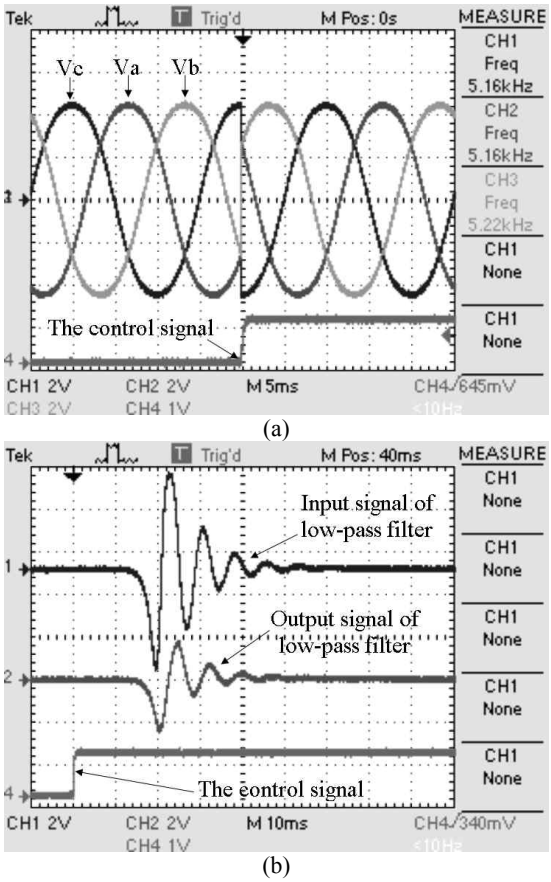


Fig. 18. Experimental waveform of SRF-PLL with low pass filter when phase step of the three-phase voltage is applied. (a) Utility voltage. (b) Waveform of steady-state error.

The output of the VCO is a constant with value of 50Hz under ideal conditions. If the utility voltage is unbalanced, the output frequency of the VCO is given by:

$$\hat{\omega}(t) = 100\pi + U_{NB} \sin(2\omega t + 14^o) \quad (31)$$

Eq. (31) indicates that the output frequency of the PLL becomes a frequency modulation signal instead of a constant frequency, as shown in Fig. 19.

The signal-noise-ratio is defined as:

$$SNR_{UB} = \frac{\text{grid frequency}}{\text{noise magnitude}} = 20\lg\frac{\omega_o}{U_{NB}} = 20\lg\frac{100\pi}{|H_N(j200\pi)|U_N} \quad (32)$$

For example, when the parameters are: $U_N = 0.3U^+$, the SNR is only $SNR_{UB} = 2.14dB$.

It is obvious that the SNR of the SRF-PLL is so low that the output frequency of the SRF-PLL is seriously distorted.

2) Case 2, SNR for high harmonic noise: The grid voltage may be distorted in the case of micro-grids working in the island condition or in weak grids with a high grid impedance because their gridvvoltage is prone to notable distorted by

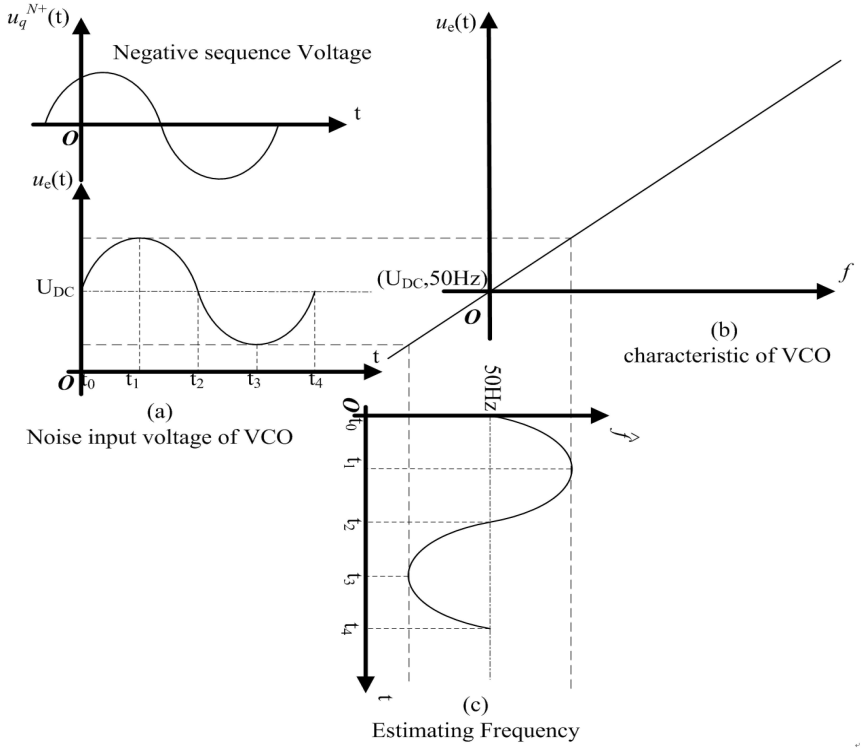


Fig. 19. Estimating frequency waveforms of the PLL by affecting the unbalance noise.

harmonics, switching notches and noise. Therefore, the high-order harmonic noise needs to be considered in this case.

If the noise voltage is defined as:

$$U_N(t)=\sum_{i=2}^{\infty}U_{2n-2}^{+}\sin 2(n-1)\omega t$$

The voltage of the input terminal of the VCO is:

$$U_{eN}(t)=1.75\sum_{i=2}^{\infty}U_{2n-2}^{+}\sin 2(n-1)\omega t \tag{33}$$

The output frequency of the VCO is given by:

$$\hat{\omega}(t)\approx 100\pi+1.75\sum_{i=2}^{\infty}U_{2n-2}^{+}\sin 2(n-1)\omega t \tag{34}$$

The signal-noise-ratio is defined as:

$$SNR_{UB}=\frac{\text{grid frequency}}{\text{noise magnitude}}=20\lg\frac{100\pi}{1.75\sqrt{\sum_{i=2}^{\infty}(U_{2n-2}^{+})^2}} \tag{35}$$

Therefore, the output frequency of the PLL is 100π plus the even harmonic components if the utility voltage is distorted.

V. CONCLUSIONS

It is difficult to investigate the electric characteristics of PLLs because they are nonlinear systems. This results from the coordinate transformation in the control block. In this paper, a canonical small–signal linearized model of the SRF-PLL has been developed to study the following issues: (1) the phase-locked process and operational principle; (2) the determination of the controller parameters; (3) the performance under various conditions.

By adopting the canonical small–signal linearized model, the following conclusions are obtained:

(1) The SRF-PLL with a PI controller is a normalized second-order system, and several formulas have been supplied in this paper to calculate its significant specifications such as the capture time, the capture rang, the bandwidth, the product of capture time and bandwidth as well as the parameters of the PI controller.

(2) It is revealed by analysis and experiment results that the steady-state error of the SRF-PLL is zero under the conditions of phase step, frequency step, amplitude step and ramp. However, the SRF-PLL has a constant error in case of a frequency ramp.

Noise analysis is also an extremely important issue for the PLL used in the control of grid-connected power inverters or macro grid inverters. In the performance analysis in the presence of noise, the following results and conclusions can be achieved:

(1) A noise model of the SRF-PLL has been proposed to investigate the performance of the SRF-PLL in the presence of noise.

(2) The SRF-PLL is incapable of rejecting noise. However, a low-pass filter in the loop can attenuate the noise at the cost of increasing the capture time.

(3)Two categories of the SNR have also been calculated.

In summary, this paper presents a detailed derivation of small-signal analysis methods to study the SRF-PLL.

Valuable conclusion can be achieved with this method. These conclusions are verified and validated by simulation and experimental results.

Moreover, the conventional SRF-PLL can be commonly used as an essential block in some advanced PLLs, such as DDSRF-PLL [14], IPT-PLL [15], PQ-PLL [15], DSC-PLL [16], [17], DSOAF-PLL [18], FRF-PLL [19] and SSI-PLL [20]. They have a small-signal linearized model that is identical to that of the conventional SRF-PLL. As a result, the proposed model and analysis method are suitable for the other typical PLLs.

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REFERENCES

[1] M. Cichowlas, M. Malinowski, D. L. Sobczuk, M. P. Kazmierkowski, P. Rodriguez, and J. Pou, "Active filtering function of three-phase PWM boost rectifier under different line voltage conditions," *IEEE Trans. Ind. Electron*, Vol. 52, No. 2, pp. 410-419, Apr.2005.

[2] R. Teodorescu and F. Blaabjerg, "Flexible control of small wind turbines with grid failure detection operating in stand-alone and grid-connected mode," *IEEE Trans. Power Electron*, Vol. 19, no. 5, pp. 1323-1332, Sep. 2004.

[3] R. Teodorescu, M. Liserre, P. Rodríguez, *Grid Converters for Photovoltaic and Wind Power Systems*, Wiley-IEEE Press, Chap. 4 and 8, 2011.

[4] R. W. Wall, "Simple methods for detecting zero crossing," in *Industrial Electronics Society, IECON'03. The 29th Annual Conference of the IEEE*, Vol. 3, pp. 2477-2481, 2003.

[5] M. M. Begovic, P. M. Djuric, S. Dunlap, and A. G. Phadke, "Frequency tracking in power networks in the presence ofharmonics," *IEEE Trans. Power Del.*, Vol. 8, No. 2, pp. 480-486, Apr. 1993.

[6] B. P. McGrath, D. G. Holmes, and J. Galloway, "Improved power converter line synchronisation using an adaptive discrete fourier transform (DFT)," in *Power Electronics Specialists Conference, PESC 2002 IEEE 33rd Annual*, Vol. 2, pp. 821-826, 2002.

[7] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl*, Vol. 33, No.1. pp. 58-63, Jan/Feb, 1997.

[8] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.,* Vol. 53, No. 5, pp. 1398-1409, Oct. 2006.

[9] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamics Systems*, 4th ed., Prentice Hall, Chap. 3, and 6, 2002.

[10] R. E. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, 5th ed., McGraw-Hill Professional, Chap. 2, 2003.

[11] H. Geng, D. Xu, and B. Wu, "A novel hardware-based all-digital phase-locked loop applied to grid-connected power converters," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 5, pp. 1737-1745, May 2011.

[12] Y. W. Li and C.-N. Kao, "An accurate power control strategy for power electronics interfaced distributed generation units operating in a low-voltage multibus microgrid," *IEEE Trans. Ind. Electron.,* Vol. 24, No. 12, pp. 2977-2988, Dec. 2009.

[13] H. Geng, C. Liu, and G. Yang, "LVRT capability of DFIG-based WECS under asymmetrical grid fault condition," *IEEE Trans. Ind. Electron.*, pp. 2495-2509, Jun. 2013.

[14] P. Rodriguez, et al., "Decoupled double synchronous reference frame PLL for power converters control power electronics," *IEEE Trans. Power Electron.*, Vol. 22, No. 2, pp. 584-592, Mar. 2007.

[15] S. M. Silva, B. M. Lopes, B. J. C. Filho, R. P. Campana, and W. C. Bosventura, "Performance evaluation of PLL algorithms for single-phase grid-connected systems," *Industry Applications Conference, 39th IAS Annual Meeting Conference Record of the 2004 IEEE*, pp.2259-2263, 2004.

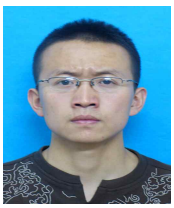
[16] H. Awad, J. Svensson, and M. J. Bollen, "Tuning software phase-locked loop for series-connected converters," *IEEE Trans. Power Del.*, Vol. 20, No. 1, pp. 300-308, Jan. 2005.

[17] Y. F. Wang and Y. W. Li, "Grid synchronization PLL based on cascaded delayed signal cancellation," *IEEE Trans. Power Electron.*, Vol. 26, No. 7, pp.1987-1997, Jul. 2011.

[18] Y. F. Wang and Y. W. Li, "Analysis and digital implementation of cascaded delayed-signal-cancellation PLL," *IEEE Trans. Power Electron.,* Vol. 26, No. 4, pp.1067-1080, Apr. 2011.

[19] G. Escobar, M. F. Martinez-Montejano, A. A. Valdez, P. R. Martinez, and M. Hernandez-Gomez, "Fixed-reference-frame phase-locked loop for grid synchronization under unbalanced operation," *IEEE Trans. Ind. Electron.,* Vol. 58, No. 5, pp. 1943-1951, May 2011.

[20] R. I. Bojoi, G. Griva, V. Bostan, M. Guerriero, F. Farina, and F. Profumo, "Current control strategy for power conditioners using sinusoidal signal integrators in synchronous reference frame," *IEEE Trans. Power Electron.,* Vol. 20, No. 6, pp. 1402- 1412, Nov. 2005.



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