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A Simple Capacitor Voltage Balancing Method with a Fundamental Sorting Frequency for Modular Multilevel Converters

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Abstract

A Fundamental Frequency Sorting Algorithm (FFSA) is proposed in this paper to balance the voltages of floating dc capacitors for Modular Multilevel Converters (MMCs). The main idea is to change the sequences of the CPS-PWM carriers according to the capacitor voltage increments during the previous fundamental period. Excessive frequent sorting is avoided and many calculating resources are saved for the controller. As a result, more sub-modules can be dealt with. Furthermore, it does not need to measure the arm currents. Therefore, the communication between the controllers can be simplified and the number of current sensors can be reduced. Moreover, the proposed balancing method guarantees that all of the switching frequencies of the sub-modules are equal to each other. This is quite beneficial for the thermal design of the sub-modules and the lifetime of the power switches. Simulation and experimental results acquired from a 9-level prototype verify the viability of the proposed balancing method.

Key words: Carrier Phase Shift PWM (CPS-PWM), Dual Sorting Mechanism, Fundamental Frequency Sorting Algorithm (FFSA), Modular Multilevel Converter (MMC)

I. INTRODUCTION

The Modular Multilevel Converter (MMC) has attracted a great deal of attention due to its outstanding performance in High Voltage Direct Current (HVDC) transmission and Flexible AC Transmission Systems (FACTS) during the last decade, especially after the Trans Bay Cable Project was successfully accomplished by Siemens [1]. When compared with diode or flying capacitor clamped multilevel converters, the MMC has many merits such as modular construction, redundancy, low switching frequency, low losses and low harmonics [1]-[3]. From recent publications, MMC-related studies are mainly focused on modulation strategies [3]-[8], modeling [9], [10], theoretical calculations [11], [12] and capacitor voltage balancing methods [4], [5], [13]-[17]. The capacitor voltage balancing method is critical for MMCs, as it is related to the safe operation of the whole system and has a significant impact on the output waveform.

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Additional hardware circuits are used to balance the capacitors in [13]. The capacitors are clamped one by one by the diodes so that the capacitor voltage of the top sub-module and the bottom sub-module must be the highest or the lowest. Thus, all of the capacitor voltages are equal when the capacitors of the top and bottom sub-modules are balanced by an additional isolated circuit. This method simplifies the controllers and is easy to realize. However, it needs an extra circuit, especially since the isolated transformer between the top and bottom sub-modules undertakes a high insulation voltage which is equal to the voltage of the DC main bus.

An open-loop balancing method with a special modulation strategy that is executed at the fundamental switching frequency without measuring the capacitor voltage is presented in [14]. It rotates the switching angles of the sub-modules at the fundamental frequency to keep the capacitor voltage stable over a large number of fundamental periods. This method saves a lot of voltage sensors. However, it cannot balance the capacitors well when the load or the DC bus voltage changes.

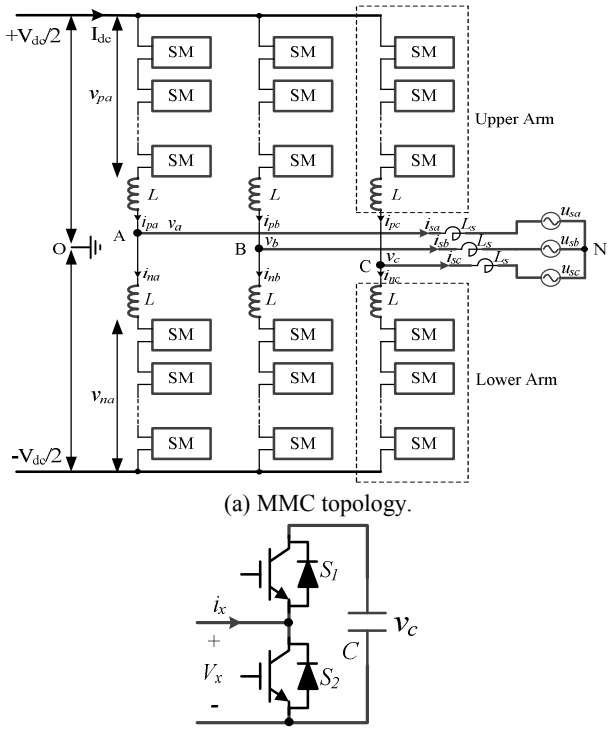
A closed-loop control method which adds an extra signal to the modulation signal is presented in [7], [15]. With this method, the modulation and the individual voltage closed-loop

control tasks are assigned to sub-module controllers, while the output voltage control, the power control and the averaging voltage control of the capacitors are done by the central controller. This distributed control structure is consistent with modular architecture. The parameters of the closed-loop controllers have to keep the system stable. Nevertheless, the difficulty of the control and the risk of instability increase with an increase of the sub-modules.

The sorting algorithm is a commonly used balancing method which can adapt to all of the modulations. Its core idea is to calculate how many sub-modules should be inserted into the circuit by the modulation strategy. Then the most suitable sub-modules are selected. This method is both simple and practical. However, there are frequent sorting issues with the capacitor voltage which are a burden to the controller, especially in the case of a large number of sub-modules. Moreover, the sub-modules are inserted and bypassed randomly so that the switching frequencies of the sub-modules are different from each other. This is harmful for the thermal design and the lifetime of the power switches due to uneven power losses and heat distribution. [4], [5], [16] reduce the calculation scale of each sorting to save calculation resources. The sorting frequency is reduced by controlling the high frequency circulating current to balance the capacitor voltages with CPS-PWM [17]. [18] adopts a counting unit to calculate the total number of switching commutations and it uses this information to keep the switching commutations evenly distributed. However, frequent sorting and uneven switching commutations cannot be solved at the same time with these methods.

In high power application, the switching frequencies of the power switches should be limited due to thermal limitations. In this paper, a CPS-PWM with fundamental carrier frequency is adopted for the Modular Multilevel Converter in order to obtain the fundamental switching frequency. At the same time, a Fundamental Frequency Sorting Algorithm (FFSA) with a dual sorting mechanism is proposed. It uses capacitor voltage increments during the previous fundamental period to judge which carrier of the CPS-PWM charges the most and the least. The first step is to sort the voltage increments of the capacitors in descending order and the present capacitor voltages in ascending order. Then, let the carrier which corresponds to the largest voltage increment drive the sub-module whose capacitor voltage is the lowest. After that, operate with the other carriers in turn. The arm current does not need to be measured. With this method, the sorting frequency and all of the switching frequencies of the power switches are equal to the fundamental frequency.

This paper is organized as follows. The structure and operation principle of the MMC are presented in Section II. A detailed analysis and operation process of the FFSA are introduced in Section III. Simulation results obtained from a 9-level inverter model are illustrated in Section IV to show the correctness of the FFSA. In Section V, experimental results are carried out to verify the proposed balancing method. The last section summarizes the conclusions.



(a) MMC topology.

(b) Configuration of sub-module.

Fig. 1. Structure of MMC.

II. Structure and Operation Principles of the MMC

A. Structure of the MMC

The typical structure of a three-phase MMC is shown in Fig. 1(a) and the configuration of a sub-module is presented in Fig. 1(b). Each phase consists of one upper arm and one lower arm, which are connected in series between two DC terminals. Each arm includes N identical sub-modules and one buffer inductor L. The sub-module is a simple bi-directional chopper cell composed of two IGBTs, S_1 and S_2, and one DC capacitor, C. When S_1 is on and S_2 is off, the SM is in the inserted state and the capacitor can be charged or discharged depending on the current direction. When S_1 is off and S_2 is on, the SM is in the bypassed state. During these two controlled states, the terminal voltage of the SM can be either zero or the capacitor voltage.

B. Steady-State Analysis

For one phase of the MMC, define half of the summation of the upper arm current and lower arm current as the circulating current i_{cirj} (j=a,b,c):

$$\begin{cases} i_{cirj} = (i_{pj} + i_{nj})/2 \\ i_{pj} = i_{cirj} + i_{sj}/2 \\ i_{nj} = i_{cirj} - i_{sj}/2 \end{cases} \quad (1)$$

where i_{pj} and i_{nj} are the upper arm current and the lower arm current of phase j (j=a,b,c), respectively, and i_{sj} is the output current of phase j (j=a,b,c).

The KVL equations of the upper arm and the lower arm can be listed as:

$$\begin{cases} v_j = \frac{1}{2}V_{dc} - v_{pj} - L\frac{di_{pj}}{dt} \\ v_j = -\frac{1}{2}V_{dc} + v_{nj} + L\frac{di_{nj}}{dt} \end{cases} \quad (2)$$

where v_{pj} and v_{nj} are the upper arm voltage and lower arm voltage of phase j (j=a,b,c), respectively, V_{dc} is the DC bus voltage and v_j is the output voltage of phase j (j=a,b,c).

From (1) and (2):

$$\begin{cases} v_j = \frac{1}{2}(v_{nj} - v_{pj}) - \frac{1}{2}L\frac{di_{sj}}{dt} \\ L\frac{di_{cirj}}{dt} = \frac{1}{2}V_{dc} - \frac{1}{2}(v_{nj} + v_{pj}) \end{cases} \quad (3)$$

It can be inferred that the output voltage depends on the voltage difference between the upper arm and the lower arm. In addition, the circulating current is controlled by the voltage summation of the upper arm and the lower arm. The fundamental frequency of the output voltage and current at the ac side of the MMC can be described as:

$$\begin{cases} v_j = V_{sm}\sin(\omega t + \theta_V) \\ i_{sj} = I_{sm}\sin(\omega t + \theta_I) \end{cases} \quad (4)$$

where θ_V and θ_I are the initial phase angles of the output voltage and current, and V_{sm} and I_{sm} are the amplitude of the output voltage and current.

If the power losses are neglected, the active power of the ac side and the dc bus should be equal.

$$3V_{sm}I_{sm}\cos\theta/2 = V_{dc}\times I_{dc} \quad (5)$$

where I_{dc} is the DC input current and θ is the load impedance angle, θ=θ_V-θ_I. θ is in the range of [-π/2,π/2].

Then the following equation can be acquired:

$$I_{dc} = \frac{3V_{sm}I_{sm}\cos\theta}{2V_{dc}} = \frac{3}{4}m_V I_{sm}\cos\theta \quad (6)$$

where m_V is the voltage modulation index, m_V=V_{sm}/(V_{dc}/2).

The arm voltage and current can be calculated as [19]:

$$\begin{cases} v_{pj} = \frac{V_{dc}}{2} - v_j = \frac{V_{dc}}{2}(1 - m_V\sin(\omega t + \theta_V)) \\ v_{nj} = \frac{V_{dc}}{2} - v_j = \frac{V_{dc}}{2}(1 + m_V\sin(\omega t + \theta_V)) \end{cases} \quad (7)$$

$$\begin{cases} i_{pj} = \frac{I_{dc}}{3} + \frac{i_{sj}}{2} = \frac{I_{sm}}{2}[\frac{1}{2}m_V\cos\theta + \sin(\omega t + \theta_I)] \\ i_{nj} = \frac{I_{dc}}{3} - \frac{i_{sj}}{2} = \frac{I_{sm}}{2}[\frac{1}{2}m_V\cos\theta - \sin(\omega t + \theta_I)] \end{cases} \quad (8)$$

[11] and [20] calculate the arm current, analyze the fluctuation of the capacitor voltage in detail, and point out that the total energy of the arm can be balanced naturally in the steady state.

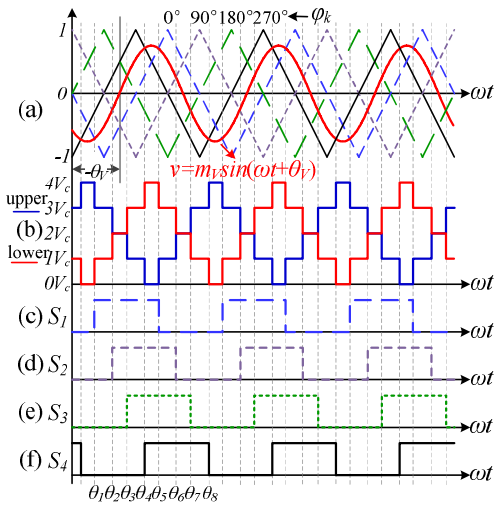


Fig. 2. CPS-PWM modulation process.

III. Derivation of the Fundamental Frequency Sorting Algorithm

A. CPS-PWM with a Fundamental Carrier Frequency

In high power applications, the power switches are always operated at a low switching frequency due to a power loss limitation. In this paper, CPS-PWM with a fundamental carrier frequency is adopted for a Modular Multilevel Converter, in order to limit the switching losses. The 5-level CPS-PWM modulation process with a fundamental carrier frequency is carried out as an example in Fig. 2. The initial phase angles of the N carriers φ_k (k=1, 2, ⋯, N) are 0, 2π/N, ⋯, (k-1)2π/N, ⋯, (N-1)2π/N. The stair waveforms of the upper arm voltage and the lower arm voltage are shown in Fig. 2(b). The drive signals S_k (k=1, 2, ⋯, N) for the lower arms are generated by the N carriers and the modulation signal, as shown in Fig. 2(c), (d), (e) and (f). The N drive signals for the upper arm are opposite to the N drive signals for the lower arm. The switching angles of the k^{th} drive signal S_k are θ_k and θ_{N+k}. Considering the symmetry of the carriers and the modulation waveforms, the switching angles satisfy (9).

$$\begin{cases} m_V\sin(\theta_k + \theta_V) = -\frac{2}{\pi}(\theta_k + 2q\pi - \varphi_k), & k = 1,2,\cdots,N \\ \theta_{N+k} = \pi + \theta_k, & k = 1,2,\cdots,N \end{cases} \quad (9)$$

where q is an integer, q=-∞,⋯,-1,0,1,⋯,+∞.

Unfortunately, the exact expression of θ_k is very complicated and hard to calculate. It depends on the modulation index m_V, the phase angle of the output voltage θ_V and the initial phase angles of the carriers φ_k. When the modulation signal is kept stable, m_V and θ_V are constant so that only θ_k depends on φ_k. The Fourier series expansion of the k^{th} drive signal S_k can be expressed as:

$$d_k = \frac{1}{2} + \frac{2}{\pi}\sum_{m=1,3,5,\cdots}^{\infty}\frac{1}{m}\sin m(\omega t - \theta_k), \quad k = 1,2,\cdots,N \quad (10)$$

As a special case, there are six crossing points between a few

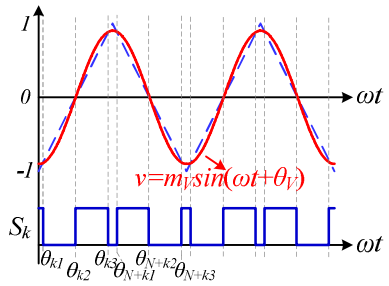


Fig. 3. Six crossing points for CPS-PWM under specific condition.

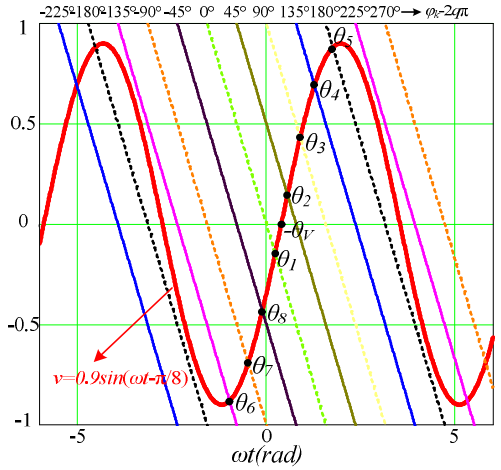


Fig. 4. Solving the switching angles with Mathcad.

carriers and the modulation waveforms when $m_V>2/\pi$, as shown in Fig. 3. Suppose the switching angles are θ_{k1}, θ_{k2}, θ_{k3}, θ_{N+k1}, θ_{N+k2}, θ_{N+k3}. With the method mentioned above, the FFT expressions of the k^{th} driving signals S_k can be analyzed as:

$$\begin{aligned} d_k &= \frac{1}{2}+\frac{2}{\pi}\sum_{m=1,3,5,\cdots}^{\infty}\frac{1}{m}[-\sin m(\omega t-\theta_{k1})] \\ &+\frac{2}{\pi}\sum_{m=1,3,5,\cdots}^{\infty}\frac{1}{m}[\sin m(\omega t-\theta_{k2})] \\ &+\frac{2}{\pi}\sum_{m=1,3,5,\cdots}^{\infty}\frac{1}{m}[-\sin m(\omega t-\theta_{k3})] \\ &=\frac{1}{2}+\frac{2}{\pi}\sum_{m=1,3,5,\cdots}^{\infty}\frac{A_{mk}}{m}\sin m(\omega t-\theta_k) \end{aligned} \quad (11)$$

where A_{mk} and θ_k relate to the three switching angles θ_{k1}, θ_{k2} and θ_{k3}. Considering that the summation of θ_{k1} and θ_{k3} is approximately 2π, A_{mk} is near to 1 and θ_k is approximately θ_{k2}.

(10) and (11) can be simplified to an approximate unified expression as:

$$d_k=\frac{1}{2}+\frac{2}{\pi}\sum_{m=1,3,5,\cdots}^{\infty}\frac{1}{m}\sin m(\omega t-\theta_k),k=1,2,3,\cdots,N \quad (12)$$

For carriers that have only two crossing points, θ_k is just the switching angle. For carriers that have six crossing points, θ_k relates to the three switching angles θ_{k1}, θ_{k2} and θ_{k3}. θ_k is approximately θ_{k2}.

Fig. 4 presents a graph method to obtain the solution of θ_k for a 9-level MMC with Mathcad software, where the modulation index m_V is 0.9, the initial phase angle of the modulation signal θ_V is $-\pi/8$ and the number of sub-modules in one arm N is 8. It can be inferred that θ_k is nearly evenly distributed in the range $[-\theta_V-\pi/2, -\theta_V+\pi/2]$. If the equivalent switching angle β_k is defined as (13), then β_k is in the range $[-\pi/2,\pi/2]$.

$$\beta_k=\theta_k+\theta_V,k=1,2,3,\cdots,N \quad (13)$$

(12) can be derived as:

$$d_k=\frac{1}{2}+\frac{2}{\pi}\sum_{m=1,3,5,\cdots}^{\infty}\frac{1}{m}\sin m(\omega t+\theta_V-\beta_k) \quad (14)$$

B. Capacitor Voltage Balance Analysis

Under the CPS-PWM with a fundamental carrier frequency, the capacitor voltage increments of the lower arm sub-modules can be calculated by:

$$\Delta v_{ck}=\frac{1}{C}\int_0^t d_k\times i_{nj}dt \quad (15)$$

The capacitor voltage increment Δv_{ck} contains a dc component, the fundamental frequency and its integer multiple components. Therefore, the capacitor voltage increment in a fundamental period can be calculated by:

$$\Delta V_{cTk}=\frac{1}{C}\int_0^T d_k\times i_{nj}dt=\frac{I_{sm}}{\omega C}[\frac{\pi}{4}m_V\cos\theta-\cos(\theta-\beta_k)] \quad (16)$$

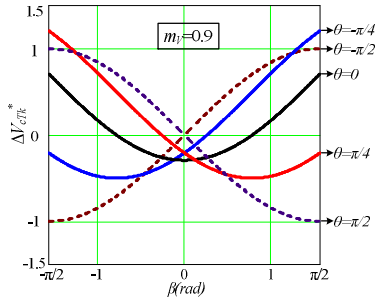
The capacitor voltage increment is proportionate to the load current and it relates to the power factor of the load and the modulation index. Define $I_{sm}/\omega C$ as the normalized reference of the voltage increment so that the normalized voltage increment can be obtained.

$$\Delta V_{cTk}^{*}=\Delta V_{cTk}/\frac{I_{sm}}{\omega C}=\frac{\pi}{4}m_V\cos\theta-\cos(\theta-\beta_k) \quad (17)$$

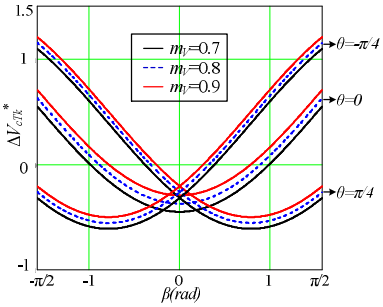
The relationship between the voltage increment during a fundamental period and the equivalent switching angle β is indicated in Fig. 5. It can be seen that some carriers can charge the capacitors, while the others can discharge the capacitors in a fundamental period. Thus, the capacitors will diverge soon without a balancing method.

C. FFSA based Balancing Method

As described above, N drive signals can be generated by the CPS-PWM. However, the capacitor voltage of the N sub-modules will be unbalanced if the N sub-modules are driven with a fixed sequence. Since different carriers have a different impact on the capacitors, alternating the sequence of the carriers in a fundamental period can change the charging state of the sub-modules. The capacitor voltage increments in a fundamental period can be used as criterion to judge which carrier can charge the most and which can discharge the most. Then let the carrier charging the most drive the sub-module with the lowest capacitor voltage, and let the carrier charging the second most to drive the sub-module with the second lowest capacitor voltage. Then deal with the other carriers in



(a) Influence of the load impedance angle θ.



(b) Influence of the modulation index m_V.

Fig. 5. capacitor voltage increment vs equivalent switching angles.

the same way. In this way, the N drive signals can match the N sub-modules one by one with the best sequence.

The detailed operation process of a FFSA based on the dual sorting mechanism is shown in Fig. 6. Firstly, calculate the capacitor voltage increments during the previous fundamental period. Then sort the capacitor voltage increments in descending order and sort the present capacitor voltage in ascending order at the minimum point of the output voltage. The next step is to determine the carriers corresponding to the voltage increments and the sub-modules corresponding to the present capacitor voltage. At last, the re-matching relationship between the carriers and the sub-modules can be carried out and the driving sequence can be changed immediately. Note that the sorting and the driving sequence change can guarantee the fundamental sorting frequency and avoid the extra switching commutation because all of the sub-modules are bypassed at the minimum point of the output voltage with N+1 levels.

The sorting frequency can be effectively reduced with the FFSA. However, the calculation resources consumed in one sorting process increase due to the dual sorting mechanism. This problem can be solved through the following three ways. Firstly, the calculation resources can be saved by dividing the whole sorting process into many asynchronous parts so that these parts can share some of the logic resources in the Field Programmable Gate Array (FPGA) controller. Even though the executing speed of the sorting process is reduced, this method has little influence on the performance of the FFSA due to its low sorting frequency. Secondly, the relationship curve of the

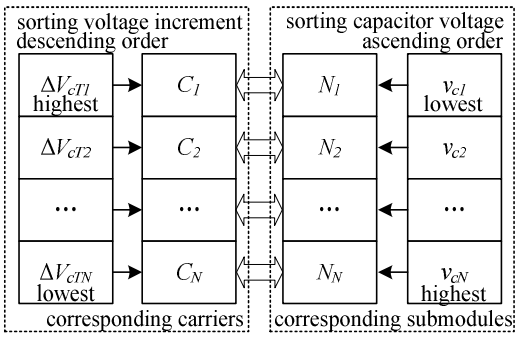


Fig. 6. FFSA with dual sorting mechanism.

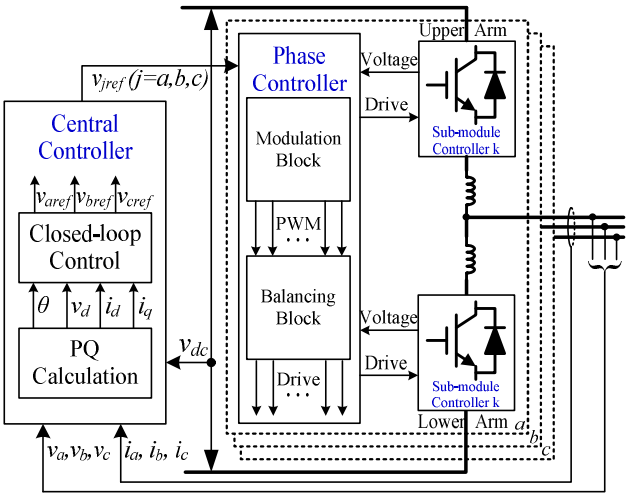


Fig. 7. Implementation of the proposed balancing method.

voltage increment and the switching angle has a minimum point, as shown in Fig. 5. The voltage increment enlarges with an increase in the absolute difference between the equivalent switching angle β and the minimum point. With this method, only after the minimum point is determined by the sorting algorithm, the sorting result of the voltage increments can be carried out. Thus, the calculation resources can be greatly saved. Thirdly, it does not need to sort the present voltages completely. Only the largest and lowest voltages, which are beyond the specified range, should be determined. Let the carriers which can discharge the most drive the sub-modules with the highest voltage, let the carriers which can charge the most drive the sub-modules with the lowest voltage, and let the other carriers drive the remaining sub-modules. With these methods, the calculation resources can be reduced a lot.

The proposed balancing method is implemented with the control system shown in Fig. 7. The whole control system includes three-level controllers. The central controller is composed of a DSP and a FPGA, while each of the phase controllers is made up of a FPGA. The main task of the central controller is to calculate the active power and the reactive power and to implement the closed-loop control algorithm. The modulation process and the balancing algorithm are executed

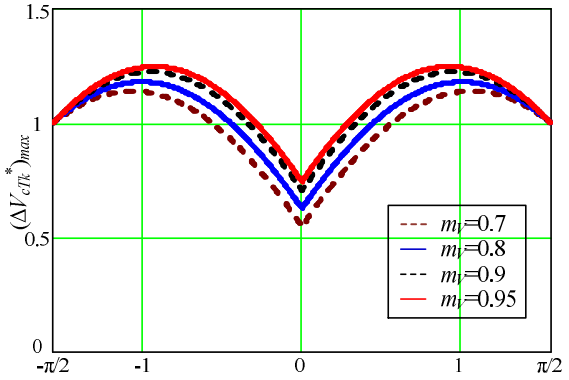


Fig. 8. The maximum ripple of DC bias with different load.

in the phase controller. The PWM signals generated by the modulation block should not drive the sub-modules directly. They are arranged in a proper order by the balancing block. The sub-module controller, which consists of a DSP, generates two driving signals with dead time according to the driving signals transmitted from the phase controller and it samples the capacitor voltage of the sub-module.

D. Capacitor Voltage Ripple with the FFSA

There are two factors that make the capacitor voltage fluctuate. One is the AC fluctuation whose ripple frequency is a multiple of the fundamental frequency. The other is the fluctuation of the DC bias. The rated sub-module capacitor voltage is 1/N of the DC bus voltage V_{dc}. However, the DC bias fluctuates with the FFSA. When β_k is π/2 or -π/2, the DC bias in one fundamental period can obtain its maximum value.

$$(\Delta V_{cTk}{}^*)_{\max} = \frac{\pi}{4} m_V \cos\theta + \sin|\theta| \tag{18}$$

Note that β_k is the equivalent switching angle and β_k is a discrete constant so that (18) is an appropriate expression. The curve of the maximum ripple of the DC bias is shown in Fig. 8. With a different load or a different modulation index, the maximum ripple varies. It can be seen that the maximum value of the maximum ripple of the capacitor voltage occurs when the load is a resistive-inductive or a resistive-capacitive load, not a pure resistor, inductor or capacitor. When the load impedance angle is (19), the maximum ripple of the DC bias obtains its maximum value (20). When the load is a pure resistive load, the maximum ripple of the DC bias acquires its minimum value $\pi m_V/4$.

$$\theta = \pm \arctan\frac{4}{\pi m_V} \tag{19}$$

$$(\Delta V_{cTk})_{\max} = \frac{Ism}{\omega C}\left(1+\frac{\pi m_V}{4}\right)\frac{1}{\sqrt{1+\left(\frac{4}{\pi m_V}\right)^2}} \tag{20}$$

(20) can be used as a criterion to choose the DC capacitance, in order to limit the ripple of the DC bias of the capacitor voltage.

TABLE I
SPECIFICATION OF THE SIMULATION MODEL

Parameters	Value
DC bus voltage (V_{dc})	6000V
Modulation index (m_V)	0.9
Output frequency (f)	50Hz
Number of SMs in each arm (N)	8
Arm inductance (L)	30mH
SM capacitance (C)	3mF
Load inductance (L_s)	15mH
Load resistance (R)	75Ω
Rated capacitor voltage (V_c)	750V
Equivalent switching frequency (Nf_{sw})	400Hz

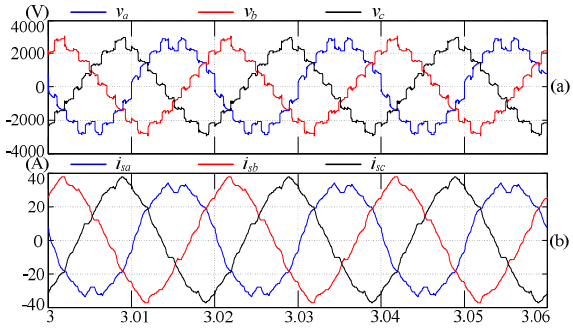


Fig. 9. Output voltage and current.

IV. SIMULATION VERIFICATION

In order to verify the effectiveness of the proposed balancing method, the 9-level three phase inverter shown in Fig. 1 is simulated in MATLAB. The detailed specifications of the whole system are listed in Table I.

The output voltage and current waveforms are shown in Fig. 9. The voltage of phase a is different from phase b and phase c because of the six crossing points between a few carriers and the modulation signal. For the FFSA, the corresponding relationship between the carriers and the sub-modules changes every fundamental period, as shown in Fig. 10. The sorting flag is shown in Fig. 10(b), and the carriers corresponding to the first and fourth sub-module in the upper arm and lower arm of phase a are presented in Fig. 10 (c), (d), (e) and (f). The drive signals for the first, third, fifth and seventh sub-modules in the upper arm of phase a are indicated in Fig. 11 (a), (b), (c) and (d). The summation of all the drive signals for the upper arm of phase a is shown in Fig. 11(e). From these simulation results, the switching frequencies of all of the sub-modules are equal.

Fig. 12 demonstrates the perfect performance of the proposed balancing method, regardless of the steady state or dynamic state. At 0.7s, the startup of the simulation system is finished and all of the capacitors are charged to 750V. Then, the inverter is working in an open loop with no balancing algorithm. The capacitor voltages are divergent and start to converge when the FFSA is effective at 0.75s. The capacitor

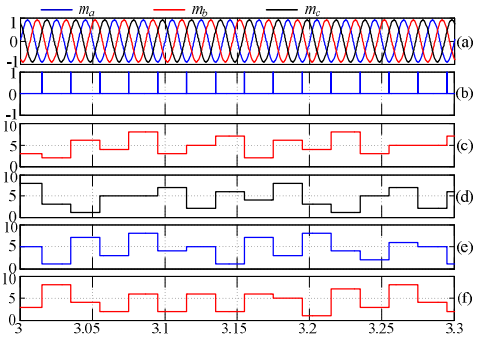


Fig. 10. Changing process of the drive sequence with FFSA.

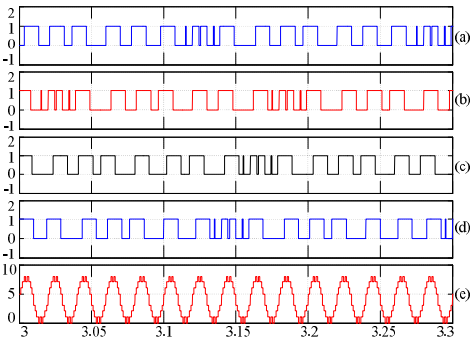


Fig. 11. Drive signals of the upper switch in each sub-module.

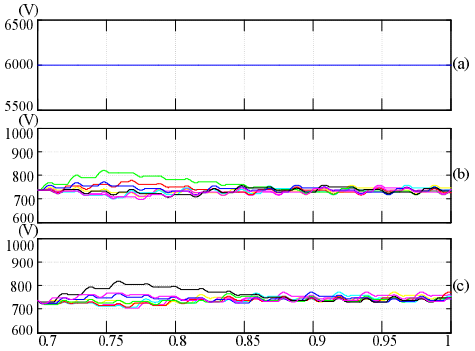
voltages are eventually stable at 750V. When the load is changed at 1.8s, the capacitor voltages can also be stable. The voltage ripples are a little bit larger under a heavy load. At 2.3s, the input voltage starts to decrease with a slope of *25000V/s* until *5000V*. With the FFSA, the capacitor voltages can be well balanced and stable at 625V. It can be inferred that the performance of the FFSA is quite good regardless of input voltage or load changes.

V. EXPERIMENTAL RESULTS

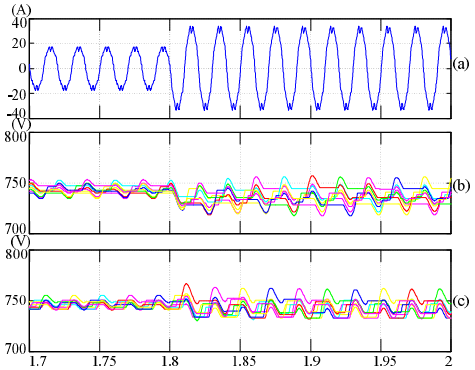
A down-scaled one-phase prototype is assembled to prove the proposed capacitor voltage balancing method. The configuration of the experimental system is presented in Fig. 13. The parameters of the prototype are indicated in Table II. The DC bus voltage is generated by an auto-transformer with a three phase diode rectifier.

Fig. 14 shows the experimental results of the CPS-PWM with a fundamental carrier frequency. The output voltage and arm voltages are all 9-level staircase waveforms. The switching frequencies of the fifth, the sixth sub-module of the upper arm and the fifth sub-module of the lower arm are equal to the fundamental frequency, as shown in Fig. 15. This proves that the switching frequencies between different sub-modules can be evenly distributed with the proposed balancing method.

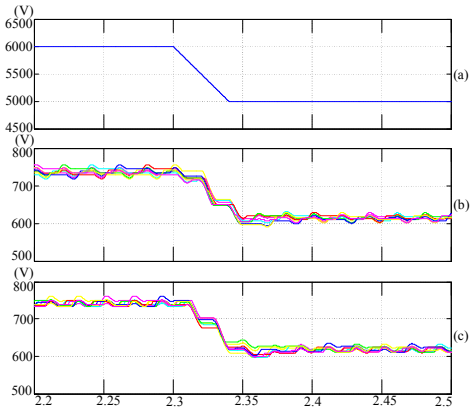
The proposed FFSA-based capacitor voltage balancing method is verified with the open-loop output voltage control strategy. The DC bus voltage is 600V and the modulation index remains at 0.9. Fig. 16 and Fig. 17 show the steady-state



(a) Steady state result.



(b) Load increasing simulation.



(c) Input voltage increasing simulation.

Fig. 12. Simulation results of the proposed balancing method.

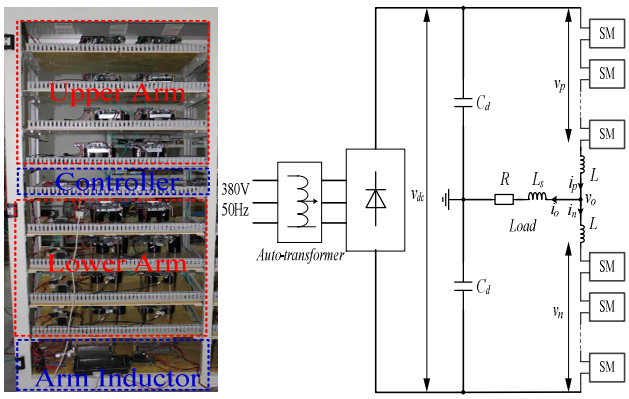


Fig. 13. Configuration of the experimental system.

TABLE II
SPECIFICATION OF THE EXPERIMENTAL SYSTEM

Parameters	Value
DC bus voltage (V_{dc})	600V
DC bus Capacitance (C_d)	3mF
Modulation index (m_V)	0.9
Output frequency (f)	50Hz
No of SMs in each arm (N)	8
Arm inductance (L)	30mH
SM capacitance (C)	3mF
Load inductance (L_s)	15mH
Load resistance (R)	25Ω
Rated capacitor voltage (V_c)	75V
Switching frequency (f_{sw})	50Hz
Equivalent switching frequency (Nf_{sw})	400Hz

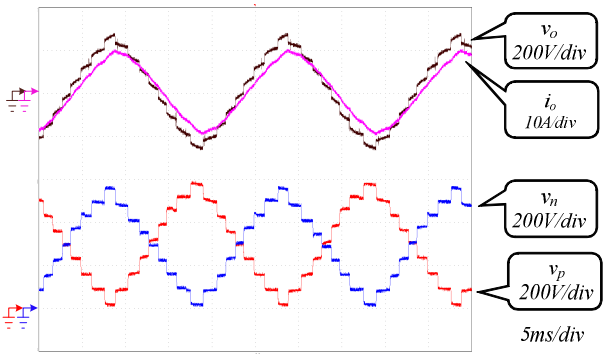


Fig. 14. Experimental results of CPS-PWM.

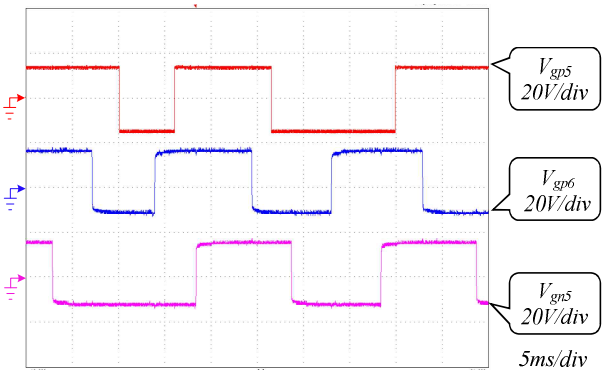
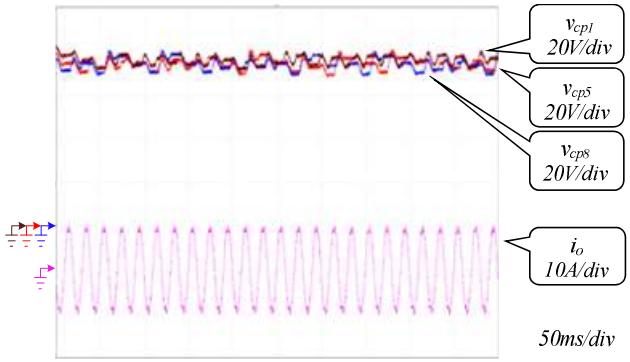
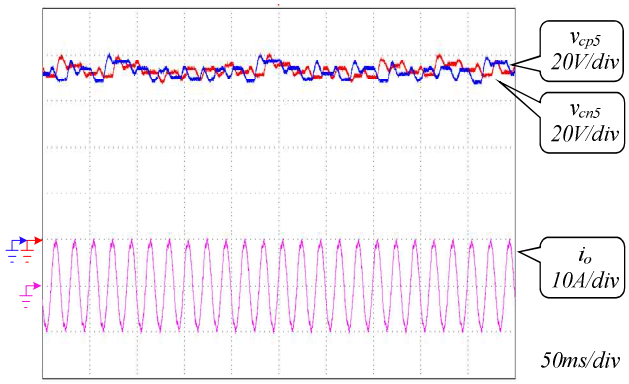


Fig. 15. Drive signals of the upper switch in each sub-module.

and dynamic results, respectively. For the steady state, the DC bias can be stable at 75V, and the ripple of the capacitor voltage is about ±5V. For the dynamic performance, experimental results under the conditions where the load increases, the load decreases and the DC bus voltage increases are carried out. When the load resistance changes from 50Ω to 25Ω or from 25Ω to 50Ω, the capacitor voltages can be stable at 75V. Only the ripples of the capacitor voltages increase a little under a heavy load. When the DC bus voltage increases from 300V to 600V by the auto-transformer, the DC bias of the capacitor voltages increases from 38V to 75V. The capacitor voltages can be well balanced with the proposed FFSA-based capacitor voltage balancing method.

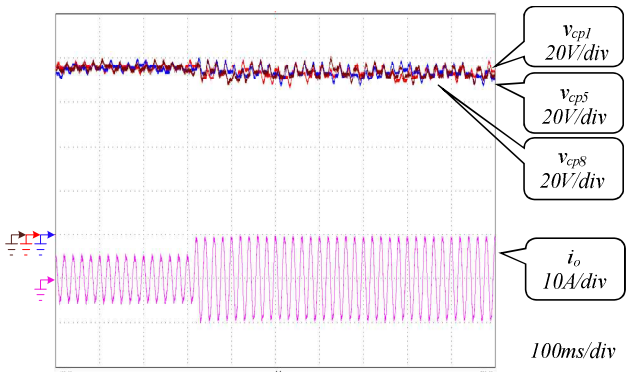


(a) Capacitor voltages of the upper sub-modules.

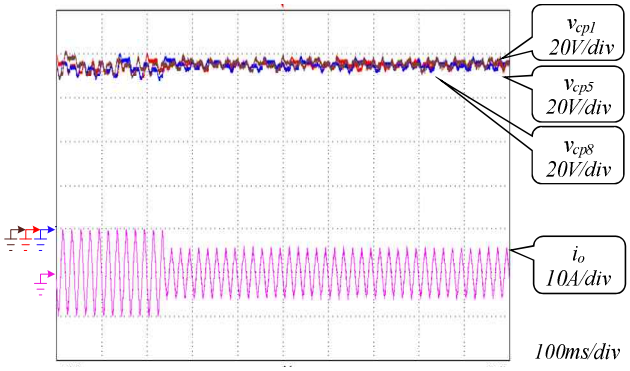


(b) Capacitor voltages of the upper arm and lower arm.

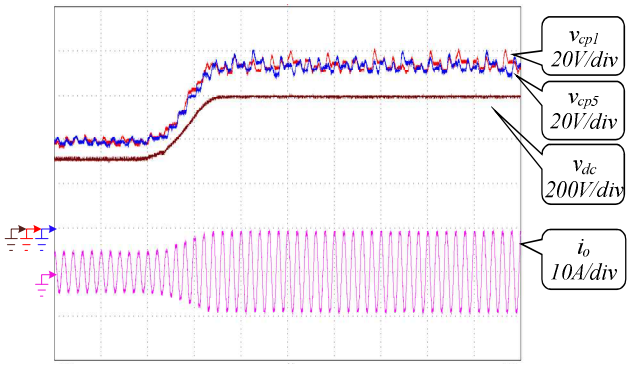
Fig. 16. Steady-state results of proposed balancing method.



(a) Load increasing experiment.



(b) Load decreasing experiment.



(c) Input voltage stepping up experiment.

Fig. 17. Dynamic results of proposed balancing method.

VI. CONCLUSIONS

In this paper, a fundamental frequency sorting algorithm based on the dual sorting mechanism is proposed to balance the dc capacitor voltages of MMCs. Excessive frequent sorting can be avoided and a lot of calculation resources can be saved for the controllers. Thus, more sub-modules can be dealt with. This can also be adapted to the large-scale MMCs. Furthermore, the arm currents do not need to be measured so that the architecture of the control system can be simplified and the current sensors can be saved. Moreover, the switching frequencies of the switches are evenly distributed between the different sub-modules. As a result, the thermal design can be simplified. Simulation and experimental results verify the correctness of the proposed FFSA-based capacitor voltage balancing method.

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