JPE 14-6-5

http://dx.doi.org/10.6113/JPE.2014.14.6.1119
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Novel Five-Level Three-Phase Hybrid-Clamped Converter with Reduced Components

Bin Chen*, Wenxi Yao†, and Zhengyu Lu*

*†Department of Electrical Engineering, Zhejiang University, Hangzhou, China

Abstract

This study proposes a novel five-level three-phase hybrid-clamped converter composed of only six switches and one flying capacitor (FC) per phase. The capacitor-voltage-drift phenomenon of the converter under the classical sinusoidal pulse width modulation (SPWM) strategy is comprehensively analyzed. The average current, which flows into the FC, is a function of power factor and modulation index and does not remain at zero. Thus, a specific modulation strategy based on space vector modulation (SVM) is developed to balance the voltage of DC-link and FCs by injecting a common-mode voltage. This strategy applies the five-segment method to synthesize the voltage vector, such that switching losses are reduced while optional vector sequences are increased. The best vector sequence is then selected on the basis of the minimized cost function to suppress the divergence of the capacitor voltage. This study further proposes a startup method that charges the DC-link and FCs without any additional circuits. Simulation and experimental results verify the validity of the proposed converter, modulation strategy, and precharge method.

Key words: Capacitor precharge, Capacitor-voltage balancing, Hybrid-clamped converters, Multilevel converters, Space vector modulation

I. INTRODUCTION

Multilevel converters have attracted considerable attention from both the industry and the academia for their use in high-power applications, such as high-voltage direct-current (HVDC) transmission, reactive power compensation, and medium-voltage industrial drives [1]. In this voltage range, multilevel converters are preferred to overcome the voltage blocking limitations of the available semiconductor switches [2], [3]. Multilevel converters used in low voltage have recently become a focus [4]-[7], given that such technology can produce more levels than the conventional two-level converters in the output voltage waveforms, thus resulting in a superior harmonic spectrum and lower switching losses [8]. However, in multilevel converters, the increasing number of components containing switches, clamping diodes, and capacitors tends to increase the conduction losses and reduce the overall reliability [9]. Thus, to design a multilevel converter with reduced components remains an attractive but challenging task.

The basic concept of a multilevel converter is to synthesize a desired AC voltage through several voltage levels, which are produced by separate DC sources or large capacitors with voltage balance control. Among numerous multilevel converter topologies that have been proposed over the past decades, three classic or traditional topologies exist. These topologies are the neutral point clamped (NPC) [10], [11], the flying capacitors (FCs) [12], and the cascade H-bridge (CHB) [13]. In CHB converters, several isolated DC sources are necessary to produce active power. The DC sources are mainly generated by isolation transformers, which are bulky and expensive [1]. Thus, the NPC and FC with a single DC source is preferred. In NPC, different voltage levels are provided by series DC-link capacitors. However, the NPC converter providing more than three levels requires numerous clamping diodes and encounters a voltage-drift phenomenon in some operating regions [14]-[16]. Correspondingly, the operating regions are enlarged in FC converters, in which different voltage levels are clamped by FCs in each phase. However, massive FCs are required as voltage level increases, thus increasing the cost and control complexity [17].

According to the aforementioned drawbacks of NPC and FC, low-level converters are commercially used in industrial applications, such as the 3L-NPC and 4L-FC [18]. To improve the voltage levels with one DC source, hybrid multilevel converters are developed [19]. In hybrid multilevel converters,

Manuscript received Jun. 9, 2013; accepted Oct. 2, 2014
Recommended for publication by Associate Editor Rae-Young Kim.
†Corresponding Author: ywxi@zju.edu.cn
Tel: +86-571-87951950, Zhejiang University
*Department of Electrical Engineering, Zhejiang University, China

more voltage levels can be generated with the same number of components by adopting different intermediate-circuit capacitor voltages [9]. The NPC-HB multilevel converter, which is composed of a series connection of a main three-level NPC converter and an auxiliary floating H-bridge, has been studied in [3], [9], and [20]. Given the different capacitor voltages of the H-bridge, the NPC-HB converter can be a five-, seven-, or nine-level converter, which is flexible and attractive. However, eight switches are used in each phase of the NPC-HB, and four series switches should pass through the conduction path. The conduction voltage drop is relatively large if the converter is adopted in low-voltage applications. A five-level active neutral-point clamped (ANPC) converter is another attractive hybrid converter [21]-[23] that can be considered as the combination of a three-level ANPC converter and a two-level cell. Eight switches are necessary for one phase of ANPC if different blocking-voltage switches are adopted. In this case, three switches, fewer than that in NPC-HB, are on the conduction path.

Based on the principles of reducing components and conduction losses, a novel five-level hybrid converter is proposed in this study. Each phase of the proposed converter contains only six switches, and the switches on the conduction path are reduced to two. The hybrid converter is a combination of an FC cell and a three-level transistor-clamped converter (TCC), which has high efficiency in low-voltage applications [6].

This paper is organized as follows: Section II introduces the topology and operating principles of the proposed converter. Section III presents an analysis of the voltage-drift phenomenon of the converter based on SPWM. Section IV discusses a modulation strategy based on space vector theory to balance the voltage of DC-link and FCs. Section V evaluates the performance of the introduced converter under the proposed modulation strategy in various operating conditions on the basis of simulation studies. Section VI presents the implementation of the method to precharge capacitors before the converter startup without additional circuits. In addition, the feasibility of the converter and modulation strategy is verified through an experiment.

II. CONVERTER TOPOLOGY

A. Proposed Five-Level Hybrid-Clamped Converter

Fig. 1 shows the topology of Phase A. The hybrid converter combines the 3L-TCC and FC cell into one circuit. In the converter, S_5 and S_6 are combined into a bidirectional switch. Another type of the bidirectional switch could also be selected, as discussed in [24]. As shown in Fig. 1, the DC bus is composed of two series capacitors, C_{d1} and C_{d2}, which is shared by three phase legs. If the DC-link voltage is assumed constant and equals 4E, where E is the voltage across the FC C_{fa}, then the voltage across C_{d1} or C_{d2} is 2E. The two series DC-link

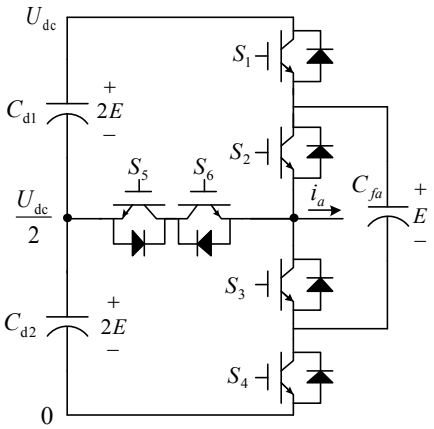

Fig. 1. Phase A of the proposed five-level hybrid-clamped converter.

capacitors provide three voltage levels. Combining the function of the FC C_{fa}, a five-level voltage waveform can be generated at the output point. Six switches are used in one phase of the proposed converter. The voltage stresses of (S_1, S_4), (S_5, S_6), and (S_2, S_3) are 3E, 2E, and E, respectively.

Insulated gate bipolar transistors (IGBTs), which are mostly used in applications in which breakdown voltage should be larger than 600 V, such that the voltage drops change slightly under different voltage levels at the same rated current and technology. As explained in [5], 1200 V IGBTs feature on-state voltages that are roughly 10% larger than that of a 600 V IGBT. Correspondingly, the switching loss energies of a 1200 V IGBT are larger by a factor of 3 to 5. In an appropriate modulation strategy, such as the method proposed in [19], higher voltage cells could operate at lower switching times to reduce switching losses. In situations in which the breakdown voltage is smaller than 300 V, metal-oxide-semiconductor field-effect transistors (MOSFETs) could be used to reduce conduction losses further.

The numbers of the components in different five-level converter topologies are compared in Table I. The components include switches, clamping diodes, and FCs. Given that the smaller number of components tends to improve reliability and reduce conduction losses, different voltage ratings of power semiconductors are used to minimize the component numbers in low-voltage applications, in which suitable voltage level switches are available. As shown in Table I, the largest advantage of the proposed circuit is the minimal number of components used. Furthermore, the only two power semiconductors are on the conduction path(illustrated in Part B), which indicates that the voltage drop on the conduction path is relatively low, thereby enabling the proposed converter to be employed in low-voltage applications. However, the proposed converter has a number of drawbacks. For instance, the voltage of the FCs is not naturally balanced. This drawback limits the operation region of the converter, which will be analyzed in Section III.

TABLE I
COMPARISON OF POWER SEMICONDUCTOR AND FC IN FIVE-LEVEL CONVERTERS

		5L-NPC [15]	5L-FC [25]	5L-ANPC [26]	Topology in [27]	Proposed topology
Switches	3E	-	-	-	-	6
	2E	-	-	12	-	6
	E	24	24	12	12	6
Clamping diodes	3E	6	-	-	-	-
	2E	6	-	-	12	-
	E	6	-	-	-	-
FCs	3E	-	3	-	-	-
	2E	-	3	-	3	-
	E	-	3	3	3	3
Total components		42	33	27	30	21
Power semiconductor on conduction path		2–4	4	3	3	2

Note: different voltage ratings of power semiconductor are used to minimize the component numbers

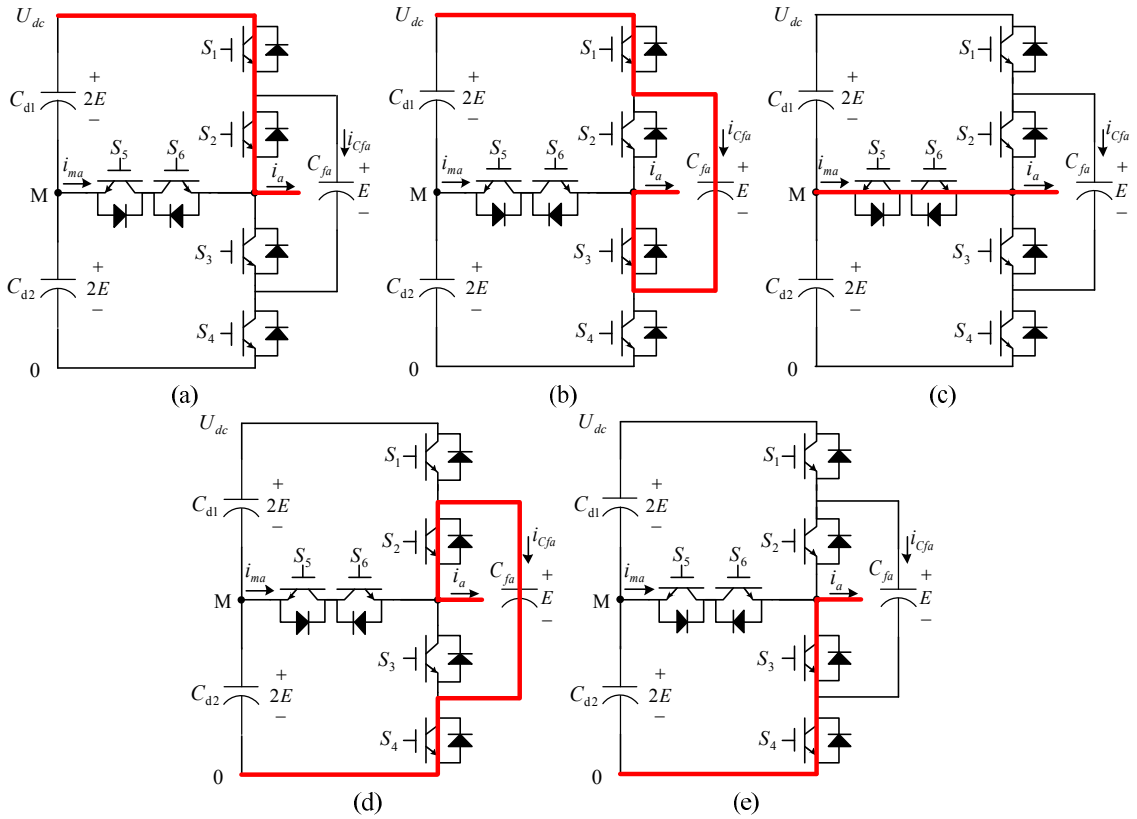

Fig. 2. Conduction paths of the five-level hybrid-clamped converter. (a) u_a=4E, Path.A; (b) u_a=3E, Path.B; (c) u_a=2E, Path.C; (d) u_a=E, Path.D; (e) u_a=0, Path.E.

B. Operation Principle

The conduction paths in different voltage levels of Phase A are shown in Fig. 2, where i_a is the output current, i_{Cfa} is the current flowing into the FC C_{fa}, and i_{ma} is the current flowing out of the middle point M. Only two switches are on the conduction path, regardless of the output voltage. For instance, if the output voltage is 0, switches S_3 and S_4 are on the conduction path. In the proposed converter, all available paths are maximally utilized. Five conduction paths correspond to five different voltage levels. However, no redundant conduction paths can be chosen to keep the FC voltage balanced in a switching period.

In different conduction paths, the adopted switching states are listed in Table II, where state condition 1 and 0 indicate ON and OFF switch status, respectively. As shown in this table, a conduction path corresponds to a set of switching states apart from Path.C. Two sets of switching state in Path.C are designed to avoid the phenomenon in which the output voltage

TABLE II
SWITCHING STATES OF THE PROPOSED FIVE-LEVEL HYBRID-CLAMPED CONVERTER IN PHASE A

Switching state	S_1	S_2	S_3	S_4	S_5	S_6	Vo	i_{ma}	i_{Cfa}	Conduction path
V4	1	1	0	0	0	1	4E	0	0	Path.A
V3	1	0	1	0	0	1	3E	0	i_a	Path.B
V2.A	0	0	1	0	1	1	2E	i_a	0	Path.C
V2.B	0	1	0	0	1	1	2E	i_a	0	Path.C
V1	0	1	0	1	1	0	E	0	$-i_a$	Path.D
V0	0	0	1	1	1	0	0	0	0	Path.E

is clamped to unwanted levels during dead-time periods [6], [21] when 2E voltage level is necessary. For example, assuming that the switching state V2.A is chosen when the output voltage changes between E and 2E, the output voltage will be clamped at 0 if the output current is positive during the dead-time period. The clamped voltage level of 0 should be avoided. Thus, the switching state of V2.A should be used to generate an output voltage larger than 2E. By contrast, V2.B is chosen to configure a voltage smaller than 2E.

This study adopts the phase-disposition (PD) PWM [28], [29] technique to control the proposed converter to output the expected voltage. PD-PWM is a simple method by which to relate each carrier with the gating signal of switches [1]. This technique generates relatively low total harmonic distortion [15]. PD-PWM is based on the comparison of a sinusoidal reference with four symmetrical carriers in a five-level converter. Fig.3 illustrates the sinusoidal PD-PWM waveforms of Phase A. Each phase contains three complimentary switch pairs, namely, $(S_2, \overline{S}_3)$, $(S_1, \overline{S}_5)$, and $(S_6, \overline{S}_4)$. For the two switches in a complementary pair, the switching states are converse. For example, if S_2 is in ON status, S_3 should remain in OFF status. As shown in Fig. 3, only a pair of complementary switches acts in each switching cycle. With high modulation index m and under low voltage stress, S_2 and S_3 switch more times within one fundamental period, which contributes to the reduction of the switching losses.

III. VOLTAGE-DRIFT PHENOMENON IN SPWM MODULATION

In the proposed hybrid converter with single DC source, the most critical issue is the voltage balancing problem of the clamping capacitors, including DC-link capacitors and FCs. The current flowing into the clamping capacitor implies the tendency of the voltage variation. Thus, the average current could be used to illustrate the voltage-drift phenomenon in the clamping capacitors. In this section, the relationships between the average current of the clamping capacitors and the proposed converter operating index, that is, modulation index and power factor, are deduced. An analysis is conducted in sinusoidal PD-PWM, as shown in Fig. 3.

Assuming that the output phase voltage and current are

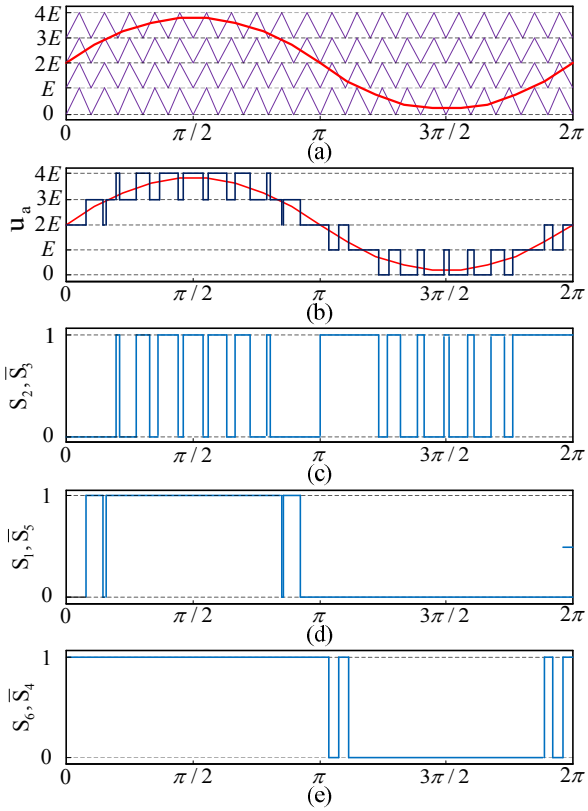

Fig. 3. Sinusoidal PD-PWM waveforms of the proposed five-level hybrid-clamped converter. (a) Carrier waveforms. (b) Phase voltage. (c)-(e) gating signals.

sinusoidal, we can reasonably assume that the three-phase system is symmetrical. Thus, one phase, for Phase A, could be used to analyze the voltage-drift phenomenon of the proposed converter. The voltage (1) and current (2) of Phase A can be expressed as follows:

$$u_a = (m \cdot \sin\theta + 1) \cdot 2E \quad (1)$$

$$i_a = I_m \cdot \sin(\theta - \varphi) \quad (2)$$

where θ is the phase voltage angle, I_m is the amplitude of the phase current, φ is the power factor angle, and m is the modulation index. In SPWM, the value of m is between 1 and 0 to output sinusoidal voltages.

In Phase A of the converter, the output current i_a flows out of the middle point M when a 2E voltage level is used to compose the wanted output voltage in PWM forms, as shown in Table II. For the FC C_{fa}, i_a flows out of C_{fa} when a 3E voltage level is selected. Thus, if i_a is positive, C_{fa} will be charged. By contrast, i_a flows into C_{fa} when E is used. In this situation, C_{fa} will be discharged when i_a is positive. According to the charging states of the clamping capacitors, one fundamental period of the phase voltage is divided into six regions, as shown in Fig.. To simplify the analysis, the assumption is made that the carrier frequency is significantly higher than fundamental frequency, such that the phase voltage and current can be considered as a constant in a carrier period.

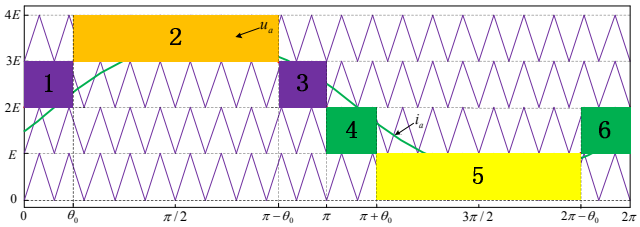

Fig. 4. Diagram of the six regions in one fundamental period of the phase voltage.

In Region.1, as shown in Fig. 4, the phase voltage angle θ covers from zero to θ_0 when m>0.5, where θ_0 is defined as:

$$\theta_0 = \arcsin\left(\frac{1}{2m}\right) \tag{3}$$

In this region, the instantaneous phase voltage changes between 2E and 3E to make the average voltage equal to u_a in a carrier period. According to the voltage-second-balance principle, the duty ratio of the higher voltage 3E in the carrier period can be deduced:

$$d_1 = 2m \cdot \sin\theta \tag{4}$$

In the duty ratio time, the phase current i_a flows into the FC. In other times, the phase current flows out of the middle point m. Thus, the average current flowing into FC in Region.1 is derived as:

$$\bar{i}_{Cfa1} = d_1 \cdot i_a \tag{5}$$

Integrating the current $\bar{i}_{Cfa1}$, the accumulated charge on the FC in Region.1 is acquired as:

$$Q_{Cfa1} = \int_0^{\theta_0} (d_1 \cdot i_a)\,d\theta = I_m \cdot 2m \cdot \int_0^{\theta_0} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \tag{6}$$

The average current flowing out of the middle point in Region.1 is derived as:

$$\bar{i}_{ma1} = (1-d_1)\cdot i_a \tag{7}$$

The output charge from the DC-link capacitor is calculated as:

$$\begin{aligned} Q_{ma1} &= \int_0^{\theta_0} ((1-d_1)\cdot i_a)\,d\theta \\ &= I_m \cdot \left(\int_0^{\theta_0} (\sin(\theta-\varphi))\,d\theta - 2m \cdot \int_0^{\theta_0} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \right) \end{aligned} \tag{8}$$

Based on similar calculations, the accumulated charge on the FC and the output charge from the middle point m in Region.2 to Region.6 are deduced as follows:

$$Q_{Cfa2} = I_m \cdot \begin{pmatrix} 2 \cdot \int_{\theta_0}^{\pi-\theta_0} (\sin(\theta-\varphi))\,d\theta \\ -2m \cdot \int_{\theta_0}^{\pi-\theta_0} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \end{pmatrix} \tag{9}$$

$$Q_{ma2} = 0 \tag{10}$$

$$Q_{Cfa3} = I_m \cdot 2m \cdot \int_{\pi-\theta_0}^{\pi} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \tag{11}$$

$$Q_{ma3} = I_m \cdot \begin{pmatrix} \int_{\pi-\theta_0}^{\pi} (\sin(\theta-\varphi))\,d\theta \\ -2m \cdot \int_{\pi-\theta_0}^{\pi} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \end{pmatrix} \tag{12}$$

$$Q_{Cfa4} = I_m \cdot 2m \cdot \int_{\pi}^{\pi+\theta_0} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \tag{13}$$

$$Q_{ma4} = I_m \cdot \begin{pmatrix} \int_{\pi}^{\pi+\theta_0} (\sin(\theta-\varphi))\,d\theta \\ +2m \cdot \int_{\pi}^{\pi+\theta_0} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \end{pmatrix} \tag{14}$$

$$Q_{Cfa5} = I_m \cdot \begin{pmatrix} -2 \cdot \int_{\pi+\theta_0}^{2\pi-\theta_0} (\sin(\theta-\varphi))\,d\theta \\ -2m \cdot \int_{\pi+\theta_0}^{2\pi-\theta_0} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \end{pmatrix} \tag{15}$$

$$Q_{ma5} = 0 \tag{16}$$

$$Q_{Cfa6} = I_m \cdot 2m \cdot \int_{2\pi-\theta_0}^{2\pi} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \tag{17}$$

$$Q_{ma6} = I_m \cdot \begin{pmatrix} \int_{2\pi-\theta_0}^{2\pi} (\sin(\theta-\varphi))\,d\theta \\ +2m \cdot \int_{2\pi-\theta_0}^{2\pi} (\sin\theta \cdot \sin(\theta-\varphi))\,d\theta \end{pmatrix} \tag{18}$$

Based on (6) and (8)-(18), when m>0.5, the average currents that flow into the FC or out of the middle point are respectively deduced as:

$$\bar{i}_{ma} = 0 \tag{19}$$

$$\bar{i}_{Cfa} = \frac{I_m \cdot \cos\varphi}{2\pi} \cdot \left(2m \cdot \left(4 \cdot \arcsin\left(\frac{1}{2m}\right) - \pi \right) + 4 \cdot \sqrt{1-\left(\frac{1}{2m}\right)^2} \right) \tag{20}$$

Given that the average current $\bar{i}_{ma}$ in a fundamental period remains at zero, the conclusion could be drawn that the voltages across the DC-link capacitors are naturally balanced under the SPWM method. However, the average current of the FC $\bar{i}_{Cfa}$ is a function of the modulation index and power factor. When the converter transforms nonzero real power, that is, $\cos\varphi \neq 0$, the current $\bar{i}_{Cf}$ is not zero, according to (19). This condition results in the deviations in the FC voltage.

Unlike the 5L-ANPC and 5L-FC converters, the proposed five-level converter has no redundant conduction paths to balance the FC voltage. To suppress the voltage-drift phenomenon, one direct method is to add auxiliary circuits for importing or exporting expected charges in FCs. Correspondingly, another method that injects common-mode voltage into the sinusoidal reference voltage is preferred without the addition of auxiliary circuits. To avoid the influence on the linear voltage of the three-phase five-level converter, the injected common voltages are composed of third harmonic and its multi-harmonics. Based on space vector theory, an excellent and flexible common-voltage injection method called space vector modulation (SVM) is developed. In the SVM-switching strategy, redundant switches can be used to prevent voltage drifts of DC-link and FCs in the same space vector of a linear voltage. In the next section, a balancing strategy based on a five-level SVM approach is proposed and analyzed.

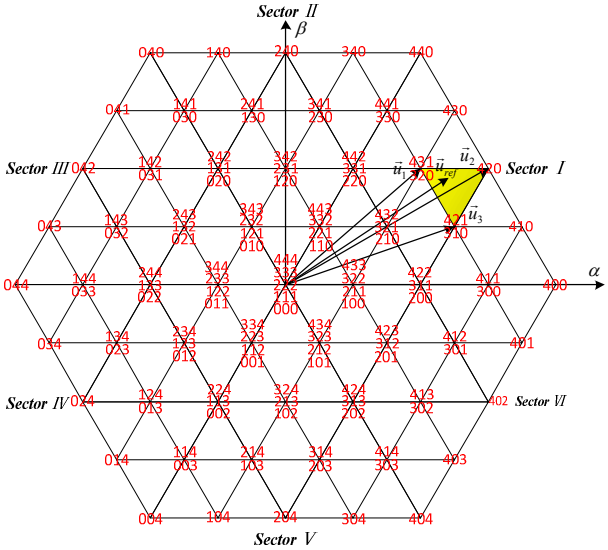

Fig. 5. Space voltage vectors and switching states of a three-phase five-level converter.

IV. Optimized SVM for Voltage Balance

A. Space Vector Diagram

The five-level three-phase inverter has $125(5^3)$ switching states. By applying Park's transformation, 61 space voltage vectors comprise these switching states. These vectors form 96 triangles distributed in six sectors on the $\alpha\beta$ coordinate, as shown in Fig. 5. The switching states are illustrated by 0, 1, 2, 3, and 4, which indicate the phase voltage of 0, E, 2E, 3E, and 4E, respectively. For the five-level SVM algorithm, the reference voltage vector $\vec{u}_{ref}(u_\alpha, u_\beta)$ must be located within a triangle formed by the three switching vectors adjacent to $\vec{u}_{ref}$. The three adjacent switching vectors constitute the best choice in synthesizing the reference voltage vector [30]. Similar to the shadowed triangle in Fig. 5, the reference voltage $\vec{u}_{ref}$ could be composed by vectors $\vec{u}_1$, $\vec{u}_2$, and $\vec{u}_3$ in a carrier period:

$$\vec{u}_{ref} = \vec{u}_1 \cdot T_1 + \vec{u}_2 \cdot T_2 + \vec{u}_3 \cdot T_3 \quad (21)$$

$$T_s = T_1 + T_2 + T_3 \quad (22)$$

where T_1, T_2, and T_3 are the duty cycle of the switching vectors $\vec{u}_1$, $\vec{u}_2$, and $\vec{u}_3$, respectively.

To reduce the switching losses, the five-segment method is used [31], [32] to synthesize the reference voltage vector $\vec{u}_{ref}$. For instance, the vector $\vec{u}_{ref}$ in Fig. 5 can be constituted by three vector sequences as shown in Fig. 6. With the five-segment method, one of the three phase voltages will stay still within a carrier period, and only four switching commutations are necessary, a reduction of one-third in comparison with the seven-segment method in [21]. Based on the number of switching states on each voltage vector, which

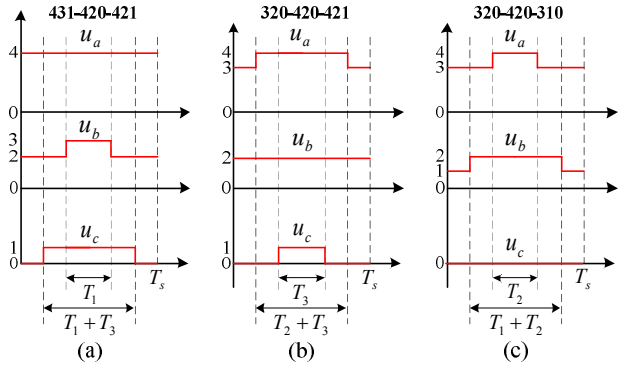

Fig. 6. Three vector sequences constitute the voltage vector $\vec{u}_{ref}$ in Fig. 5.

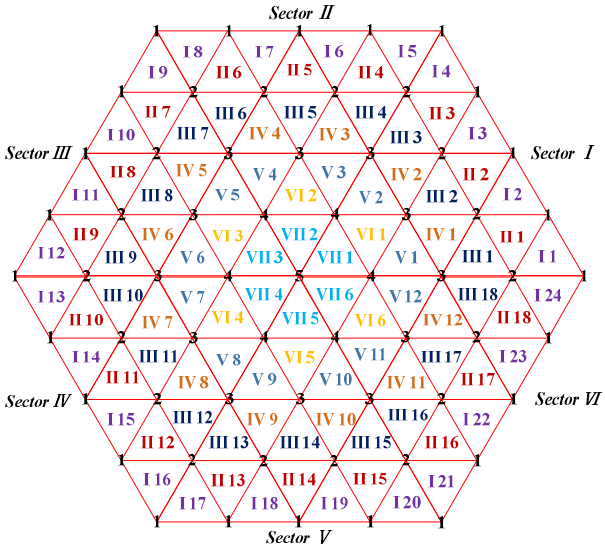

Fig. 7. Diagram of the triangles in seven categories of a three-phase five-level converter.

TABLE III
Number of Vector Sequences in Seven Category Triangles

Category	I	II	III	IV	V	VI	VII
Triangles	24	18	18	12	12	6	6
vector sequences	2	3	5	6	8	9	11

are labeled on the top of the switching vectors, the 96 triangles can be divided into seven categories, as shown in Fig. 7. In different categories, the numbers of optional vector sequences based on the five-segment method are listed in Table III. Apart from the advantage of reducing the typical one-third switching losses, the five-segment method also has more optional vector sequences to balance the voltage of DC-link and FCs, compared with the seven-segment method in [21].

B. Voltage-Drift Suppression

As the vector sequences in each triangle are not unique, this part shows how to select a proper vector sequence to suppress the voltage-drift phenomenon. Similar to [15] and [33], the positive-definite cost function based on the voltage deviations of DC-link and FCs is defined as:

$$J=\frac{1}{2}\sum_{x=a,b,c}C_{fx}\left(u_{Cfx}-E\right)^2+\frac{1}{2}\sum_{i=1,2}C_{di}\left(u_{Cdi}-2E\right)^2 \quad (23)$$

In the proposed five-level converter, assuming that the FCs of each phase and the series DC-link capacitors are equal, respectively, i.e., $C_{fa}=C_{fb}=C_{fc}=C_f$ and $C_{d1}=C_{d2}=C_d$, Equation (23) is simplified as:

$$J=\frac{1}{2}C_f\sum_{x=a,b,c}\Delta u_{Cfx}^2+\frac{1}{2}C_d\sum_{i=1,2}\Delta u_{Cdi}^2 \quad (24)$$

where $\Delta u_{Cfx}=u_{Cfx}-E$ and $\Delta u_{Cdi}=u_{Cdi}-2E$ are voltage deviations from their nominal voltage. If the DC-link and the FC are kept at their nominal values, the cost function J can be minimized to zero. The mathematical condition to minimize J is [15]:

$$\frac{dJ}{dt}=C_f\sum_{x=a,b,c}\Delta u_{Cfx}i_{Cfx}+C_d\sum_{i=1,2}\Delta u_{Cdi}i_{Cdi}\le 0 \quad (25)$$

where i_{Cfx} is the current through the FC C_{fx} and i_{Cdi} is the current through the DC-link capacitor C_{di}. Assuming that the DC bus voltage is clamped at 4E by DC source, thus:

$$\Delta u_{Cdc1}+\Delta u_{Cdc2}=0 \quad (26)$$

Further, the relationship between i_{Cd1} and i_{Cd2} is:

$$i_m=i_{Cd1}-i_{Cd2} \quad (27)$$

Based on Equations (26) and (27), Equation (25) is simplified as:

$$\frac{dJ}{dt}=C_f\sum_{x=a,b,c}\Delta u_{Cfx}i_{Cfx}+C_d\Delta u_{Cd1}i_m\le 0 \quad (28)$$

Assuming that the capacitor voltages and phase currents can remain constant during one carrier period T_s, the average value of operator (28) over one T_s is deduced as:

$$C_f\sum_{x=a,b,c}\Delta u_{Cfx}\left(\frac{1}{T_s}\int_{kT_s}^{(k+1)T_s}i_{Cfx}dt\right)+C_{dc}\Delta u_{Cd1}\left(\frac{1}{T_s}\int_{kT_s}^{(k+1)T_s}i_m dt\right)\le 0$$
$$\Rightarrow C_f\sum_{x=a,b,c}\Delta u_{Cfx}\bar{i}_{Cfx}+C_{dc}\Delta u_{Cd1}\bar{i}_m\le 0 \quad (29)$$

In practice, $\bar{i}_{Cfx}$ and $\bar{i}_m$ are acquired through the duty cycle and their relationship with phase current in a specific output voltage, as shown in Table II. In the case shown in Fig. 6(a), $\bar{i}_{Cfa}=0$, $\bar{i}_{Cfb}=i_b\cdot T_1/T_s$, $\bar{i}_{Cfc}=-i_c\cdot(T_1+T_3)/T_s$, and $\bar{i}_m=i_b\cdot(T_2+T_3)/T_s$. As shown in Table III, more than one vector sequences could be used to constitute a voltage vector. The vector sequences that minimize the function of Equation (29) would be the best vector sequences.

V. Simulation Results

A simulation platform is developed to evaluate the performance of the five-level converter under the proposed modulation strategy. In the proposed strategy, SVM is used to inject common-mode voltages to the reference voltage to suppress the voltage-drift phenomenon. The PD-PWM technique is then employed to control the proposed converter to output the expected voltages, which contain the reference voltages and the injected common-mode voltages. In the simulation platform, the S-Function model is used to realize the control system in discrete time domain. The DC side of the converter is supplied by a constant DC source. By contrast, the AC side of the converter is connected to a three-phase symmetrical RL load. The system parameters are given in Table IV.

TABLE IV
Parameters of the Converter in Simulation

Converter Parameters	Values
AC-side Current i_o	50 A
DC-link Voltage u_{dc}	1200 V
DC Capacitor C_{dc}	1000 μF
FC C_f	1000 μF
Carrier Frequency f_c	10 kHz
Fundamental Frequency f_o	50 Hz

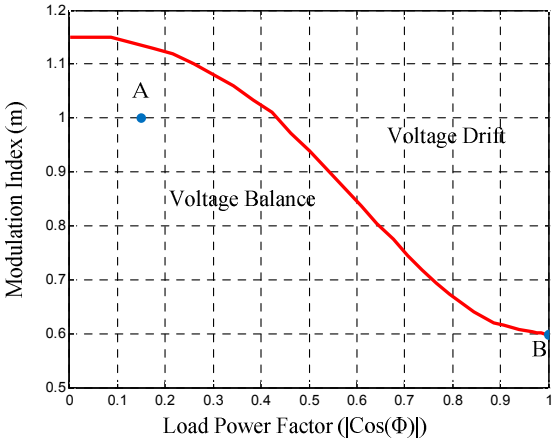

Fig. 8. Limits of the voltage balance for the proposed converter with proposed modulation strategy. A – Operating point corresponding to Figs. 10 and 14. B – Operating point corresponding to Figs. 11 and 15.

A. Limits of Operation

Similar to 5L-NPC, the strategy, which minimizes the differential of the cost function (dJ/dt) to mitigate the voltage-drift phenomenon, cannot guarantee the capacitor voltage under all possible operating conditions without auxiliary circuits. Fig. 8 shows the boundary under which the proposed modulation strategy can control and achieve balanced capacitor voltages. By injecting a common voltage, the modulation index *m* could expand to 1.15, as shown in Fig. 8. This condition is an advantage of SVM for improved DC-voltage utilization. The solid line shows the boundary of the proposed converter. The boundary is depicted by simulation results at various modulation indices and load power factor values.

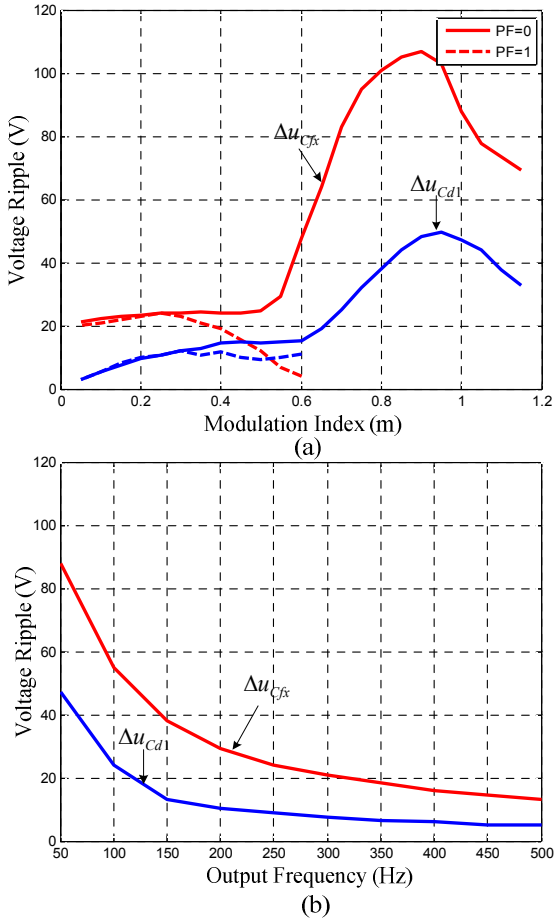

Fig. 9. Voltage ripples of flying and DC-link capacitors when i_o=50 A: (a) modulation index varies when f_o=50 Hz; (b) output frequency varies when m=1 and PF=1

B. Voltage Ripples of DC-Link and FCs

In specific operation conditions, the voltage ripples of DC-link and FCs are depicted in Fig. 9. As shown in Fig. 9(a), the voltage ripples are changed as the modulation index varies. The DC-link capacitor voltage ripple is smaller than the FC voltage ripple under the same conditions. When PF=1 and m>0.6, the voltage ripples are not described, as the voltage-drift phenomenon cannot be suppressed. If PF=0, the voltage ripples become larger when m>0.6. As shown in Fig. 9(a), Δu_{Cfx} is larger than 100 V when PF=0 and m=1. If the maximum capacitor ripple was specified to 7.5% of the DC-link voltage [34], a larger capacitor is necessary to reduce the voltage ripples in the operation conditions. In addition, a higher output frequency is helpful to decrease the voltage ripples, as shown in Fig. 9(b). If the output frequency is 250 Hz, Δu_{Cfx} is about 24 V when switching frequency is maintained at 10 kHz. Combined with the performance of the proposed converter, as shown in Figs. 8 and 9, the converter is suitable for handling high frequency reactive power. This finding is consistent with applications of the active power filter, which mainly deals with the fifth and seventh reactive harmonics.

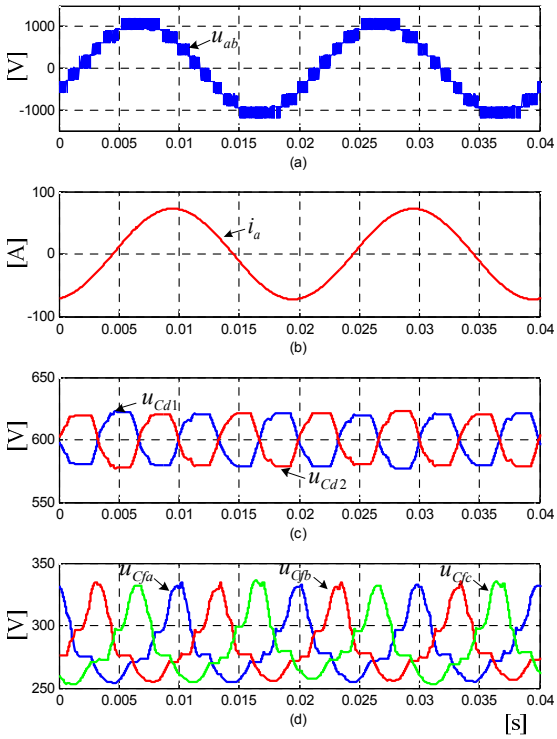

Fig. 10. Simulation results when m=1 and PF=0.16 (L=26.7mH, R=1.36Ω): (a) line voltage u_{ab}, (b) phase current i_a, (c) DC-link-capacitor voltages u_{Cd1} and u_{Cd2}, (d) FC voltages u_{Cfa}, u_{Cfb}, and u_{Cfc}.

C. Simulation Results in Different RL load

Fig. 10 shows the simulation waveforms of the proposed converter at a power factor of PF=0.16 and a modulation index of m=1. Figs. 10(a) to (d) shows the line voltage u_{ab}, phase-a current i_a, DC-link capacitor voltages, and FC voltages, respectively.

In this condition, the voltages of DC-link and FCs remain stable at their nominal values. Fig. 11 shows that the DC-link and FCs voltages remain balanced at PF=1 and m=0.6. The waveforms in Figs. 10 and 11 are consistent with the conclusion in Fig. 8. For high modulation index m, the line voltage has nine distinct levels. Correspondingly, in a lower modulation index, the line voltage has smaller distinct levels, i.e., m=0.6 has seven distinct levels. Compared with Figs. 10 and 11, the voltages of DC-link and FCs have smaller ripples when m=0.6, as the SVM strategy has more optional vector sequences to suppress the voltage deviation.

VI. Experimental Results

A low power three-phase five-level converter has been constructed to verify the validity of the proposed converter and modulation strategy. The prototype of the experimental platform is shown in Fig. 12. Each phase board contains a 1000 μF FC, six IGBTs and their relative gate drivers, a FC voltage

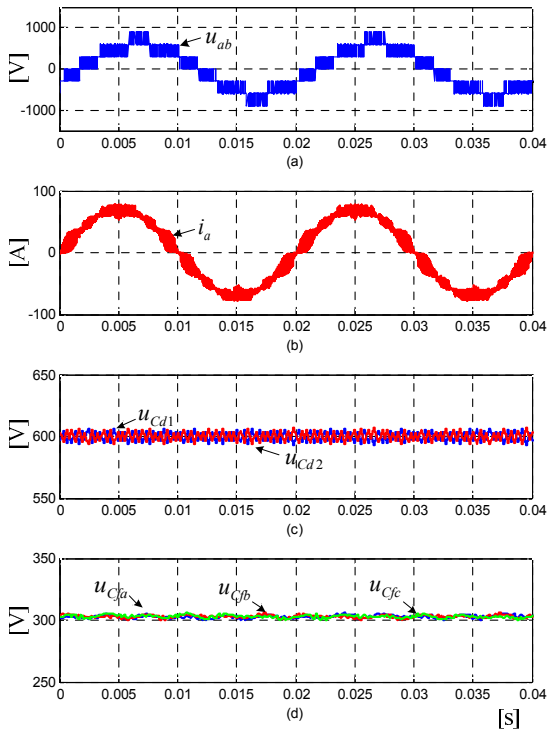

Fig. 11. Simulation results when m=0.6 and PF≈1 (L=100μH, R=5.09Ω): (a) line voltage u_{ab}, (b) Phase A current i_a, (c) DC-link-capacitor voltages u_{Cd1} and u_{Cd2}, (d) flying capacitor voltages u_{Cfa}, u_{Cfb}, and u_{Cfc}.

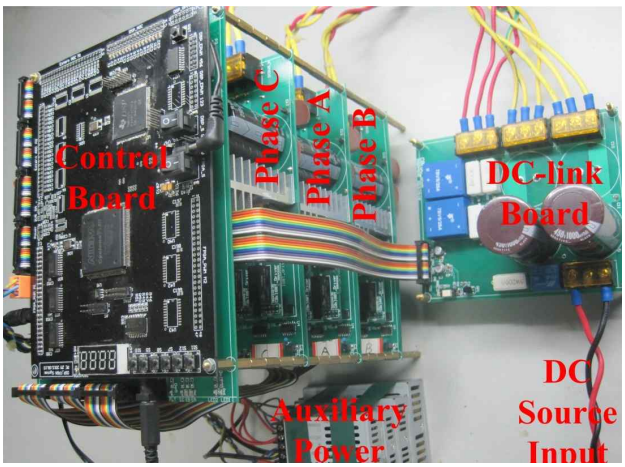

Fig. 12. Prototype of the proposed three-phase five-level hybrid-clamped converter.

sampling circuit, and a phase current sampling circuit. The DC-bus board includes two 1000 μF series capacitors, two DC-capacitor voltage sampling circuits, and a precharge circuit composed of precharge resistors and a bypass contactor. The controller is based on a DSP TMS320F28335 and a FPGA EP3C25Q240C8. In this section, the DC-link voltage is approximately 100 V supplied by a DC source, and the switching frequency is 10 kHz.

A. Precharge Process

A special precharge method has been developed to precharge the FCs without additional equipment. As shown in Fig. 13, the proposed precharge process can be divided into three steps:

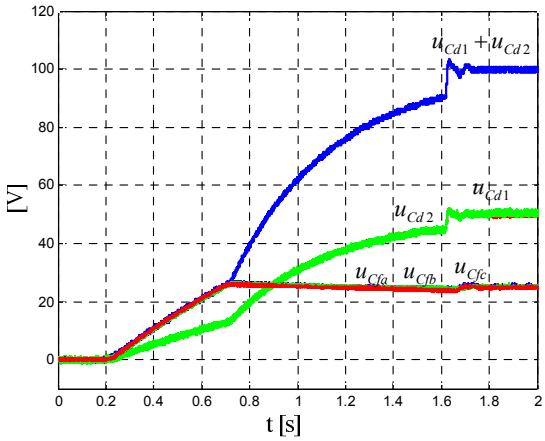

Fig. 13. Waveforms of DC-link and FC voltages during the precharge process.

(1) S1 and S2 (see Figure 1) of each phase leg are turned on at 0.2 second. Thus, these FCs are parallel to and charged together with the DC-link capacitor through precharge resistors. If the FC voltage of each phase is equal to its nominal value of 25 V, the relative S1 and S2 are turned off. In the process, the charging time is affected by total capacitors and precharge resistors.

(2) The DC-link capacitors continue to be charged through precharge resistors until the sum of two DC-capacitor voltages is close to the DC source voltage, i.e., 90 V. In this period, the charging process is much faster as the smaller remaining capacitors.

(3) At 1.62 seconds, the bypass contactor is turned on. Two DC-link capacitors are quickly charged to their nominal value of 50 V.

B. Experimental Results in Different RL load

Fig. 14 shows the experimental waveforms of the proposed converter at a power factor of PF=0.16 and a modulation index of m=1. As shown in Fig. 14, DC-link and FC voltages remain stable at their nominal values. Figure 15 shows that the DC-link and FCs voltages remain balanced at PF=1 and m=0.6. The experimental results and simulation results are mainly consistent. In Figs. 14(a) and 15(a), some unwanted voltage glitches were caused by the switches between different vector sequences to suppress the voltage-drift phenomenon.

VII. CONCLUSIONS

A novel five-level three-phase hybrid-clamped converter is introduced in this paper. The converter is composed of only six switches and one FC per phase. The main advantage of the converter is that it consists less components compared with other five-level converters, as shown in Table I. The proposed converter helps to improve reliability, reduce costs and

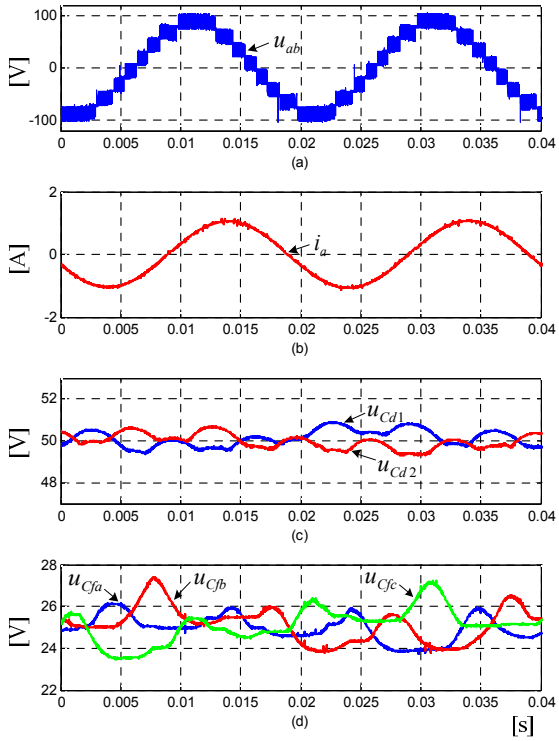

Fig. 14. Experimental results when m=1 and PF=0.16 (L=141mH, R=7.18Ω): (a) line voltage u_{ab}, (b) Phase A current i_a, (c) DC-link-capacitor voltages u_{Cd1} and u_{Cd2}, (d) FC voltages u_{Cfa}, u_{Cfb}, and u_{Cfc}.

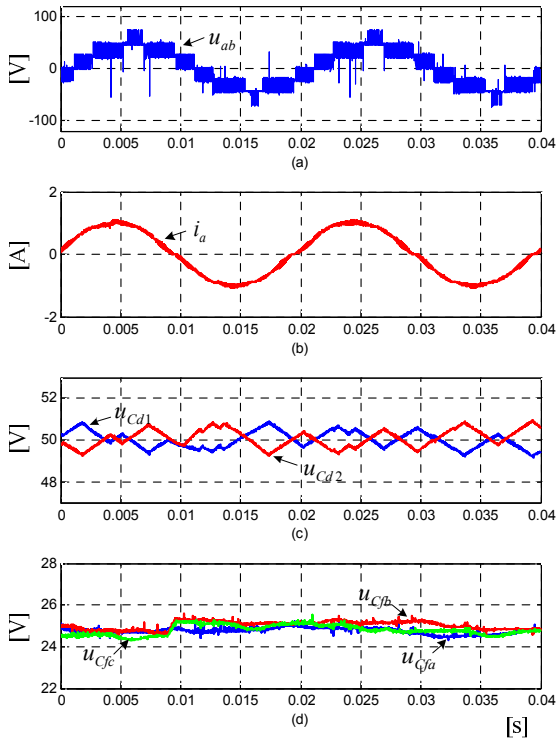

Fig. 15. Experimental results when m=0.6 and PF≈1 (L=2mH, R=25Ω): (a) line voltage u_{ab}, (b) phase-a current i_a, (c) DC-link-capacitor voltages u_{Cd1} and u_{Cd2}, (d) FC voltages u_{Cfa}, u_{Cfb} and u_{Cfc}.

conduction losses, and is attractive for low-voltage applications. However, the converter cannot keep the voltage of DC-link and FCs balanced under SPWM. Thus, a specific modulation strategy based SVM is developed to balance the voltage by injecting a common-mode voltage. Simulation and experimental results conclude that the introduced modulation strategy is capable of balancing the voltages of DC-link and FCs within specified operating ranges. Based on the aforementioned analysis, the proposed converter is suitable for handling high frequency reactive power, such as the active power filter. This study further presents a startup method that charges DC-link and FCs without any additional circuits. Experimental results confirm the feasibility of the precharge method.

ACKNOWLEDGMENT

This research is sponsored by Zhejiang Key Science and Technology Innovation Group Program (2010R50021), and National Natural Science Foundation of China under grant (51177148).

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L.G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.

[2] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6, pp. 2930-2945, Dec. 2007.

[3] C. A. Silva, L. A. Cordova, P. Lezana, and L. Empringham, "Implementation and control of a hybrid multilevel converter with floating dc links for current waveform improvement," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 6, pp. 2304-2312, Jun. 2011.

[4] B. A. Welchko, M. B. R. Correa, and T. A. Lipo, "A three-level MOSFET inverter for low-power drives," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 3, pp. 669-674, Jun. 2004.

[5] R.Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Trans. Ind. Appl.*, Vol. 41, No. 3, pp. 855-865, May/Jun. 2005.

[6] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, Vol. 28, No. 2, pp. 899-907, Feb. 2013.

[7] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 12, pp. 5515-5527, Dec. 2013.

[8] J. Ebrahimi, E. Babaei, and G. B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 2, pp. 655-667, Feb. 2012.

[9] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Trans. Ind. Appl.*, Vol. 41, No. 2, pp. 655-664, Mar./Apr. 2005.

[10] Z. Shu, X. He, Z. Wang, D. Qiu, and Y. Jing, "Voltage balancing approaches for diode-clamped multilevel

converters using auxiliary capacitor-based circuits," *IEEE Trans. Power Electron.,* Vol. 28, No. 5, pp. 2111-2124, May 2013.
[11] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, Vol. IA-17, No. 5, pp. 518-523, Sep./OCT. 1981.
[12] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Proc. IEEE 23rd Power Electron. Spec. Conf.,* Vol. 1, pp. 397-403, 1992.
[13] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non conventional power converter for plasma stabilization," in *Proc. IEEE 19th Power Electron. Spec. Conf.,* Apr. 11-14, 1988, Vol. 1, pp.122-129.
[14] J. Pou, R. Pindado, and D. Boroyevich, "Voltage-balance limits in four-level diode-clamped converters with passive front ends," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 1, pp. 190-196, Feb. 2005.
[15] M. Saeedifard, R. Iravani, and J. Pou, "Analysis and control of dc-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6, pp. 3255-3266, Dec. 2007
[16] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Trans. Power Electron.,* Vol. 23, No. 4, pp. 1751-1758, Jul. 2008.
[17] K. Wang, Z. Zheng, Y. Li, K. Liu, and J. Shang, "Neutral-point potential balancing of a five-level active neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 1907-1918, May 2013.
[18] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters – State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp. 2581-2596, Aug. 2010.
[19] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: unified analysis and design considerations," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 2, pp. 1092-1104, Apr. 2007.
[20] M. Zygmanowski, J. Michalak, B. Grzesik, "DC-link voltage balancing method for a hybrid asymmetric multilevel converter," in *Proc. 15th Eur. Conf. on Power Electronics and Applications (EPE),* 2013.
[21] G. Tan, Q. Deng, and Z. Liu, "An optimized SVPWM strategy for five-level active NPC (5L-ANPC) converter," *IEEE Trans. Power Electron.,* Vol. 29, No. 1, pp. 386-395, Jan. 2014.
[22] S. R. Pulikanti, G. S. Konstantinou, and V. G. Agelidis, "Generalisation of flying capacitor-based active-neutral-point-clamped multilevel converter using voltage-level modulation," *IET Power Electron.,* Vol. 5, No. 4, pp. 456-466, Apr. 2012.
[23] S. R. Pulikanti and V. G. Agelidis, "Hybrid flying-capacitor-based active-neutral-point-clamped five-level converter operated with SHE-PWM," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 10, pp. 4643-4653, Oct. 2011
[24] T. B. Soeiro and J. W. Kolar, "The new high-efficiency hybrid neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 1919-1935, May 2013.
[25] A. M. Y. M. Ghias, J. Pou, V. G. Agelidis, and M. Ciobotaru, "Initial capacitor charging in grid-connected flying capacitor multilevel converters," *IEEE Trans. Power Electron.,* Vol. 29, No. 7, pp. 3245-3249, Jul. 2014.
[26] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, and N. Celanovic, "Active neutral-point-clamped multilevel converters," in *Proc. IEEE 36th Power Electron. Spec. Conf.,* Vol. 1, pp. 2296-2301, 2005.
[27] J.-I. Itoh, Y. Noge, and T. Adachi, "A novel five-level three-phase PWM rectifier with reduced switch count," *IEEE Trans. Power Electron.,* Vol. 26, No. 8, pp. 2221-2228, Aug. 2011.
[28] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.,* Vol. 7, No. 3, pp. 497-505, Jul. 1992.
[29] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.
[30] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, Vol. 37, No. 2, pp. 637-641, Mar./Apr. 2001.
[31] B. Kaku, I. Miyashita, and S. Sone, "Switching loss minimised space vector PWM method for IGBT three-level inverter," in *Proc. Inst. Elect. Eng.-Elect. Power Appl.*, Vol. 144, pp. 182-190, 1997.
[32] C. Yan, C. Sun, Y. Zhang, M. Chen, and D. Xu, "A hybrid PWM modulation scheme for PV inverter," *Future Energy Electronics Conference (IFEEC),* Vol. 1, pp. 406-410, 2013.
[33] M. Saeedifard, P. M. Barbosa, and P. K. Steimer, "Operation and control of a hybrid seven-level converter," *IEEE Trans. Power Electron.,* Vol. 27, No. 2, pp. 652-660, Feb. 2012.
[34] D. Krug, S. Berten, S. S. Fazel, K. Jalili, and M. Malinowski, "Operation and control of a hybrid seven-level converter," *IEEE Trans. Power Electron.,* Vol. 27, No. 2, pp. 652-660, Feb. 2012.

Bin Chen was born in Quzhou, Zhejiang Province, China, in 1988. He received his B.S. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2010, where he is currently working toward a Ph.D. degree in Electrical Engineering. His present research interests are in the areas of speed-sensorless induction motor drives, multilevel converters, and digital-signal-processor-based real-time control.

Wenxi Yao was born in Haining, Zhejiang Province, China, in 1977. He received his B.S. and Ph.D. degrees in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2000 and 2006, respectively. He is currently an Associate professor of Electrical Engineering at Zhejiang University. From 2010 to 2011, he was a visiting scholar at FREEDM, North Carolina State University. His research interests include digital control in power electrics and sensorless control of AC motor drives. He has authored and coauthored more than 50 published technical papers.

Zhengyu Lu received his B.S. degree in industrial automatic control from Ohai University, China, in 1982 and Ph.D. degree in power electronics from Zhejiang University, China, in 1987. From 1996 to 1998, he was a visiting scholar and worked as a researcher at the University of Birmingham and Imperial College, UK. He is currently a professor at Zhejiang University and is the director of China National Power Electronics Laboratory. Since 1982, he has been teaching and conducting research on power electronic devices and power converters at Zhejiang University, China. His main research interests include power converter, electrical track, vehicle electronics, electronics in FACTS application, and power electronics system integration.