JPE 14-6-11

http://dx.doi.org/10.6113/JPE.2014.14.6.1178
ISSN(Print): 1598-2092/ISSN(Online): 2093-4718

Finite State Model-based Predictive Current Control with Two-step Horizon for Four-leg NPC Converters

Venkata Yaramasu[*], Marco Rivera[†], Mehdi Narimani[*], Bin Wu[*], and Jose Rodriguez[**]

[*]Department of Electrical and Computer Engineering, Ryerson University, Toronto, Canada
[†]Department of Industrial Technologies, Universidad de Talca, Curico, Chile
[**]Electronics Engineering Department, Universidad Tecnica Federico Santa Maria, Valparaiso, Chile

Abstract

This study proposes a finite-state model predictive controller to regulate the load current and balance the DC-link capacitor voltages of a four-leg neutral-point-clamped converter. The discrete-time model of the converter, DC-link, inductive filter, and load is used to predict the future behavior of the load currents and the DC-link capacitor voltages for all possible switching states. The switching state that minimizes the cost function is selected and directly applied to the converter. The cost function is defined to minimize the error between the predicted load currents and their references, as well as to balance the DC-link capacitor voltages. Moreover, the current regulation performance is improved by using a two-step prediction horizon. The feasibility of the proposed predictive control scheme for different references and loads is verified through real-time implementation on the basis of dSPACEDS1103.

Key words: Current control, DC–AC power conversion, DC-link capacitor voltage balancing, Digital control, Discrete-time signals, Distributed generation, Finite control set model predictive control, Four-leg converters, Multilevel converters

NOMENCLATURE

$\underline{\mathbf{v_{dc}}}$	DC-link voltage	$[\underline{v_{c1}} \quad \underline{v_{c2}}]^T$
$\underline{\mathbf{v}}$	Converter voltage	$[\underline{v_{an}} \quad \underline{v_{bn}} \quad \underline{v_{cn}}]^T$
$\underline{\mathbf{i}}$	Load (output) current	$[\underline{i_a} \quad \underline{i_b} \quad \underline{i_c}]^T$
$\underline{\mathbf{i}}^*$	Reference load current	$[\underline{i_a^*} \quad \underline{i_b^*} \quad \underline{i_c^*}]^T$
$\mathbf{C_{dc}}$	DC-link capacitance	$[C_1 \quad C_2]^T$
L_f	Filter inductance	$[L_{fa} \quad L_{fb} \quad L_{fc}]^T$
R_f	Filter leakage resistance	$[R_{fa} \quad R_{fb} \quad R_{fc}]^T$
R	Load resistance	$[R_a \quad R_b \quad R_c]^T$
L_n, R_n	Neutral inductance and its leakage resistance	
L_{nl}, R_{nl}	Non-linear load inductance and resistance	
T_s	Sampling time	
N	Prediction horizon	
$\underline{x}$	Time-varying quantity	

Manuscript received May 8, 2014; accepted Oct. 6, 2014
Recommended for publication by Associate Editor Seung-Ki Sul.
[†]CorrespondingAuthor:marcoriv@utalca.cl
Tel: +56 9 95442860,Universidad de Talca
[*]Department of Electrical and Computer Engineering, Ryerson University, Canada
[**]Electronics Engineering Department, Universidad Tecnica Federico Santa Maria, Chile

I. INTRODUCTION

Imbalanced and non-linear loads cause a large amount of neutral current in three-phase four-wire systems. Hence, conventional three-leg, three-phase power converters are unsuitable for such applications. Correspondingly, four-leg converters provide the best path for neutral currents [1]-[3]. Many applications, including distributed generation, universal power quality conditioners, electric drives, shunt active power filters, and active front-end rectifiers, that utilize four-leg converters require precise current control [4]-[8].

Multilevel diode-clamped converters reach high power levels with reduced common mode voltages, total harmonic distortion, and electromagnetic interference [9]. Hence, these converters are highly suitable for medium-voltage, high-power applications. Moreover, diode-clamped converters employ clamping diodes and cascaded DC capacitors to produce AC voltage waveforms with multiple levels [10]. Three-level diode-clamped converters commonly known as neutral-point-clamped (NPC) converters are used in numerous high-power, medium-voltage industrial applications [11]. These four-leg NPC converters provide a promising topology in four-wire, medium-voltage systems, as well as offer full utilization of DC-link voltage and less stress

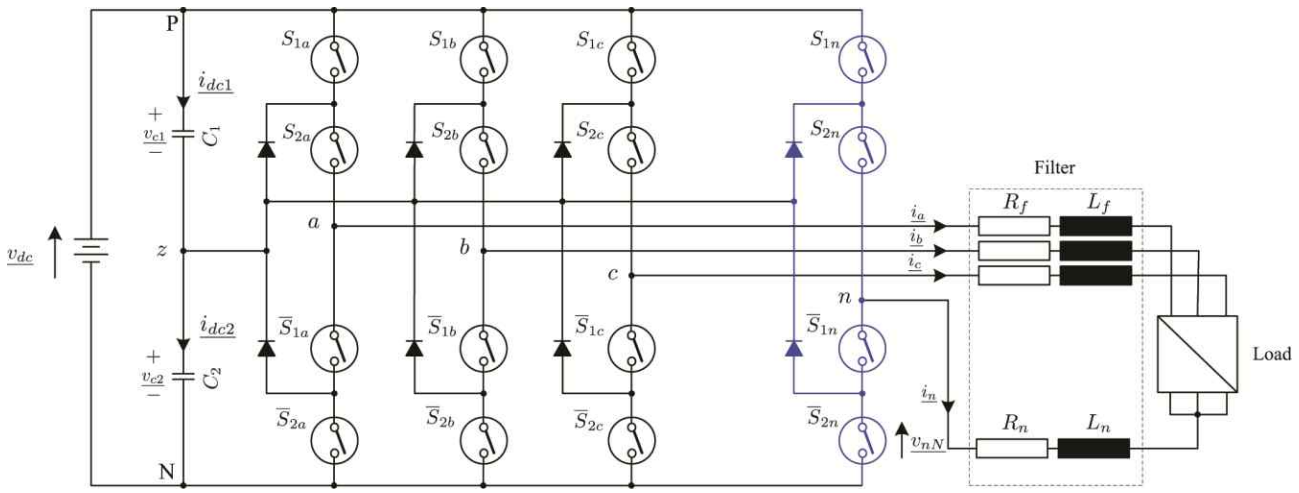

Fig. 1. Topology of the four-leg NPC converter with arbitrary load.

on the DC-link capacitors [12], [13]. Both carrier-based and three-dimensional space vector modulations are available for four-leg converters [12]-[18].

The finite-state or finite control set model predictive control (FCS-MPC) is a simple, intuitive, and powerful class of receding horizon control algorithm [19] controlling power converters with diverse and complex control challenges and restrictions [20], [21]. The tool is a true model-based optimization control strategy involving a large number of calculations [22]-[24]. Accordingly, available digital implementation platforms, such as microprocessors, digital signal processors, and field-programmable gate arrays, can handle such computations. Recent scholarly works demonstrate the easy application of the FCS-MPC in various power converters [25]-[34].

This study proposes an FCS-MPC to regulate the load currents while minimizing the imbalance between the DC-link capacitor voltages in a four-leg NPC converter. These objectives are expressed as a cost function. The future values of the control variables for each possible switching state of the converter are predicted using the discrete-time model of the system. The switching state that minimizes the cost function and meets the control goals is then selected and applied to the converter. Variable prediction is conducted over one or more sample periods. The one-step prediction horizon provides simplified analysis and computational cost, such that is widely applied in FCS-MPC works on power converters [25], [30]-[32]. Refs. [35] and [36] used simulations to demonstrate the control performance improvement under a prediction horizon of more than one step. However, Ref. [37] has reported that its feasibility is only verified by real-time implementation for three-phase converters, but not for four-leg converters. This study uses the concept of two-step prediction to improve the regulation of load currents for different reference and load conditions. The experimental results are presented using the dSPACE DS1103 rapid prototyping real-time implementation platform to validate the feasibility of the proposed control method.

The remainder of this paper is organized as follows: Section II presents the mathematical model of the converter. Section III explains the proposed control strategy. Section IV discusses the experimental results. Section V draws the conclusions.

II. Four-Leg NPC Converter Topology

A three-phase, four-leg NPC converter with an output *L* filter is shown in Fig. 1. This converter presents a connection format similar to that of the conventional three-phase NPC converter, albeit with an additional leg connected to the neutral point of the load. The converter is composed of 16 active switches and 8 clamping diodes. The switching states and the corresponding converter terminal voltages are shown in Table I. The table shows that (a) only two switches are conducted at any time and (b) switch pairs $(S_{1x}, \overline{S}_{1x})$ and $(S_{2x}, \overline{S}_{2x})$ operate in a complementary manner [10]. A total of 81 (3^4) switching combinations are available for this converter.

The voltage in any phase-*x* of the converter measured from the negative point of the DC-link (*N*) is expressed in terms of switching states and DC-link capacitor voltages as follows (Table I):

$$\begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \\ v_{nN} \end{bmatrix} = v_{c1} \begin{bmatrix} S_{1a} \\ S_{1b} \\ S_{1c} \\ S_{1n} \end{bmatrix} + v_{c2} \begin{bmatrix} S_{2a} \\ S_{2b} \\ S_{2c} \\ S_{2n} \end{bmatrix} \tag{1}$$

The preceding converter voltages are expressed with respect to the mid-point (*n*) of the neutral leg as follows:

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} v_{aN} - v_{nN} \\ v_{bN} - v_{nN} \\ v_{cN} - v_{nN} \end{bmatrix} \tag{2}$$

TABLE I
SWITCHING STATES AND CONVERTER TERMINAL VOLTAGES
($x = a, b, c, n$)

S_x	S_{1x}	S_{2x}	$\overline{S}_{1x}$	$\overline{S}_{2x}$	v_{xN}
1	1	1	0	0	$\underline{v_{c1}} + \underline{v_{c2}}$
0	0	1	1	0	$\underline{v_{c2}}$
−1	0	0	1	1	0

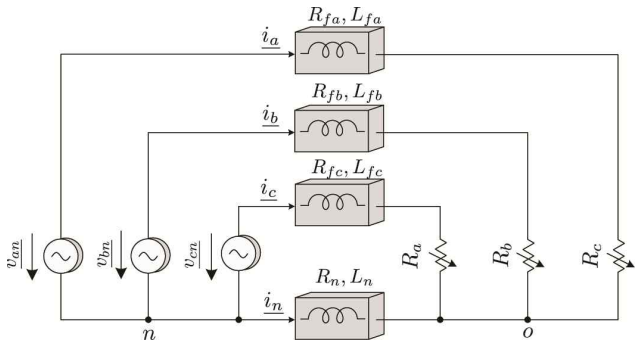

Fig. 2. Representation of L filter and load connected to the four-leg NPC converter.

By solving Eqs. (1) and (2), the load voltages are expressed in terms of switching states and DC-link capacitor voltages as follows:

$$\begin{bmatrix} \underline{v_{an}} \\ \underline{v_{bn}} \\ \underline{v_{cn}} \end{bmatrix} = \underline{v_{c1}} \begin{bmatrix} S_{1a} - S_{1n} \\ S_{1b} - S_{1n} \\ S_{1c} - S_{1n} \end{bmatrix} + \underline{v_{c2}} \begin{bmatrix} S_{2a} - S_{2n} \\ S_{2b} - S_{2n} \\ S_{2c} - S_{2n} \end{bmatrix} \quad (3)$$

The equivalent circuit of the four-leg NPC converter with an output L filter is shown in Fig. 2.The variables in the figure are defined in the Nomenclature section. Subscripts a, b, and c represent the three phases. n and o represent the converter and load neutrals, respectively. By applying Kirchhoff's voltage law in Fig. 2, the converter AC side voltages are expressed in terms of load voltages, load currents, and load neutral current as follows:

$$\begin{bmatrix} \underline{v_{an}} \\ \underline{v_{bn}} \\ \underline{v_{cn}} \end{bmatrix} = R_f \begin{bmatrix} \underline{i_a} \\ \underline{i_b} \\ \underline{i_c} \end{bmatrix} + L_f \frac{d}{dt} \begin{bmatrix} \underline{i_a} \\ \underline{i_b} \\ \underline{i_c} \end{bmatrix} + \begin{bmatrix} R_a & 0 & 0 \\ 0 & R_b & 0 \\ 0 & 0 & R_c \end{bmatrix} \begin{bmatrix} \underline{i_a} \\ \underline{i_b} \\ \underline{i_c} \end{bmatrix} - R_n \underline{i_n} - L_n \frac{d}{dt} \underline{i_n} \quad (4)$$

where $R_f = R_{fa} = R_{fb} = R_{fc}$ and $L_f = L_{fa} = L_{fb} = L_{fc}$.

The relationship between the load currents and the load neutral current is obtained as follows:

$$\underline{i_n} = -\left(\underline{i_a} + \underline{i_b} + \underline{i_c}\right) \quad (5)$$

By substituting Eq. (5) into Eq. (4), the converter AC side voltages can be expressed independent of the load neutral current as follows:

$$\begin{bmatrix} \underline{v_{an}} \\ \underline{v_{bn}} \\ \underline{v_{cn}} \end{bmatrix} = R_{eq} \begin{bmatrix} \underline{i_a} \\ \underline{i_b} \\ \underline{i_c} \end{bmatrix} + L_{eq} \frac{d}{dt} \begin{bmatrix} \underline{i_a} \\ \underline{i_b} \\ \underline{i_c} \end{bmatrix} \quad (6)$$

Where

$$R_{eq} = \begin{bmatrix} R_f + R_n + R_a & 0 & 0 \\ 0 & R_f + R_n + R_b & 0 \\ 0 & 0 & R_f + R_n + R_c \end{bmatrix}$$

$$L_{eq} = \begin{bmatrix} L_f + L_n & L_n & L_n \\ L_n & L_f + L_n & L_n \\ L_n & L_n & L_f + L_n \end{bmatrix}.$$

The differential load currents from Eq. (6)are expressed as follows:

$$\frac{d}{dt} \begin{bmatrix} \underline{i_a} \\ \underline{i_b} \\ \underline{i_c} \end{bmatrix} = -L_{eq}^{-1} R_{eq} \begin{bmatrix} \underline{i_a} \\ \underline{i_b} \\ \underline{i_c} \end{bmatrix} + L_{eq}^{-1} \begin{bmatrix} \underline{v_{an}} \\ \underline{v_{bn}} \\ \underline{v_{cn}} \end{bmatrix} \quad (7)$$

The DC-link capacitor voltages are expressed in terms of DC-link capacitor currents as follows:

$$\left.\begin{aligned} \frac{d}{dt}\underline{v_{c1}} &= \frac{1}{C_1}\underline{i_{dc1}} \\ \frac{d}{dt}\underline{v_{c2}} &= \frac{1}{C_2}\underline{i_{dc2}} \end{aligned}\right\} \quad (8)$$

The capacitor currents (i.e., $\underline{i_{dc1}}$ and $\underline{i_{dc2}}$) are estimate during the three-phase load currents (i.e., $\underline{i_a}$, $\underline{i_b}$, and $\underline{i_c}$) and the converter switching states as follows:

$$\left.\begin{aligned} \underline{i_{dc1}} &= K_a.\underline{i_a} + K_b.\underline{i_b} + K_c.\underline{i_c} \\ \underline{i_{dc2}} &= Q_a.\underline{i_a} + Q_b.\underline{i_b} + Q_c.\underline{i_c} \end{aligned}\right\} \quad (9)$$

where $K_x$and $Q_x$depend on the voltage levels, such that

$$\left.\begin{aligned} K_x &= sgn\{S_n - 1\} - sgn\{S_x - 1\} \\ Q_x &= sgn\{S_n + 1\} - sgn\{S_x + 1\} \end{aligned}\right\} \quad (10)$$

where S_n and $S_x$correspond to the neutral and phase levels, respectively. sgn is the argument sign with a value corresponding to 0, 1, or −1.

Based on Eqs. (7) and (9), the load currents and the DC-link capacitor voltages are related to the switching states. Moreover, they are controlled by choosing a proper switching state.

III. FINITE-STATES MODEL PREDICTIVE CONTROL

A. Control Strategy

The proposed predictive control aims to regulate the load currents and balance the DC-link capacitor voltages (Fig. 3). The proposed FCS-MPC uses the discrete-model of the system, current state (k) load currents, DC-link capacitor voltages, and 81 switching states to predict the future behavior of the control variables.

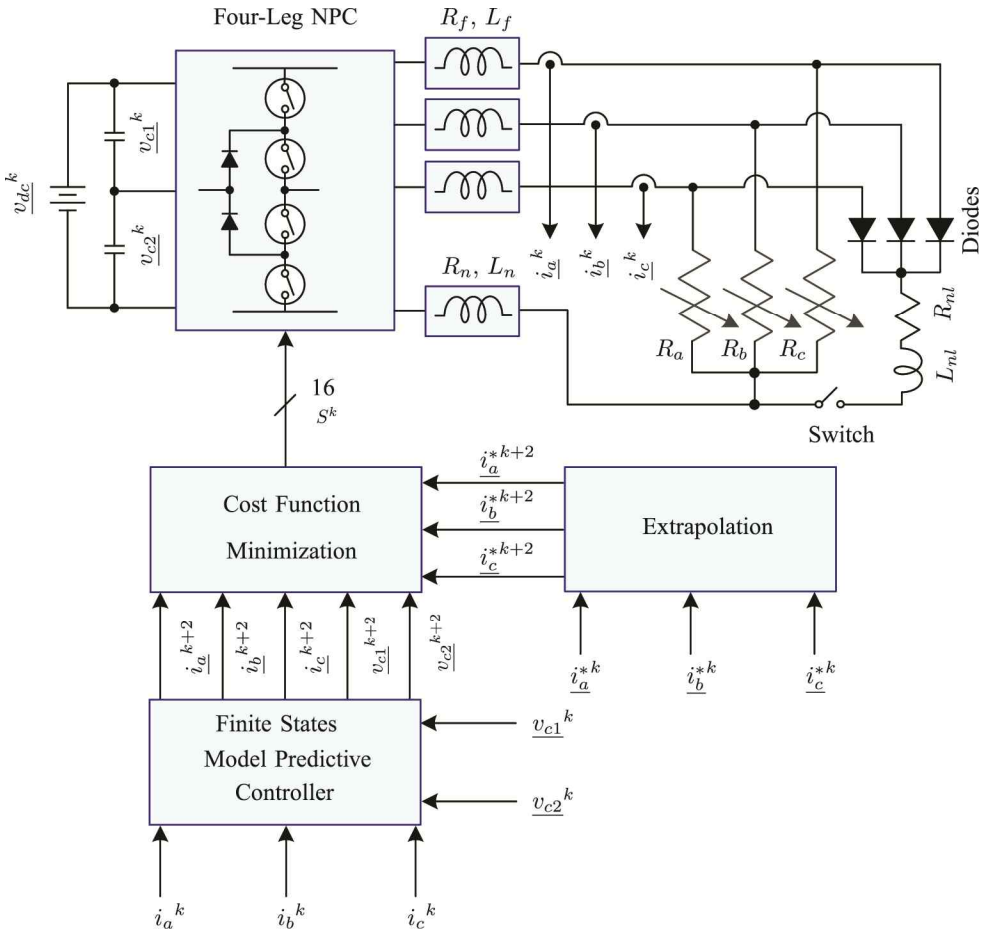

Fig. 3. Proposed FCS-MPC control scheme for a four-leg NPC converter.

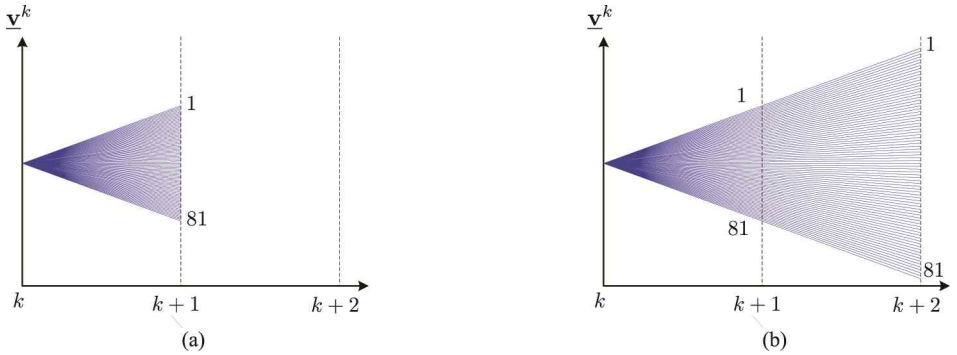

Fig. 4. Control variable prediction for a four-leg NPC converter. (a) One-step prediction. (b) Modified two-step prediction.

A cost function is utilized to evaluate the predictions. The switching state leading to the minimal value of the cost function is chosen and directly applied to the converter. The proposed FCS-MPC does not require linear current regulators (i.e., PI controllers) and modulation.

The 81 switching states at sampling time k are used to predict the converter voltage $\underline{\mathbf{v}}^k$ for the one-step prediction horizon, as shown in Fig. 4(a). The number of feasible switching states becomes $81^2 = 6561$ for a prediction horizon of $N = 2$. This value provides optimal performance [38]-[40] but greater computational burden. A modified two-step prediction is used to reduce the switching changes (i.e., switching frequency) and the computational burden caused by 6561, as shown in Fig. 4(b).

This approach uses 81 switching states projected to the sampling time $k + 2$. Subsequently, the state variables achieve 81 possible conditions. The algorithm calculates all these conditions in the future sample $k + 2$. The control strategy chooses a switching state in the sampling instant k, which minimizes the cost function in the $k + 2$ sampling instant.

The system applies this switching state during the next sampling period.

B. Cost Function Design

The defined cost function has two objectives: (a) minimize the error between the predicted load currents $\underline{\mathbf{i}}^{k+2}$ and theirreferences $\underline{\mathbf{i}}^{*k+2}$ and (b) balance the DC-link capacitor voltages. These control objectives are represented as follows:

$$g_{track}{}^{k+2} = \left[\underline{i_a^*}^{k+2} - \underline{i_a}^{k+2}\right]^2 + \left[\underline{i_b^*}^{k+2} - \underline{i_b}^{k+2}\right]^2 + \left[\underline{i_c^*}^{k+2} - \underline{i_c}^{k+2}\right]^2$$
$$g_{bal}{}^{k+2} = \lambda_{dc}\left[\underline{v_{c1}}^{k+2} - \underline{v_{c2}}^{k+2}\right]^2 \quad (11)$$

where $\lambda_{dc}$is the weighting factor adjusted according to the desired performance.

The future reference currents are obtained by fourth-order Lagrange extrapolation using present and past current references. This process is demonstrated as follows [41]:

$$\underline{i}^{*k+2} = 10\,\underline{i}^{*k} - 20\,\underline{i}^{*k-1} + 15\,\underline{i}^{*k-2} - \underline{i}^{*k-3} \quad (12)$$

The final cost function is defined as follows:

$$g^{k+2} = g_{track}{}^{k+2} + g_{bal}{}^{k+2} \quad (13)$$

The switching state that minimizes the cost function is chosen and applied at the next sampling instant. Additional constraints (e.g., switching frequency reduction, current limitation, and spectrum shaping) can be included by adding them in the cost function [20].

C. Predictive Variables with Two-step Horizon

As shown in Fig. 3, the cost function requires predicted load currents $\underline{\mathbf{i}}^{k+2}$ and capacitor voltages $\underline{v_{c1}}^{k+2}$ and $\underline{v_{c2}}^{k+2}$ in discrete-time form.The load current prediction is obtained from continuous time state–space system in Eq. (7) as follows:

$$\begin{bmatrix}\underline{i_a}^{k+1}\\ \underline{i_b}^{k+1}\\ \underline{i_c}^{k+1}\end{bmatrix} = \mathbf{\Phi}\begin{bmatrix}\underline{i_a}^{k}\\ \underline{i_b}^{k}\\ \underline{i_c}^{k}\end{bmatrix} + \mathbf{\Gamma}\begin{bmatrix}\underline{v_{an}}^{k}\\ \underline{v_{bn}}^{k}\\ \underline{v_{cn}}^{k}\end{bmatrix} \quad (14)$$

where

$$\mathbf{\Phi} = e^{-L_{eq}^{-1}R_{eq}T_s} \quad (15)$$

$$\mathbf{\Gamma} = \int_0^{T_s} e^{-L_{eq}^{-1}R_{eq}T_s}L_{eq}^{-1}\,d\tau = (-L_{eq}^{-1}R_{eq})^{-1}(\mathbf{\Phi} - \mathbf{I}_{3\times3})L_{eq}^{-1} \quad (16)$$

The load current prediction at the $k+2$ instant is obtained as follows:

$$\begin{bmatrix}\underline{i_a}^{k+2}\\ \underline{i_b}^{k+2}\\ \underline{i_c}^{k+2}\end{bmatrix} = \mathbf{\Phi}\begin{bmatrix}\underline{i_a}^{k+1}\\ \underline{i_b}^{k+1}\\ \underline{i_c}^{k+1}\end{bmatrix} + \mathbf{\Gamma}\begin{bmatrix}\underline{v_{an}}^{k}\\ \underline{v_{bn}}^{k}\\ \underline{v_{cn}}^{k}\end{bmatrix} \quad (17)$$

Comparing Eq. (17) with Eq. (14), the same converter voltage vector is used in both $k+1$ and $k+2$ predictions.

The first-order nature of the state equations describes the model in Eqs. (1)-(10). Hence, this study considers a first-order forward Euler approximation for the derivative providing sufficient accuracy. The calculation is as follows:

$$\frac{d}{dt}\underline{x} = \frac{1}{T_s}(\underline{x}^{k+1} - \underline{x}^{k}) \quad (18)$$

By substituting Eq. (18) in Eq. (8), the DC-link capacitor voltages are represented in discrete-time form as follows:

$$\left.\begin{aligned}\underline{v_{c1}}^{k+1} &= \underline{v_{c1}}^{k} + \frac{T_s}{C_1}\underline{i_{dc1}}^{k+1}\\ \underline{v_{c2}}^{k+1} &= \underline{v_{c2}}^{k} + \frac{T_s}{C_2}\underline{i_{dc2}}^{k+1}\end{aligned}\right\} \quad (19)$$

where T_s is the sampling time, and C_1 and C_2 are the capacitances of the DC-link capacitors-1 and -2, respectively.

The DC-link capacitor currents are expressed in discrete-time as follows:

$$\left.\begin{aligned}\underline{i_{dc1}}^{k+1} &= K_a.\underline{i_a}^{k} + K_b.\underline{i_b}^{k} + K_c.\underline{i_c}^{k}\\ \underline{i_{dc2}}^{k+1} &= Q_a.\underline{i_a}^{k} + Q_b.\underline{i_b}^{k} + Q_c.\underline{i_c}^{k}\end{aligned}\right\} \quad (20)$$

The DC-link capacitor voltages for the two-step prediction are obtained by shifting variables into one future sample. This process is exhibited as follows:

$$\left.\begin{aligned}\underline{v_{c1}}^{k+2} &= \underline{v_{c1}}^{k+1} + \frac{T_s}{C_1}\underline{i_{dc1}}^{k+2}\\ \underline{v_{c2}}^{k+2} &= \underline{v_{c2}}^{k+1} + \frac{T_s}{C_2}\underline{i_{dc2}}^{k+2}\end{aligned}\right\} \quad (21)$$

where

$$\left.\begin{aligned}\underline{i_{dc1}}^{k+2} &= K_a.\underline{i_a}^{k+1} + K_b.\underline{i_b}^{k+1} + K_c.\underline{i_c}^{k+1}\\ \underline{i_{dc2}}^{k+2} &= Q_a.\underline{i_a}^{k+1} + Q_b.\underline{i_b}^{k+1} + Q_c.\underline{i_c}^{k+1}\end{aligned}\right\} \quad (22)$$

IV. Real-Time Implementation and Validation

The block diagram of the experimental setup for the proposed finite-state model predictive control of the four-leg NPC converter is shown in Fig. 5. The MATLAB/Simulink software is used along with a real-time implementation block set for all the control and feedback syntheses. The DS1103 controller is employed to handle the control processes (e.g., load current prediction and cost function minimization). The load currents and the DC-link capacitor voltages are measured using LEM LA55-P and LV25-P transducers, respectively. The feedback from the sensors is sent to the controller through the CP1103 I/O connector. The DC power supply is obtained by employing the Xantrex XDC-600-20.

The predictive controller directly generates the gating signals. These signals are then sent to the converter through the SKHI22B gate drivers. The experimental results are obtained during the steady and transient states with balanced,

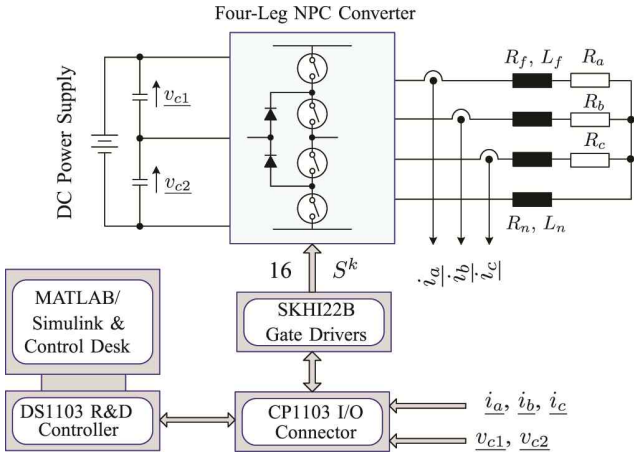

Fig. 5.Experimental setup block diagram.

TABLE II

FOUR-LEG NPC CONVERTER AND CONTROLLER PARAMETERS

Variable	Description	Value
v_{dc}	DC-link voltage	300 V
C_{dc}	DC-link capacitance	4700 µF
R_f, R_n	Filter leakage resistance	0.045 Ω
L_f, L_n	Filter inductance	10 mH
i_o^*	Nominal reference load current	10 A rms
f_o^*	Nominal reference load frequency	60 Hz
R	Nominal linear load resistance	10 Ω
R_{nl}	Nominal non-linear load resistance	20 Ω
L_{nl}	Nominal non-linear load inductance	2.5 mH
T_s	Sampling time	100 µs
λ_{dc}	Weighting factor	0.5

unbalanced, and non-linear loads considering a sampling time of T_s = 100 µs. The converter and controller parameters are summarized in Table II. The performance index parameters (i.e., $e_{\dot{v}}$, % total harmonic distortion (THD) and f_{sw}) are defined in Refs. [42] and [43]. The one-step and the proposed two-step predictions are shown in Figs. 6 and 7, respectively. A balanced reference of 10 A (rms) and a balanced load of 10 Ω are considered. The load currents with one step-prediction are shown in Fig. 6(a). This approach produces 5% reference tracking error $e_{\dot{v}}$ and 3.8%THD. The average switching frequency f_{sw} is 1996 Hz. The converter line–line voltage v_{ab} produces higher *dv*/*dt*s and THD, as shown in Fig. 6(b). The load currents with the proposed two-step prediction are shown in Fig. 7(a). $e_{\dot{v}}$, THD, and f_{sw} are 3.3%, 3.1%, and 724 Hz, respectively. Furthermore, the switching frequency significantly decreases with the proposed approach. $e_{\dot{v}}$ and THD are lower than those in the one-step predictiondespite the 2.8 times lower switching frequency. This method gives a new approach of controlling high-power converters that requiresan operation with alower switching frequency. The converter line–line voltage shown in Fig. 7(b) produces low *dv*/*dt*s compared to the one-step prediction. The fast Fourier transform window shows that the peak magnitude of the harmonics is lower with the two-step prediction. The error between the DC-link capacitor voltages lowers with the two-step prediction.

The experimental results of the unbalanced references (i.e., $\underline{i_a^*}$=12A, $\underline{i_b^*}$=10A, and $\underline{i_c^*}$=8A) and the balanced loads (i.e., $R_a = R_b = R_c = 10\ \Omega$) are presented in Fig. 8. The setup in the figure is a typical application for the three-phase, four-wire systems with different load demands in each phase. The controller independently handles each phase current. Hence, the load currents track to their references with less steady-state error, as shown in Fig. 8(a). The neutral current, which is the sum of the three-phase currents, flows through the fourth NPC leg. The neutral current in the four-leg NPC converter does not circulate through the DC-link capacitors, unlike the case of three-leg NPC converters. Hence, the DC-link capacitor voltages remain balanced, as shown in Fig. 8(b). The converter line–line voltage perfectly shows five voltage levels. $e_{\dot{v}}$, %THD, and f_{sw} are similar to the operating conditions of the previous balanced references and loads (Fig. 7). The operating condition discussed in Fig. 8 is repeated with the combined unbalanced resistive load and non-linear load (Fig. 9). The unbalanced load values are R_a = 8 Ω, R_b = 10 Ω, R_c = 12 Ω.The non-linear load values are R_{nl} = 20 Ω and L_{nl} = 2.5 mH. The load variation information is not provided to the predictive controller. The controller chooses a switching state producing a minimal error in the reference tracking and DC-link capacitor voltages even though the load parameters change. Consequently, the load currents effectively track to their references [Fig. 9(a)]. The DC-link capacitor voltages are also perfectly balanced [Fig. 9(b)]. $e_{\dot{v}}$, %THD, and f_{sw} are 4.1%, 3.6%, and 1235 Hz, respectively. This increase is insignificant although these values are higher than those of the previous operating condition (Fig. 8). This operating condition demonstrates that the proposed FCS-MPC controller is robust and handles the load parameter variations. The transient analysis is conducted considering the balanced loads (i.e., $R_a = R_b = R_c = 12\ \Omega$). A balanced step change in the reference currents is applied from "no load" to 10 A(rms) in the first case (Fig. 10). The load currents track to the references with fast rise time and no overshoot [Fig. 10(a)]. The DC-link capacitors are perfectly balanced even under the no-load condition [Fig. 10(b)]. Step change is applied from the balanced reference currents (i.e., $\underline{i_a^*} = \underline{i_b^*} = \underline{i_c^*}$ = 10 A at 60 Hz) to the unbalanced reference currents (i.e., $\underline{i_a^*}$ = 12 A at 60 Hz, $\underline{i_b^*}$ = 10 A at 120 Hz, and $\underline{i_c^*}$ = 8 A at 120 Hz) in the second case (Fig. 11). The load currents track to their references and exhibit no overshoots during the transient period [Fig. 11(a)]. Accordingly, the load neutral current changes because of the changes in the reference currents. The DC-link capacitor voltages remain balanced despite of the transient change in the reference currents [Fig. 11(b)]. The effectiveness of the

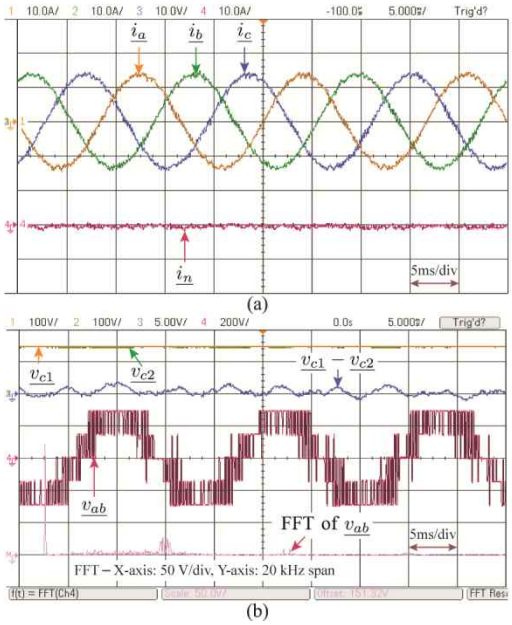

Fig. 6. Experimental results of the one-step prediction during steady state with balanced references and balanced resistive load. (a) Ch1: phase-*a* output current (10 A/div); Ch2: phase-*b* output current (10 A/div); Ch3: phase-*c* output current (10 A/div); and Ch4: output neutral current (10 A/div). (b) Ch1: DC-link capacitor-1 voltage (100 V/div); Ch2: DC-link capacitor-2 voltage (100 V/div); Ch3: difference between the DC-link capacitor voltages (5 V/div); and Ch4: converter line–line voltage (200 V/div).

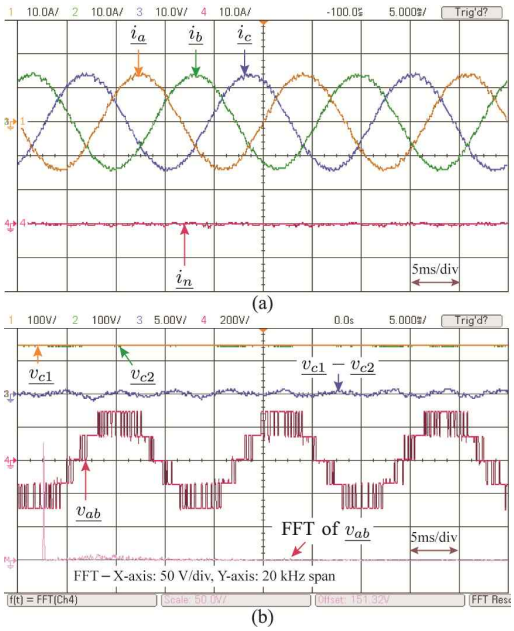

Fig. 7. Experimental results of the modified two-step prediction during steady state with balanced references and balanced resistive load. (a) Ch1: phase-*a* output current (10 A/div); Ch2: phase-*b* output current (10 A/div); Ch3: phase-*c* output current (10 A/div); and Ch4: output neutral current (10 A/div). (b) Ch1: DC-link capacitor-1 voltage (100 V/div); Ch2: DC-link capacitor-2 voltage (100 V/div); Ch3: difference between the DC-link capacitor voltages (5 V/div); and Ch4: converter line–line voltage (200 V/div).

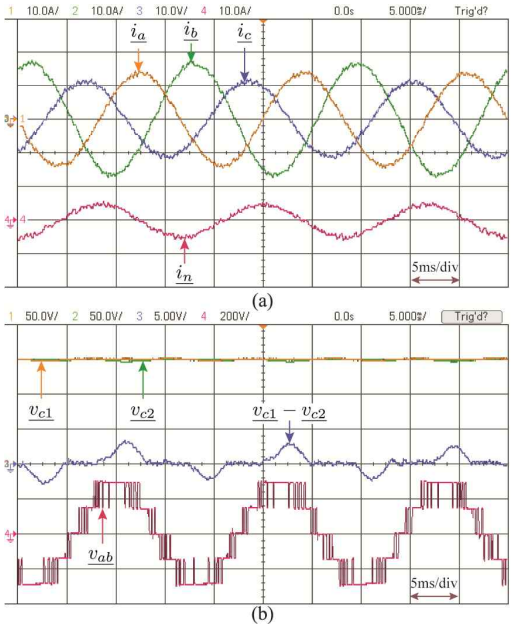

Fig. 8. Experimental results of the modified two-step prediction during steady state with unbalanced references and balanced resistive load. (a) Ch1: phase-*a* output current (10 A/div); Ch2: phase-*b* output current (10 A/div); Ch3: phase-*c* output current (10 A/div); and Ch4: output neutral current (10 A/div). (b) Ch1: DC-link capacitor-1 voltage (50 V/div); Ch2: DC-link capacitor-2 voltage (50 V/div); Ch3: difference between the DC-link capacitor voltages (5 V/div); and Ch4: converter line–line voltage (200 V/div).

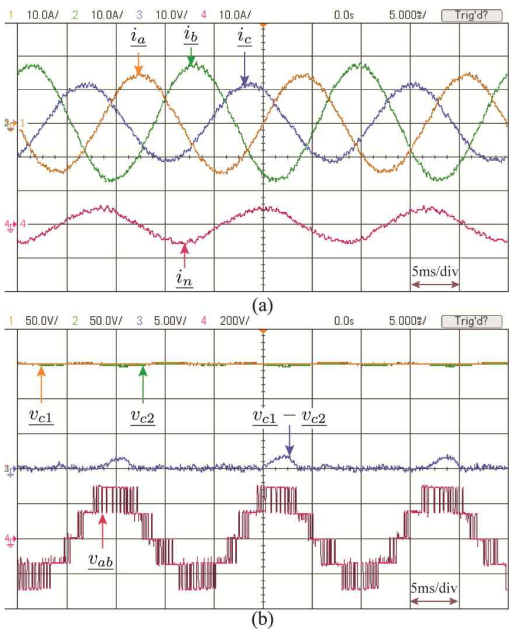

Fig. 9. Results of the modified two-step prediction during steady state with unbalanced references and unbalanced resistive + non-linear load. (a) Ch1: phase-*a* output current (10 A/div); Ch2: phase-*b* output current (10 A/div); Ch3: phase-*c* output current (10 A/div); and Ch4: output neutral current (10 A/div). (b) Ch1: DC-link capacitor-1 voltage (50 V/div); Ch2: DC-link capacitor-2 voltage (50 V/div); Ch3: difference between the DC-link capacitor voltages (5 V/div); and Ch4: converter line–line voltage (200 V/div).

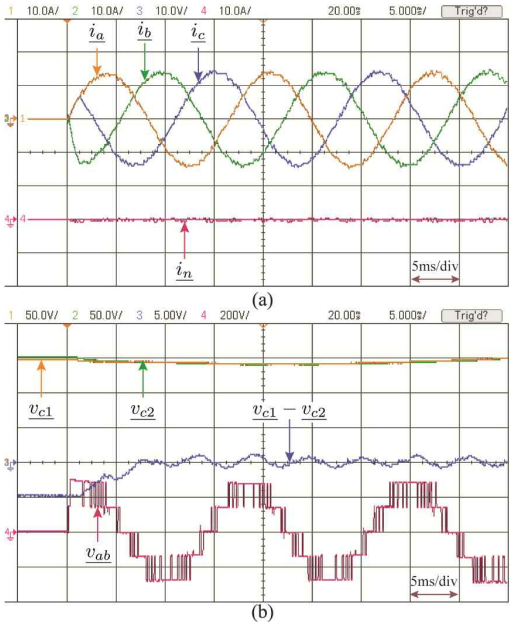

Fig. 10. Experimental results of the modified two-step prediction and balanced resistive load (10 Ω) during step change from "no references" to balanced references. (a) Ch1: phase-*a* output current (10 A/div); Ch2: phase-*b* output current (10 A/div); Ch3: phase-*c* output current (10 A/div); and Ch4: output neutral current (10 A/div). (b) Ch1: DC-link capacitor-1 voltage (50 V/div); Ch2: DC-link capacitor-2 voltage (50 V/div); Ch3: difference between the DC-link capacitor voltages (5 V/div); and Ch4: converter line–line voltage (200 V/div).

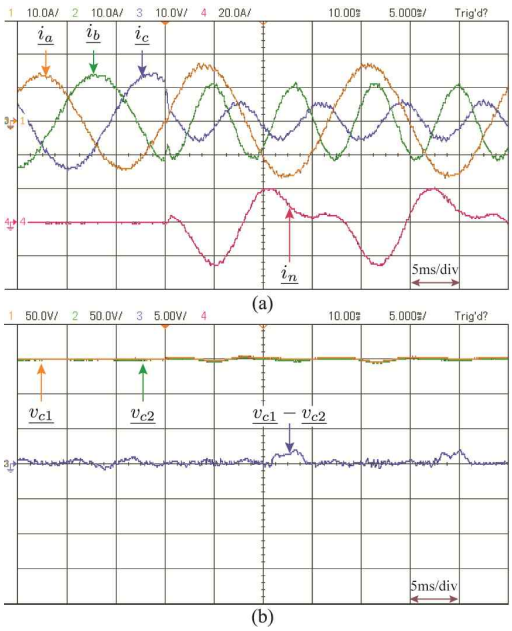

Fig. 11. Experimental results of the modified two-step prediction and balanced resistive load (10 Ω) during step change from balanced to unbalanced references. (a) Ch1: phase-*a* output current (10 A/div); Ch2: phase-*b* output current (10 A/div); Ch3: phase-*c* output current (10 A/div); and Ch4: output neutral current (10 A/div). (b) Ch1: DC-link capacitor-1 voltage (50 V/div); Ch2: DC-link capacitor-2 voltage (50 V/div); Ch3: difference between the DC-link capacitor voltages (5 V/div); and Ch4: converter line–line voltage (200 V/div).

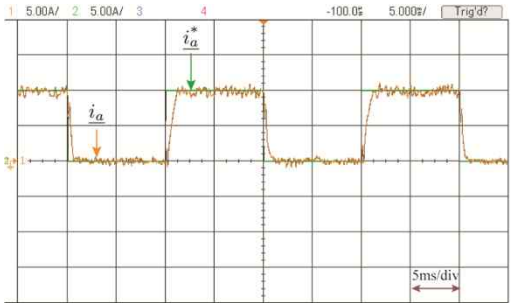

Fig. 12. Experimental results of the modified two-step prediction for square wave reference and balanced resistive load (10 Ω). (a) Ch1: reference current (10 A/div) and Ch2: load current (10 A/div).

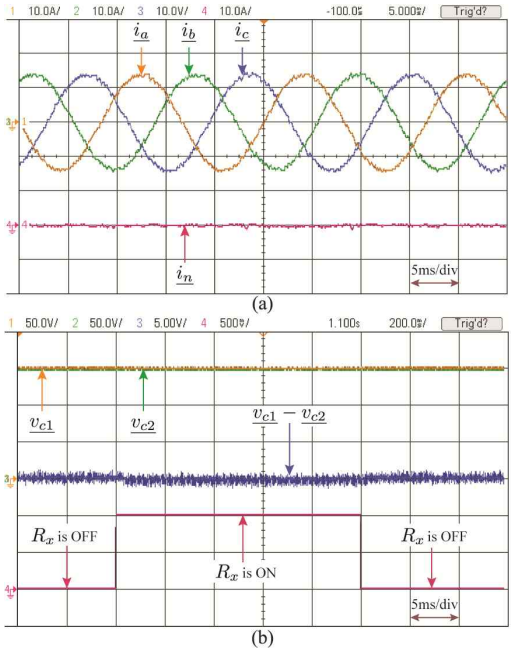

Fig. 13. Experimental results of the modified two-step prediction during steady state with balanced references, balanced resistive load (10 Ω), and a resistor across the DC-link capacitor-1. (a) Ch1: phase-*a* output current (10 A/div); Ch2: phase-*b* output current (10 A/div); Ch3: phase-*c* output current (10 A/div); and Ch4: output neutral current (10 A/div). (b) Ch1: DC-link capacitor-1 voltage (50 V/div); Ch2: DC-link capacitor-2 voltage (50 V/div); Ch3: difference between the DC-link capacitor voltages (5 V/div); and Ch4: converter line–line voltage (200 V/div).

proposed FCS-MPC controller to track to any kind of references is exhibited in Fig. 12. A square wave reference with 5 A amplitude and 60 Hz frequency is considered. The loads are similar to those of the preceding transient-state analysis. A good load current tracking to its reference is observed with a fast and dynamic response and no oscillations in Fig. 12.

An external resistor R_x (100 Ω) is deliberately connected across the DC-link capacitor$C_1$to verify the robustness of the proposed algorithmin minimizing the imbalance of the DC-link capacitor voltages. The balanced references of 10 A(rms) and the balanced loads of 10 Ωare considered for this test. The turn-on and turn-off signals for the relay connecting and

disconnecting$R_x$are shown in Fig. 13(b). The controller acts in a few sampling instants even with the step-connection of the resistor. Hence, the capacitor voltages are continuously balanced [Fig. 13(b)]. The load currents continue to track to their references during this process as in Fig. 13(a). The feasibility of the proposed predictive control scheme is verified for different references and loads.

The FCS-MPC strategy strongly relies on the system model and the converter and load parameters. The tests in Figs.9 and 13 validate that the FCS-MPC strategy compensates for the changes in the load and the DC-link parameter variations, respectively. The FCS-MPC strategy also effectively handles the inductive filter parameter variations [25], [41], [43]. Extreme variations in the converter and load parameters deteriorate the control performance. An online parameter estimation algorithm should be used in conjunction with the FCS-MPC strategy in such conditions [33].

This study uses a sampling time $T_s$of 100 µs. This value represents the minimum execution time required to perform the optimization algorithm during each sampling interval. The T_s value dictates the switching frequency f_{sw} in the classical control techniques. However, the converter switching frequency in the FCS-MPC strategy varies according to the operating conditions. The nature of the variable-switching frequency is controlled by including a constraint in the cost function. The steady-state performance offered by the classical and predictive control techniques is almost similar. However, the latter approach provides a superior and dynamic performance because of the elimination of internal current loops and modulators [25], [28], [34], [41]. The comprehensive comparison and analysis between the classical and the proposed two-step FCS-MPC are not covered in the scope of this study. Hence, these two aspects are considered as topics for future work.

V. CONCLUSIONS

This study proposes a finite-set model predictive control strategy with a two-step prediction horizon to control a three-phase, four-leg NPC converter. The proposed two-step prediction significantly decreases the switching frequency while maintaining an acceptable load current quality. This method is simple and promising for the control of high-power converters. The control algorithm evaluates each of the 81 possible switching states and chooses a switching state that minimizes the cost function. The ideal minimum of the cost function is zero, which indicates that the control objectives are perfectly achieved. The load currents are tracked to their references with acceptable error using the proposed predictive control. Furthermore, the DC-link capacitor voltages are balanced during all the operating conditions. The control scheme also compensates for the perturbations in the DC-link and load parameter changes, while the load currents continue effective tracking to their references. This compensation is achieved without sacrificing the converter operation. The linear PI controllers and the modulation stage are further eliminated. As a result, a fast and dynamic response is achieved. Therefore, the proposed methodology is an attractive alternative for controlling four-leg NPC converters. The feasibility of the proposed algorithm is experimentally verified.

ACKNOWLEDGMENT

The authors wish to thank the financial support from the Natural Sciences and Engineering Research Council of Canada (NSERC) through Wind Energy Strategic Network (WESNet) Project 3.1, Fondecyt Initiation into Research 11121492, CONICYT PCCI 12048 Project and Universidad Tecnica Federico Santa Maria. This publication was made possible by NPRP grant 4-077-2-028 from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors.

REFERENCES

[1] D. Fernandes, F. Costa, and E. dos Santos Jr., "Digital-scalar PWM approaches applied to four-leg voltage-source inverters," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 2022-2030, May 2013.

[2] Z. Liu, J. Liu, and J. Li, "Modeling, analysis and mitigation of load neutral point voltage for three-phase four-leg inverter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 2010-2021, May 2013.

[3] M. Rivera, V. Yaramasu, A. Llor, J. Rodriguez, B. Wu, and M. Fadel, "Digital predictive current control of a three-phase four-leg inverter," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 11, pp. 4903-4912, Nov. 2013.

[4] X. Wang, F. Zhuo, J. Li, L. Wang, and S. Ni, "Modeling and control of dual-stage high-power multifunctional PV system in d-q-o coordinate," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 4, pp. 1556-1570, Apr. 2013.

[5] N. Prabhakar and M. Mishra, "Dynamic hysteresis current control to minimize switching for three-phase four-leg VSI topology to compensate nonlinear load," *IEEE Power Electron. Lett.*,Vol. 25, No. 8, pp. 1935-1942, Aug. 2010.

[6] B. Singh, P. Jayaprakash, S. Kumar, and D. Kothari, "Implementation of neural-network-controlled three-leg VSC and a transformer as three- phase four-wire DSTATCOM," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 4, pp. 1892-1901, Jul./Aug. 2011.

[7] S. Karanki, N. Geddada, M. Mishra, and K. Boddeti, "A modified three- phase four wire UPQC topology with reduced DC-link voltage rating," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 9, pp. 3555-3566, Sep. 2013.

[8] Y. Kumsuwan, S. Premrudeepreechacharn, and V. Kinnares, "A carrier- based unbalanced PWM method for four-leg voltage source inverter fed unsymmetrical two-phase induction motor," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 5, pp. 2031-2041, May. 2013.

[9] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Perez, and J. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 8, pp.

2553-2580, Aug. 2010.
[10] B. Wu, High-power converters and AC drives, 1st ed., ser. Wiley-IEEE Press. John Wiley & Sons, Inc., 2006.
[11] J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neutral- point-clamped inverters," *IEEE Trans. Ind. Electron.*, Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.
[12] S. Ceballos, J. Pou, J. Zaragoza, J. Martin, E. Robles, I. Gabiola, and P. Ibanez, "Efficient modulation technique for a four-leg fault-tolerant neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 3, pp. 1067-1074, Mar. 2008.
[13] J.-H. Kim, S.-K. Sul, and P. Enjeti, "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage- source inverter," *IEEE Trans. Ind. Appl.*, Vol. 44, No. 4, pp. 1239-1248, Jul./Aug. 2008.
[14] N.-Y. Dai, M.-C. Wong, and Y.-D. Han, "Application of a three-level NPC inverter as a three-phase four-wire power quality compensator by generalized 3DSVM," *IEEE Trans. Power Electron.*, Vol. 21, No. 2, pp. 440-449, Mar. 2006.
[15] M.-C. Wong, Z.-Y. Zhao, Y.-D. Han, and L.-B. Zhao, "Three- dimensional pulse-width modulation technique in three-level power inverters for three-phase four-wired system," *IEEE Trans. Power Electron.*, Vol. 16, No. 3, pp. 418-427, May 2001.
[16] L. Franquelo, M. Prats, R. Portillo, J. Galvan, M. Perales, J. Carrasco, E. Diez, and J. Jimenez, "Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 2, pp. 458-466, Apr. 2006.
[17] S. Ceballos, J. Pou, J. Zaragoza, J. Martin, E. Robles, I. Gabiola, and P. Ibanez, "Efficient modulation technique for a four-leg fault-tolerant neutral-point-clamped inverter," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 3, pp. 1067-1074, Mar. 2008.
[18] D. Lee, J. Jung, and S. Kwak, "Simple space vector pwm scheme for 3-level npc inverters including the over modulation region," *Journal of Power Electronics*, Vol. 11, No. 5, pp. 688-696, Sep. 2011.
[19] W. Kwon, S. Han, and S. Han, *Receding Horizon Control: Model Predictive Control for State Models*, ser. Advanced Textbooks in Control and Signal Processing. Springer-Verlag, 2005.
[20] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model predictive control-A simple and powerful method to control power converters," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 6, pp. 1826-1838, Jun. 2009.
[21] P. Cortes, M. Kazmierkowski, R. Kennel, D. Quevedo, and J. Rodriguez, "Predictive control in power electronics and drives," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 12, pp. 4312-4324, Dec. 2008.
[22] T. Vyncke, S. Thielemans, and J. Melkebeek, "Finite-set model-based predictive control for flying-capacitor converters: Cost function design and efficient FPGA implementation," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 2, pp. 1113-1121, 2013.
[23] P. Martin Sanchez, O. Machado, E. Bueno, F. J. Rodriguez, and F. J. Meca, "FPGA-based implementation of a predictive current controller for power converters," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 3, pp. 1312-1321, Aug. 2013.
[24] A. Damiano, G. Gatto, I. Marongiu, A. Perfetto, and A. Serpi, "Operating constraints management of a surface-mounted PM synchronous machine by means of an FPGA-based model predictive control algorithm," *IEEE Trans. Ind. Informat.*, Vol. 10, No. 1, pp. 243–255, Feb. 2014.
[25] J.-i. Kang, S.-K. Han, and J. Han, "Lossless snubber for tapped-inductor boost converter for high step-up application," in *Proc. ICIT*, pp. 253-260, 2014.
[26] R. Morales-Caporal, E. Bonilla-Huerta, C. Hernandez, M. Arjona, and M. Pacas, "Transducerless acquisition of the rotor position for predictive torque controlled PM synchronous machines based on a DSP-FPGA digital system," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 2, pp. 799-807, May 2013.
[27] J. Scoltock, T. Geyer, and U. Madawala, "A comparison of model predictive control schemes for MV induction motor drives," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 2, pp. 909-919, May 2013.
[28] R. Aguilera, P. Lezana, and D. Quevedo, "Finite-control-set model predictive control with improved steady-state performance," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 2, pp. 658-667, May 2013.
[29] J. Hu, "Improved dead-beat predictive DPC strategy of grid-connected dc-ac converters with switching loss minimization and delay compensations," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 2, pp. 728-738, May 2013.
[30] D. du Toit, H. Mouton, R. Kennel, and P. Stolze, "Predictive control of series stacked flying-capacitor active rectifiers," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 2, pp. 697-707, May 2013.
[31] M. Preindl and S. Bolognani, "Model predictive direct torque control with finite control set for PMSM drive systems, Part 1: Maximum torque per ampere operation," *IEEE Trans. Ind. Informat.*, Vol. 9, No. 4, pp. 1912-1921, Nov. 2013.
[32] M. Rivera, J. Rodriguez, J. Espinoza, and H. Abu-Rub, "Instantaneous reactive power minimization and current control for an indirect matrix converter under a distorted AC supply," *IEEE Trans. Ind. Informat.*, Vol. 8, No. 3, pp. 482-490, Aug. 2012.
[33] C. Xia, M. Wang, Z. Song, and T. Liu, "Robust model predictive current control of three-phase voltage source PWM rectifier with online disturbance observation," *IEEE Trans. Ind. Informat.*, Vol. 8, No. 3, pp. 459-471, Aug. 2012.
[34] H. Young, M. Perez, J. Rodriguez, and H. Abu-Rub, "Assessing finite- control-set model predictive control: A comparison with a linear current controller in two-level voltage source inverters," *IEEE Ind. Electron. Mag.*, Vol. 8, No. 1, pp. 44-52, Mar. 2014.
[35] P. Stolze, P. Landsmann, R. Kennel, and T. Mouton, "Finite-set model predictive control of a flying capacitor converter with heuristic voltage vector preselection," in *Proc. IEEE–ICPE-ECCE Conf.*, pp. 210-217, 2011.
[36] V. Yaramasu, B. Wu, M. Rivera, and J. Rodriguez, "Enhanced model predictive voltage control of four-leg inverters with switching frequency reduction for standalone power systems," in *Proc. IEEE–EPE/PEMC Conf.*, pp. DS2c.6–1– DS2c.6–5, 2012.
[37] T. Geyer and D. Quevedo, "Multistep finite control set model predictive control for power electronics - Part 1: Algorithm," *IEEE Trans. Power Electron.*, Vol. 29, No. 12, pp. 6836–6846, Dec. 2014.
[38] V. Yaramasu, B. Wu, M. Rivera, J. Rodriguez, and A. Wilson, "Cost-function based predictive voltage control of two-level four-leg inverters using two step prediction horizon for standalone power systems," in *Proc. IEEE–APEC Conf.*, pp. 128-135, 2012.

[39] P. Cortes, J. Rodriguez, S. Vazquez, and L. Franquelo, "Predictive control of a three-phase UPS inverter using two steps prediction horizon," in *Proc. IEEE–ICIT Conf.*, pp. 1283-1288,2010.
[40] T. Geyer, "Generalized model predictive direct torque control: Long prediction horizons and minimization of switching losses," in *Proc. IEEE–CCC Conf.*, pp. 6799-6804, 2009.
[41] J. Rodriguez and P. Cortes, *Predictive Control of Power Converters and Electrical Drives*, 1st ed. IEEE Wiley press, 2012.
[42] V. Yaramasu, M. Rivera, B. Wu, and J. Rodriguez, "Model predictive current control of two-level four-leg inverters – Part I: Concept, algorithm and simulation analysis," *IEEE Trans. Power Electron.*, Vol. 28, No. 7, pp. 3459-3468, Jul. 2013.
[43] M. Rivera, V. Yaramasu, J. Rodriguez, and B. Wu, "Model predictive current control of two-level four-leg inverters – Part II: Experimental implementation and validation," *IEEE Trans. Power Electron.*, Vol. 28, No. 7, pp. 3469-3478, Jul. 2013.

Venkata Yaramasu(S'08-M'14)received his M.E. and Ph.D degrees in Electrical Engineering from SGS Institute of Technology and Science, Indore, India, in 2008 and Ryerson University, Toronto, Canada, in 2014, respectively. He is currently a Postdoctoral Research Fellow with Ryerson University. His research interests include renewable energy, high power converters, electric vehicles, and predictive control.

Marco Rivera (S'09-M'11) received his B.Sc. in Electronics Engineering and M.Sc. in Electrical Engineering from the Universidad de Concepción, Chile in 2007 and 2008, respectively. He earned his PhD degree at the Department of Electronics Engineering, Universidad Técnica Federico Santa María, in Valparaíso, Chile, in 2011. He is currently a professor in the Department of Industrial Technologies at Universidad de Talca, Curicó, Chile. In 2013 Prof. Rivera was awarded with the Premio Tesis de Doctorado Academia Chilena de Ciencias 2012, which is awarded to the best PhD Thesis developed in 2011 for national and foreign students in any exact or natural sciences program that is a member of the Academia Chilena de Ciencias, Chile.

Mehdi Narimani received his B.S. and M.S degrees from Isfahan University of Technology (IUT), Isfahan, Iran in 1999 and 2002 respectively, and his PhD degree from University of Western Ontario, Ontario, Canada, all in Electrical Engineering. He is currently a Postdoctoral Research Associate at the Department of Electrical and Computer Engineering at Ryerson University and Rockwell Automation Canada. He worked as a faculty member of Isfahan University of Technology from 2002 to 2009, where he was involved in design and implementation of several industrial projects. He is the author of more than 45 journal and conference proceeding papers, and he holds three patents (pending review). His current research interests include high power converters, control of power electronics, and renewable energy Systems.

Bin Wu (S'89-M'92-SM'99-F'08) received his M.A.Sc. and Ph.D. degrees in Electrical and Computer Engineering from the University of Toronto, Toronto, ON, Canada in 1989 and 1993, respectively.In 1993, he joined Ryerson University, Toronto, where he is currently a Professor and Senior NSERC/Rockwell Automation Industrial Research Chair in Power Electronics and Electric Drives.He has has published more than 300 technical papers, authored/coauthored two Wiley-IEEE Press books, and holds more than 25 issued/pending patents in the area of power conversion, medium-voltage drives, and renewable energy systems.Dr. Wu received the Gold Medal of the Governor General of Canada in 1993, Premier's Research Excellence Award in 2001, NSERC Synergy Award for Innovation in 2002, Ryerson Distinguished Scholar Award in 2003, YSGS Outstanding Contribution to Graduate Education Award, and the Professional Engineers Ontario Engineering Excellence Medal in 2014.He is a Fellow of the Engineering Institute of Canada and Canadian Academy of Engineering (CAE).

Jose Rodriguez (M'81-SM'94-F10) received his degree in Electrical Engineering from the Universidad Federico Santa Maria (UTFSM), Valparaiso, Chile, in 1977 and his Dr.-Ing. degree in Electrical Engineering from the University of Erlangen, Erlangen, Germany, in 1985. He has been with the Department of Electronics Engineering, University Federico Santa Maria since 1977, where he is currently Full Professor and Rector. He has co-authored more than 350 journal and conference papers. His main research interests include multilevel inverters, new converter topologies, control of power converters, and adjustable-speed drives. Prof. Rodriguez is the Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS, INDUSTRIAL ELECTRONICS, and INDUSTRIAL INFORMATICS. He has received a number of Best Paper Awards from different IEEE Journals. Prof. Rodríguez is a Fellow of the Chilean Academy of Engineering and of the IEEE. He was the recipient of the National Applied Sciences and Technology Award of Chile 2014.