JPE 14-6-12

http://dx.doi.org/10.6113/JPE.2014.14.6.1189
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Module Multilevel-Clamped Composited Multilevel Converter (M-MC^2) with Dual T-Type Modules and One Diode Module

Haoze Luo*, Yufei Dong*, Wuhua Li†, and Xiangning He*

*†College of Electrical Engineering, Zhejiang University, Hangzhou, China

Abstract

A modular multilevel-clamped composited multilevel converter (M-MC^2) is proposed. M-MC^2 enables topology reconfiguration, power device reuse, and composited clamping. An advanced five-level converter (5L-M-MC^2) is derived from the concept of M-MC^2. 5L-M-MC^2 integrates dual three-level T-type modules and one three-level neutral point clamped module. This converter can also integrate dual three-level T-type modules and one passive diode module by utilizing the device reuse scheme. The operation principle and SPWM modulation are discussed to highlight converter performance. The proposed M-MC^2 is comprehensively compared with state-of-the-art five-level converters. Finally, simulations and experimental results are presented to validate the effectiveness of the main contributions of this study.

Key words: Composited clamped scheme, Multilevel modular converter, Power device reuse

I. INTRODUCTION

Multilevel converters are generally recognized as reasonable and effective configurations to break down contradictions between limited power device capacities and medium-voltage (MV) high power systems, such as new energy power generation and high power driver systems [1]-[5]. Multilevel converters achieve higher output voltage levels than traditional two-level converters by reducing the voltage steps from indirect power devices in series. Increased output voltage levels result in low dv/dt, which enhances output power quality and decreases insulation damage in MV high power systems.

Voltage source multilevel converters are generally divided into three fundamental groups, namely, diode-clamped converters, flying capacitor (FC) converters, and cascaded H-bridge converters (CHB) [6], [7], which have been successfully applied in industrial areas. Three-level neutral point clamped inverters (3L-NPC) with IGBTs or IGCTs are standard products in MV drives [8]-[10]. Clamped diodes are replaced by active power devices to derive the active 3L-NPC (3L-ANPC) topology and to solve the thermal imbalance in 3L-NPC circuits [11]. However, additional voltage levels are needed to decrease total harmonic distortion (THD) in some high-quality AC systems. The number of diodes or FCs significantly increase when diode-clamped or FC converters are expanded to higher voltagelevel applications. The CHB topology can be easily extended to higher level applications because of its modular design. However, each H bridge cell requires an isolated DC supply, which is generally obtained from multipulse diode rectifiers [12]. The high complexity and cost of phase shifting transformers are the main drawbacks when high voltage levels are required. Advanced multilevel converters are introduced and developed according to combined basic ML topologies to derive high-performance five-level converters with simplified structures. A five-level NPC H-bridge inverter (5L-NPC/H-bridge) is proposed and applied, as shown in Fig. 1(a); these H-bridge cells consist of two three-level NPC circuits [13].

Consequently, the power switch numbers are less than those of 5L diode-clamped converters. An additional auxiliary 3L-NPC is inserted into a three-phase 3L-NPC topology to generate a five-level multilevel clamped multilevel converter (5L-MLC^2) with fewer power devices [14]. However, the modulation of 5L-MLC^2 is slightly complex because the additional auxiliary 3L-NPC unit has three phases. Two

Manuscript received Mar. 31, 2014; accepted Oct. 6, 2014
Recommended for publication by Associate Editor Seung-Ki Sul.
†Corresponding authors: woohualee@zju.edu.cn
Tel: + 86-571-87952416, Zhejiang University
*College of Electrical Engineering, Zhejiang University, China

half-bridge cells and one 3L-NPC converter are integrated to reduce the number of diodes in 5L diode-clamped converters and to derive a 5L-composed topology, as plotted in Fig. 1(b) [15]. However, the voltage stress of diodes may double in the case of the highest level generation when compared with the switch voltage stress. Furthermore, a five-level hybrid converter composed of active NPC and FC configuration (5L-ANPC) is proposed by ABB and employed in a commercial ACS 2000 system [16], as demonstrated in Fig. 1(c). However, the pre-charging and voltage balance of the FC is a serious concern.

Modular multilevel structures generally increase system reliability and are suitable for large-scale manufacturing. However, most state-of-the-art multilevel topologies are generated only through cell-by-cell combination with different basic units [17]-[19]. Deriving advanced multilevel converters with modular configuration and less power switches remains an attractive research topic. A modular multilevel-clamped composited multilevel converter (M-MC^2) is proposed to provide information on modular multilevel topology generation and its advantages, including topology reconfiguration, power device reuse, and composited clamping. On the basis of M-MC^2, one 3L-NPC and two 3L-T-type converters are integrated and reconstituted to derive an advanced five-level converter. The derived 5L topology only consists of two three-level T-type modules and one passive diode module because some power switches are shared in the proposed topology.

This paper is organized as follows: In Section II, the proposed concept of M-MC^2 is highlighted to derive an advanced five-level converter. In Section III, the operation principle and PWM modulation of the derived 5L-M-MC^2 are described. In Section IV, the advantages of the derived converter are explored by comprehensively comparing it with other multilevel converters. In Section V, the simulation and experimental waveforms of the proposed converter are illustrated to demonstrate its superior performance. In Section VI, the conclusions are drawn and summarized.

II. Modular Multilevel-Clamped Composited Multilevel Converter (M-MC^2) Concept

Fig. 2 shows the multilevel-clamped multilevel converters (MLC^2) proposed in [14].

The MLC^2 solution is different from the conventional multilevel generation law; a set of multilevel clamping units (MCU) is connected to one multilevel output unit (MOU) in the main power converter. MCU is an auxiliary switched circuit unit that conveys additional voltage levels, and the number of auxiliary clamping points depends on the MOU configuration. MCU and MOU could be two-level or multilevel converters. Consequently, the output voltage levels

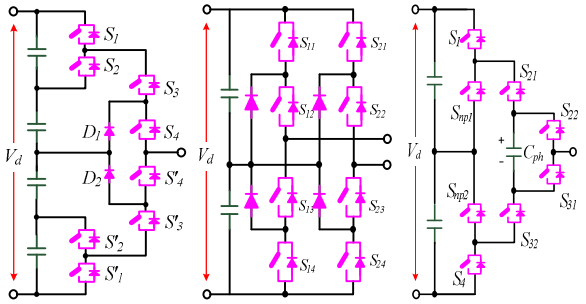


Fig. 1. State-of-the-art five-level topologies: (a) 5L-NPC/H-bridge converter, (b) 5L-Composed topology, (c) 5L-ANPC converter.

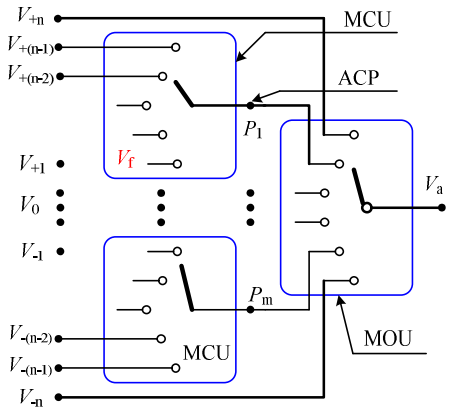


Fig. 2. Published MLC^2 concept in [14].

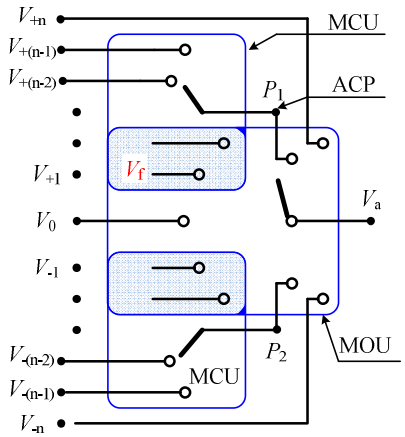


Fig. 3. Block diagram of the proposed M-MC^2.

of MOU can be easily expanded by MCU. The topological complexity, which originates from the MLC^2 concept, depends on the specific configurations of MCU and MOU. The combined converters generally become more complex as the voltage levels of MCU or MOU increase. However, inner voltage level generation, excluding the outmost voltage levels, should be connected to auxiliary clamping points, as shown in Fig. 2. The power in inner voltage levels should flow through both MCU and MOU. This procedure increases the complexity of the converters derived from MLC^2.

The switches in MCU and MOU could be composited to decrease circuit configuration and simplify the power flow path

through valuable innovations. Fig. 3 shows an improved modular multilevel-clamped composited multilevel converter (M-MC^2) derived from a power device reuse scheme.

The outmost voltage levels and part of the inner voltage levels remain unchanged in the proposed M-MC^2, similar to MLC^2. However, the rest of the inner voltage levels are directly generated by MOU because of the original function of MOU and the shared power switches in MCU and MOU, which make the auxiliary clamping point dispensable. Consequently, the circuit configuration of derived multilevel converters from M-MC^2 can be simplified. An advanced five-level converter (5L-M-MC^2) is generated (Fig. 4). This converter is employed to explore the detailed topology generation procedure on the basis of M-MC^2.

Two three-level T-type modules and one 3L-NPC module are integrated and composited. The bidirectional switches in the three-level T-type modules are implemented by two independent or reverse-blocking IGBTs [20]. The series active switches S_{a1}, S_{a02}, S_{a3}, and S_{a4} in the two three-level T-type modules coincide with the four series switches in the 3L-NPC module.

According to M-MC^2, some power devices could be shared when two structures are combined. Fig. 3 shows that the two 3L-T-type modules serve as MCUs, and the 3L-NPC module acts as an MOU. The outmost voltage levels are directly generated by conducting S_{a1}, S_{a2} or S_{a3}, S_{a4} in the derived 5L-M-MC^2. The innermost voltage level is generated by conducting S_{a2}, D_{ca1} or S_{a3}, D_{ca2}, similar to the case of the MOU in the 3L-NPC converter. The other voltage levels are synthesized by generating S_{ca1}/S_{ca3}, S_{a2} or S_{ca2}/S_{ca4}, S_{a3}, which integrates MCUs and the MOU. Consequently, the required power switch number is reduced because the power devices in the dual 3L-T-type and 3L-NPC modules are shared and reused. Both diode- and active-clamped approaches are included in the derived 5L-M-MC^2. Key power switches are reused and reconfigured in the MCUs and MOU. Fig. 5 shows that the derived 5L-M-MC^2 can easily be extended to three-phase systems.

III. Operation Principle and Modulation for the Derived 5L-M-MC^2

A. Switching Pattern

The single phase of the derived 5L-M-MC^2 is re-drawn in Fig. 6 for improved switching pattern analysis.

Inverter leg A consists of eight active switches and two clamping diodes. In the following analysis, the voltage across each capacitor is assumed to be E, and the total DC voltage V_d is equally divided by the capacitors (V_d =4E).

Table I shows the operating status of the proposed topology, as represented by the switching states; "1" indicates that the corresponding active switch is turned on, whereas "0" indicates that the switch is turned off. The voltage at terminal A with

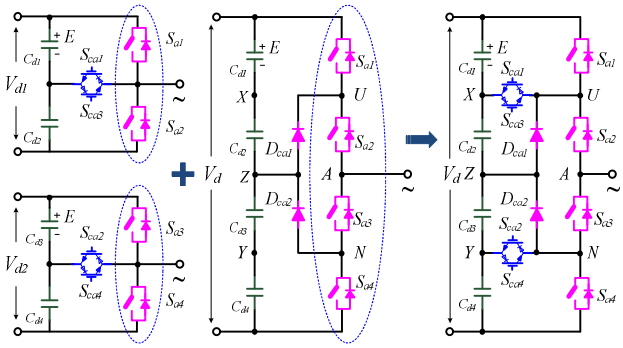


Fig. 4. Derivative processes of the proposed five-level topology.

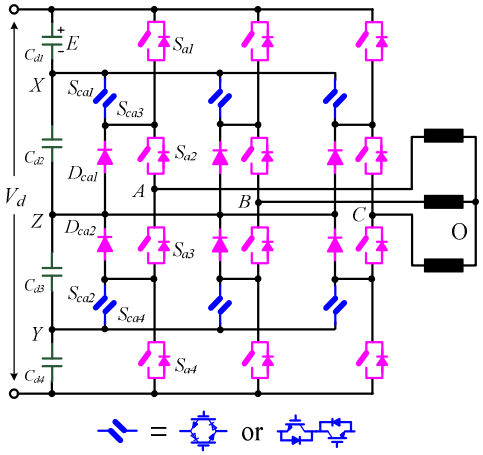


Fig.5. Circuit configuration of the three-phase 5L-M-MC^2 system.

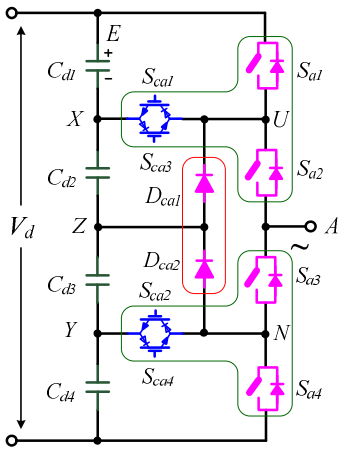


Fig. 6. Single phase of the proposed 5L-M-MC^2.

respect to neutral point Z is the terminal voltage v_{AZ}. Five different output voltage levels are synthesized with the corresponding switching states. Four switches are observed in the conduction states at any time, and the switch pairs [(S_{a1}, S_{ca1}), (S_{a2}, S_{ca2}), (S_{a3}, S_{ca3}), (S_{a4}, S_{ca4})] are complementary. Only two of eight active devices in the inverter leg are involved in the transition between adjacent states. The output voltage has five voltage levels, namely, +2E, +1E, 0E, -1E, and -2E.

B. Switching Commutation

TABLE I
DEFINITION OF SWITCHING STATES

Switching State	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{ca1}	S_{ca2}	S_{ca3}	S_{ca4}
2P(+2*E*)	**1**	**1**	0	0	0	0	**1**	**1**
P (+1*E*)	0	**1**	0	0	**1**	0	**1**	**1**
O (0*E*)	0	**1**	**1**	0	**1**	0	0	**1**
N (-1*E*)	0	0	**1**	0	**1**	**1**	0	**1**
2N (-2*E*)	0	0	**1**	**1**	**1**	**1**	0	0

Fig. 7 illustrates the commutation process with $i_{out} > 0$. In the switching state "2P," the load current i_{out} flows though S_{a1} and S_{a2}, whereas S_{ca3} and S_{ca4} are gated on. S_{ca3} and D_{ca1} are reversed-biased because of the conduction of S_{a1}. The voltage across the bidirectional switches is equal to E, which indicates that S_{ca1} is reversed-biased and is thus turned off. When the switching state commutates to state "P," S_{a1} should first be turned off with the current i_{out} naturally commutating through S_{ca3}; S_{ca1} is then turned on after time δ. The current is diverted from S_{ca3} to D_{ca1} when the converter commutates from state "P" to state "O" with $i_{out} > 0$. S_{ca3} is first turned off, and the path of i_{out} changes from S_{ca3} to D_{ca1}. S_{ca4} is reversed-blocked but gated on.

Figs. 7(c) to (d) illustrates the other commutations and voltage stress changes. The maximum voltage stress of S_{a1} to S_{a4} is half of V_d, whereas the two bidirectional switches withstand only a quarter of V_d. The commutation with $i_{out} < 0$ is similar because of the symmetry of the proposed topology.

C. Modulation of the Proposed Converter

Space vector modulation (SVM) is widely used for voltage source inverters because of real-time modulation and high DC bus voltage utilization. However, space vectors and redundant switching states exponentially increase when the number of output voltage levels exceeds three. The location of the reference vector is difficult to determine in the Cartesian coordinate system. However, the fast space vector modulation algorithm based on a hexagonal coordinate system avoids several trigonometric operations and reduces computational workload [21]. This fast algorithm is applicable to the proposed 5L-M-MC^2. Level-shifted multicarrier modulation is also extensively employed in multilevel converter applications. This modulation is divided into three schemes: in-phase disposition (IPD), alternative phase opposite disposition (APOD), and phase opposite disposition (POD). The IPD modulation scheme provides a notable harmonic profile, which is discussed in [22]. Fig.8 presents the key waveforms of a five-level inverter modulated by the IPD carrier-based modulation scheme.

Four carrier waves (v_{car1}, v_{car2}, v_{car3}, and v_{car4}) are disposed vertically. Gate signals (v_{g1}, v_{g2}, v_{g3}, and v_{g4}) for S_{a1}, S_{a2}, S_{a3}, and S_{a4} in Fig. 8 are generated at the intersections of the

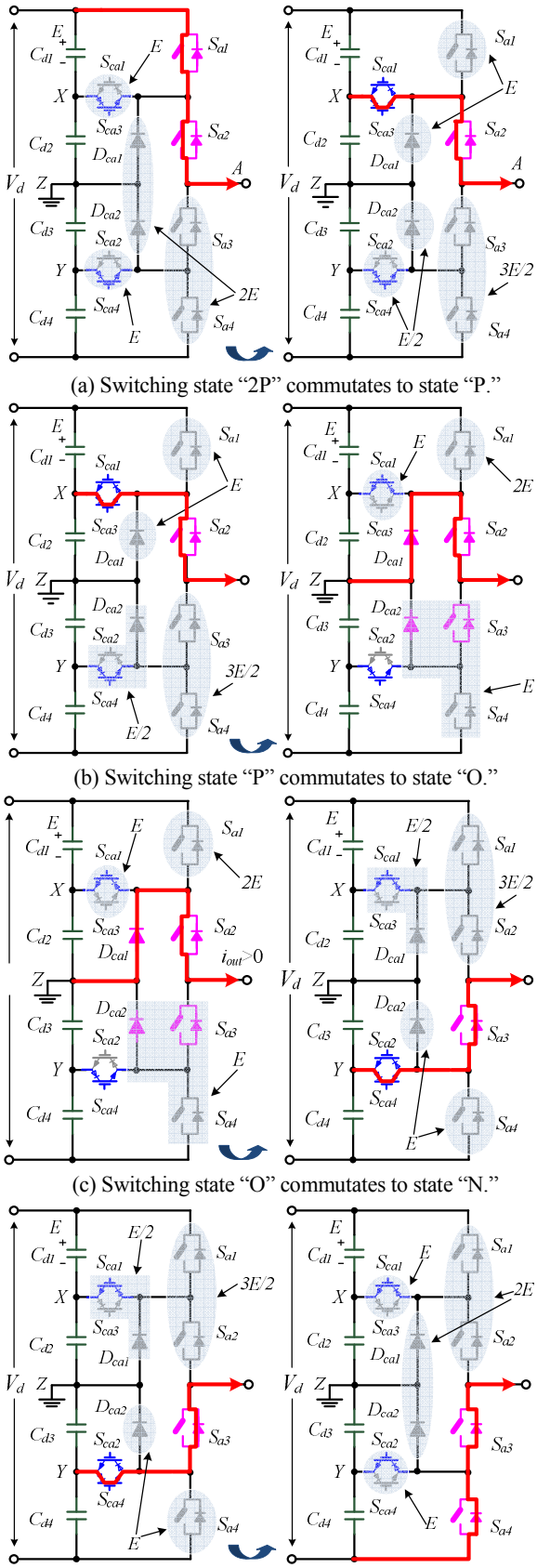


Fig. 7. Commutation between different switching states with $i_{out} > 0$.

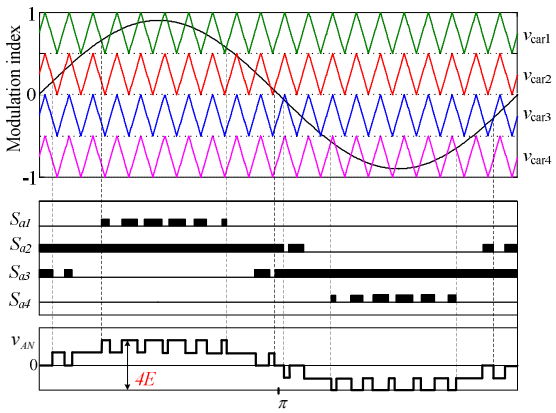


Fig. 8. Simulation waveforms in the proposed converter using IPD modulation (f_o=50Hz, f_{sw}=1kHz, M=0.95).

carrier waveforms and the modulation wave. The gate signals of S_{ca1}, S_{ca2}, S_{ca3}, and S_{ca4} are complementary to v_{g1}, v_{g2}, v_{g3}, and v_{g4} and are thus, not plotted in Fig. 8. The modulation of the proposed 5L-M-MC^2 is straightforward and easily implemented.

IV. Significant Converter Features and Performance Comparison

The practical establishment of the proposed 5L-M-MC^2 is simpler than that of conventional multilevel topologies because only three modules are required (i.e., two 3L-T-type modules and one diode module). The modularized structure facilitates the bus–bar design and modular production in high-power applications. The clamping diodes and active switches could withstand different voltage stresses. For instance, when the switching state "2P" commutates to state "P" with $i_{out} > 0$, the voltage across switches S_{a3} and S_{a4} are $2E$ and $3E/2$, respectively. However, the maximum voltage stresses of the power devices could withstand half of the total DC voltage during commutation, whereas the two bidirectional switches could withstand only one quarter of V_d. The bidirectional switches consist of low-voltage devices, which significantly reduces the cost of 5L-M-MC^2.

Table II presents a comparison of the state-of-the-art 5L topologies. The conventional 5L diode-clamped converter requires eight switches and 12 diodes with $V_{dc}/4$ voltage rating. The number of diodes is significantly reduced to two in 5L-M-MC^2. Unlike the conventional 5L FC converter, 5L-M-MC^2 does not require bulky and costly fly capacitors. Although the 5L-CHB circuit requires a minimum component quantity, the six necessary isolated DC supplies increase the system cost and converter size in the three-phase system.

The three-phase 5L-M-MC^2 system only requires one DC source. Although the ANPC-FC topology does not require clamping diodes, the voltage balance of the FC requires an additional control scheme. Assuming that the bidirectional switches are implemented by RB-IGBTs, the load current only

TABLE II

Comparison of State-of-the-Art Five-Level Topologies

Per phase leg	Typical 5L converters with different clamping types			
	Diode clamped	Cascaded H-bridge	ANPC -FC	Proposed inverter
Number of active switches	8	8	8	8
Number of clamping diodes	12	0	0	2
Number of clamping flying-capacitors	0	0	1	0
Number of DC power supplies	1	2	1	1

flows through two power devices during the switching states. However, a minimum of three power devices are involved in the flowing path in other topologies. M-MC^2 features are optimized by combining various basic multilevel clamping units.

V. Simulation and Experimental Results

To verify the validity of the proposed converter, a three-phase system is simulated in Matlab/Simulink. The simulated waveforms of the three-phase inverter are illustrated in Fig. 9. The DC input voltage is supplied by four independent 1000 V voltage sources, whereas the entire DC bus voltage reaches 4000 V. All capacitors have the same capacitance (1000 μF). A three-phase series R-L load is connected to the AC side with Ro=100 Ω and Lo=10mH. The fundamental frequency is set to 50 Hz, whereas the modulation frequency is 5 kHz. The modulation index (M) is set to 0.95. Fig. 10 shows the line-to-line voltage v_{AB} in 40 ms.

The line-to-line voltage is close to the sinusoidal waveform because it has nine voltage levels. Fig. 10 shows the voltage stress of the main power devices. The voltage rating of S_{a1} and S_{a2} is $V_d/2$ or $V_d/4$. The maximum blocking voltage for active switches S_{a1} and S_{a2} is half of V_d .The voltage stress of the bidirectional switches is $V_d/4$ or $V_d/8$, whereas the maximum voltage stress is only one quarter of V_d. The output line-to-line voltage decreases from nine levels to three levels when the modulation index in the proposed 5L-M-MC^2 changes from 1 to 0. Fig. 11 shows the total THD and output voltage level for line-to-line voltage with different values of M.

A prototype of the three-phase converter is built and tested with the proposed topology. The T-type 3-L module is F3L80R12W1H3_B11 from Infineon, and the clamping diode is the SKKD_75F12 diode module from SEMIKRON. The prototype is controlled by a digital signal processing board from TI (TMS320F28335). The DC input voltage is supplied by four independent voltage sources of 17 V, and

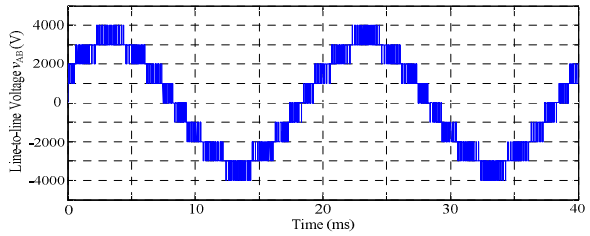


Fig. 9. Line-to-line voltage v_{AB} for 5L-M-MC^2 (M=0.95).

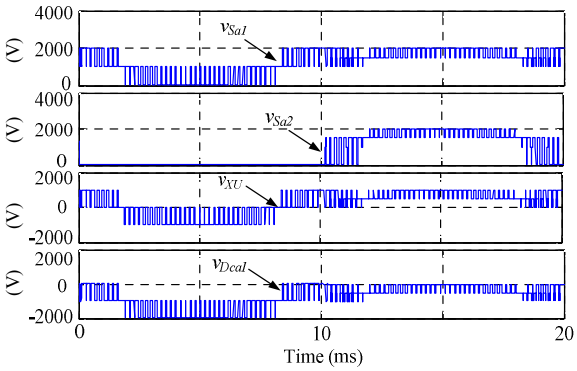


Fig.10. Voltage stress of the main devices in the single phase leg.

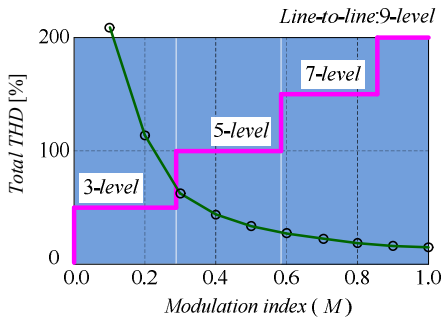


Fig. 11. Simulated THD of line-to-line voltage with modulation index.

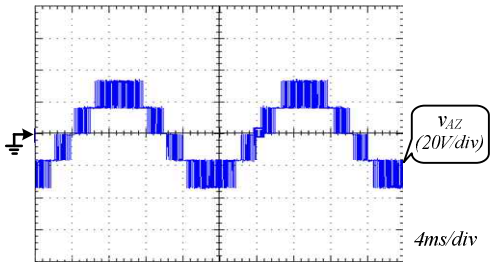
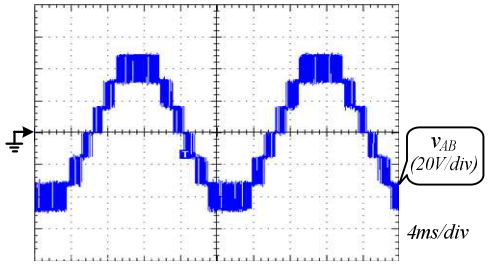
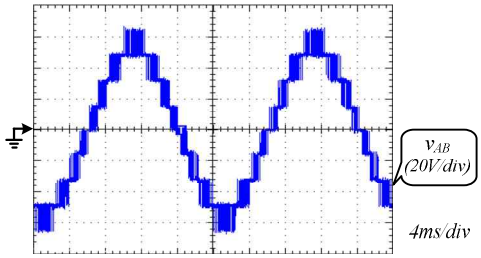


Fig.12. Experimental results of phase voltage v_{AZ} with f_o=50Hz.



(a)



(b)

Fig. 13. Experimental results of line-to-line voltage v_{AB} for f_o = 50 Hz: (a) voltage waveforms of v_{AB} in M = 0.8, (b) voltage waveforms of v_{AB} in M = 0.95.

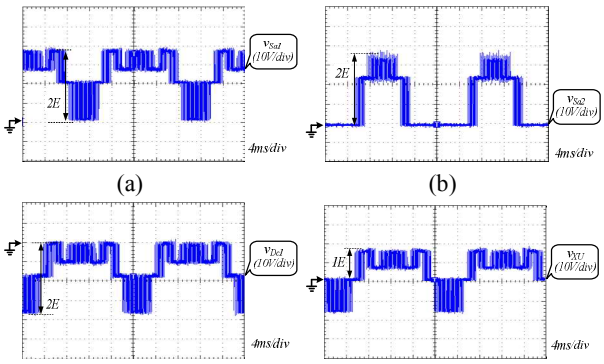


Fig. 14. Experimental results of main power devices: (a) voltage waveforms of switch S_{a1}, (b) voltage waveforms of switch S_{a2}-, (c) voltage waveforms of diode D_{ca1}, (d) voltage waveforms of bidirectional switch S_{ca1}/S_{ca3}.

each series capacitor has the same capacitance of 1410 μF. The output frequency is set as 50 Hz, whereas the modulation frequency is 5 kHz. The dead time is set to 2 μs. Fig. 12 shows the experimental results of the single-phase voltage v_{AZ} for M = 0.8. The phase output voltage has five levels. Fig. 13(a) shows that the measured line-to-line voltage v_{AB} has seven output levels for M = 0.8. Fig. 1(b) shows that the line-to-line voltage v_{AB} contains nine levels for M = 0.95.

Fig. 14 shows the measured voltage stress of the main power devices. Figs. 14(a) to 14(c) show the voltage waveforms of switches S_{a1}, S_{a2}, and D_{ca1}, respectively. The maximum voltage stress of the main power devices is half of the dc voltage, which is 2E. The main devices have the same voltage stresses as NPC-3L. Fig. 14(d) shows that the maximum value of v_{XU} across S_{ca1}/S_{ca1} is V_d/4, which implies that the bidirectional switches are achieved by low-voltage power devices. The experimental results are consistent with the simulated results in Figs. 12 to 14. Consequently, the simulated and experimental results confirm the validity of the proposed topology.

VI. Conclusions

This study proposes 5L-M-MC^2 for multilevel converters. A streamlined topology can be generated though the organic composition of two or more basic units by reusing power

devices. An advanced 5L-M-MC^2 with a simplified structure is derived from two 3L-T type modules and one diode module. The operational principle and PWM modulation are analyzed in detail. The proposed 5L-M-MC^2 is compared with other state-of-the-art topologies to present its advantages. Simulation and experimental results verify the feasibility of the derived 5L-M-MC^2. Future works could focus on the balancing of capacitor voltage and its future applications.

ACKNOWLEDGMENT

This work is sponsored by the National Basic Research Program of China (973Program 2014CB247400) and the National Nature Science Foundations of China (51361130150, 51222702).

REFERENCES

[1] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2553-2580, Aug. 2010.

[2] H. Abu-Rub, J. Holtz, J. Rodriguez, and B. Ge, "Medium-voltage multilevel converters – State of the Art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2581-2596, Aug. 2010.

[3] J. Rodriguez, S. Bernet, P. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," *IEEE Trans. Ind. Electron.* Vol. 57, No. 7, pp. 2219-2230, Jul. 2010.

[4] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family, " *IEEE Trans. Ind. Electron*. , Vol. 52, No. 7, pp. 662-669, Jun. 2005.

[5] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 6 , pp. 2930-2945, Dec. 2007.

[6] Y. Xue and M. Manjrekar, "A new class of single-phase multilevel inverters," in *Proc. IEEE PEDG* , pp. 565-571, 2010.

[7] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, Vol.57, No.7, pp. 2197-2206, Jul. 2010.

[8] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, Vol. IA-17, No. 5, pp. 518-523, Sep./Oct. 1981.

[9] C. Dietrich, S. Gediga, M. Hiller, R. Sommer, and H. Tischmacher, "A new 7.2kV medium voltage 3-Level-NPC inverter using 6.5kV-IGBTs," in *Proc. Eur. Power Electron*, pp. 1-9, 2007.

[10] K. Komatsu, M. Yatsu, S. Miyashita, S. Okita, H. Nakazawa, S. Igarashi, Y. Takahashi, Y. Okuma, Y. Seki, and T. Fujihira, "New IGBT modules for advanced neutral-point-clamped 3-level power converters," in *Proc. IEEE IPEC* , pp. 523-527, 2010.

[11] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, Vol.52, No.3, pp. 855-868, Jun. 2005.

[12] B. Wu, Y. Li, and S. Wei, "Multipulse diode rectifiers for high-power multilevel inverter fed drives," in *Proc. IEEE CIEP*, pp. 9-14, 2004.

[13] C. M. Wu, W. H. Lau, and H. Chung, "A five-level neutral-point-clamped H-bridge PWM inverter with superior harmonics suppression: A theoretical analysis," in *Proc. IEEE ISCAS*, pp. 198-201, 1999.

[14] P. Rodriguez, M. D. Bellar, R. S. Muñoz-Aguilar, S. Busquets-Monge, and F. Blaabjerg, "Multilevel-clamped multilevel converters (MLC2)," *IEEE Trans. Power Electron*, Vol. 27,No. 3, pp. 1055-1060, Mar. 2012.

[15] P. Zhiguo, F. Z. Peng, V. Stefanovic, and M. Leuthen, "A diode-clamped multilevel converter with reduced number of clamping diodes," in *Proc. IEEE APEC*, pp. 820-824, 2004.

[16] F. Kieferndorf, M. Basler, L. A. Serpa, J. H. Fabian, A. Coccia, and G. A. Scheuer, "A new medium voltage drive system based on ANPC-5L technology," in *Proc. IEEE* ICIT, pp. 643-649, 2010.

[17] S. K. Chattopadhyay, C. Chakraborty, and B. C. Pal, "A hybrid multilevel inverter topology with third harmonic injection for grid connected photovoltaic central inverters," in *Proc. IEEE ISIE*, pp. 1736-1741, 2012.

[18] P. Roshankumar, R. P. Rajeevan, K. Mathew, K.Gopakumar, J. I. Leon, and L. J. Franquelo, "A five-level inverter topology with single DC-supply by cascading a flying capacitor inverter and an H-bridge," *IEEE Trans. Power Electron,* Vol. 27, No. 8, pp. 3505-3512, Aug. 2012.

[19] A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells," *IEEE Trans. Power Electron*, Vol. 26, No. 1, pp. 51-65, Jan. 2011.

[20] H. Kapels and D. Drucke, "Optimized device concepts for reverse blocking IGBTs," in *Proc, IEEE ISPSD,* pp. 148-151, 2003.

[21] N. Celanovic and D. Boroyevich, "A fast space-vector modulation algorithm for multilevel three-phase converters," *IEEE Trans. Ind. Appl.*, Vol. 37, No. 2, pp. 637-641, Mar. 2001.

[22] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, Vol. 7, No. 3, pp.495-505, Jul.1992.

Haoze Luo was born in Jiangxi, China in 1986. He received his B.S. and M.S. degrees from the Department of Electrical Engineering, Hefei University of Technology, Hefei, China, in 2008 and 2011, respectively. He is currently working toward his Ph.D degree at the College of Electrical Engineering, Zhejiang University. His research interests include high-power converters and the reliability of high-power modules.

Yufei Dong was born in Shandong, China in 1990. He received his B.S. degree from the Department of Electrical Engineering, Hunan University, Changsha, China, in 2012. He is currently working toward his M.S. degree at the College of Electrical Engineering, Zhejiang University. His research interests include multilevel converters and reliability of high power modules.

Wuhua Li (*M'09*) received his B.Sc. and Ph.D. degrees in Applied Power Electronics and Electrical Engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively. From September 2004 to March 2005, he was a Research Intern, and from January 2007 to June 2008, he worked as a Research Assistant in GE Global Research Center, Shanghai, China. From July 2008 to April 2010, he joined the College of Electrical Engineering, Zhejiang University as a Post doctor. In May 2010, he became a faculty member at Zhejiang University as a Lecturer. In December 2010, he was promoted to Associate Professor. Since December 2013, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University. From July 2010 to September 2011, he was a Ryerson University Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. His research interests include high-efficiency power converters and renewable energy power conversion systems. Dr. Li has published more than 100 peer-reviewed technical papers and holds over 30 issued/pending patents. His excellent teaching and research contributions enabled Dr. Li to receive the 2011 TOP TEN Excellent Young Staff Award and the 2012 Distinguished Young Scholar from Zhejiang University, the 2012 Outstanding Young Researcher Award from Zhejiang Province, and the 2012 Delta Young Scholar from Delta Environmental & Educational Foundation. He received three Scientific and Technological Achievement Awards from the Zhejiang Provincial Government and the State Educational Ministry of China in 2009 and 2011, respectively.

Xiangning He *(M'95--SM'96--F'10)* received his B.Sc. and M.Sc. degrees from Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and his Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989. From 1985 to 1986, he was an Assistant Engineer at the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he obtained a Fellowship from the Royal Society of U.K. and subsequently conducted research in the Department of Computing and Electrical Engineering, Heriot–Watt University, Edinburgh, U.K., as a Post-Doctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University. He was the Director of the Power Electronics Research Institute and the Head of the Department of Applied Electronics, and he is currently the Vice Dean of the College of Electrical Engineering, Zhejiang University. His research interests are power electronics and their industrial applications. He is the author or co-author of more than 280 papers and one book, "Theory and Applications of Multi-level Converters." He holds 22 patents. Dr. He received the 1989 Excellent Ph.D. Graduate Award, the 1995 Elite Prize Excellence Award, the 1996 Outstanding Young Staff Member Award, and 2006 Excellent Staff Award from Zhejiang University for his teaching and research contributions. He received seven Scientific and Technological Achievement Awards from the Zhejiang Provincial Government and the State Educational Ministry of China in 1998, 2002, 2009 and 2011 respectively, as well as six Excellent Paper Awards. Dr. He is a Fellow of The Institute of Electrical and Electronics Engineers (IEEE). He was appointed an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011. He is also a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.