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Carrier Phase-Shift PWM to Reduce Common-Mode Voltage for Three-Level T-Type NPC Inverters

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Abstract

Common-mode voltage (CMV) causes overvoltage stress to winding insulation and damages AC motors. CMV with high *dv/dt* causes leakage currents, which create noise problems for equipment installed near the converter. This study proposes a new pulse-width modulation (PWM) strategy for three-level T-type NPC inverters. This strategy substantially eliminates CMV. The principle for selecting suitable triangle carrier signals for the three-level T-type NPC is described. The proposed method can mitigate the peak value of CMV by 50% compared with the phase disposition pulse-width modulation method. Furthermore, the proposed method exhibits better harmonic spectrum and lower root mean square value for the CMV than those of the reduced-CMV method on the basis of the phase opposition disposition PWM scheme with modulation index higher than 0.5. The proposed modulation can easily be implemented using software without any additional hardware modifications. Both simulation and experimental results demonstrate that the proposed carrier phase-shift PWM method has good output waveform performance and reduces CMV.

Key words: Common-mode voltage, Phase disposition PWM, Phase opposition disposition PWM, Sinusoidal PWM, Three-level inverter, T-type NPC

I. INTRODUCTION

Interest in multilevel topologies has been increasing because of the many possibilities in power electronics applications, such as in the military, e-vehicles, and renewable energy. Multilevel converters synthesize output voltage from more than two voltage levels. Therefore, the spectrum of the output signal is significantly improved when compared with that of classical two-level converters. The multilevel inverter reduces voltage constraints on switches while lowering the total harmonic distortion (THD) of output voltages [1]-[5]. The main drawback of multilevel converters is the number of switches, which increases with the number of levels.

Multilevel inverters are classified into three groups: neutral-point-clamped (NPC) inverters, floating point capacitor inverters, and cascade H–bridge inverters, with NPC inverters being the most widely used [6]-[8]. Recently, T-type NPC (T-NPC) inverters have been proposed as more efficient alternatives to traditional NPC inverters [9], [10]. Until recently, multilevel NPC inverters have received considerable attention for commercial applications, and many researchers have focused on improving the output performance while reducing the power losses, the number of power switches, and the common-mode voltage (CMV) of such converters [11]-[15]. Previous research deemed CMV reduction to be important in extending the lifetime of electrical equipment.

CMV attributed to high-speed pulse-width modulation (PWM) in power converters introduces numerous problems

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within an electrical system. CMW is the main source of early motor-winding failure, bearing deterioration, and wide-band electromagnetic interference. Reducing the CMV within the power converter is important. Two main solutions used to reduce CMV have been presented in previous research. One solution is based on the use of additional hardware, such as passive filters, active cancellers, or electromagnetic interference filters, to mitigate CMV [16], [17]. However, this method introduces increased converter volume, weight, and cost. Another solution is to investigate the modulation technique. Using suitable PWM, mitigating the CMV is achievable within the power converter. Several studies have proposed CMV reduction for NPC topology by applying the appropriate modulation techniques. However, these methods focus on the SVPWM method, which has several disadvantages [18], [19]. This method requires complex calculations and tables to synthesize the reference output voltage. In [20]-[22], the phase opposition disposition (POD) was proposed to reduce CMV for NPC. However, this method has high THD in the output voltage, a high RMS value, and a poor harmonics spectrum in the CMV.

To overcome the drawbacks of phase disposition (PD) PWM and POD PWM schemes, this study proposes a novel carrier-based PWM method for use with T-NPC to eliminate CMV. The proposed strategy uses three-phase carriers of the same frequency with a phase difference of 120°. The proposed method is simple to implement and does not require any additional hardware. The advantages of the proposed method are as follows:

- Eliminates the peak value of the CMV, and the magnitude is reduced by 50% compared with that when using the conventional PD PWM scheme.
- Exhibits better harmonic spectrum for CMV and reduces the RMS of CMV when with the conventional POD PWM scheme.

The remainder of this paper is organized as follows: The three-level T-type NPC operation and the effect of the switching state on CMV are described in Section II. The conventional PD and POD schemes are also presented in this section. The proposed method is presented in Section III. The simulation and experimental results are provided in Sections IV and V, respectively. Study conclusions are provided in the final section.

II. CMV Analysis and Conventional Methods

A. Three-Level T-Type NPC Inverter Topology

The three-level T-type NPC inverter topology is illustrated in Fig. 1. Each leg of the TNPC consists of four power-switch devices: IGBT1X and IGBT4X (X = A,B,C) are connected to the positive and negative poles of the dc power supply, respectively, and one bidirectional switch (IGBT2X and IGBT3X) connects the middle point of the dc-link to the load. The three-level T-type NPC topology is simpler than that of conventional NPC and provides some advantages that are unavailable in conventional NPC, such as low conduction losses, fewer power switches, and small size [9], [10].

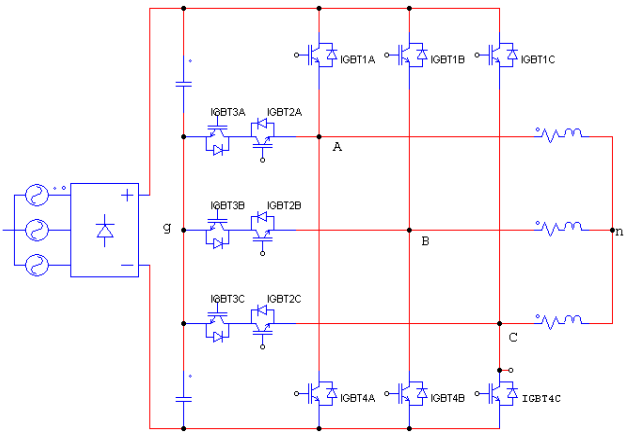


Fig. 1. Three-level T-NPC Inverter topology.

TABLE I
Switching States of the T-NPC

Switching State S_X	Switching Status				Output Voltage
	IGBT1X	IGBT2X	IGBT3X	IGBT4X	V_{Xg}
+1	ON	ON	OFF	OFF	$V_{dc}/2$
0	OFF	ON	ON	OFF	0
-1	OFF	OFF	ON	ON	$-V_{dc}/2$

The switching states of the power switches and the output voltage of the three-level T-Type NPC are shown in Table I. The three phase levels of common point voltage that can be generated on each phase leg are $+V_{dc}2$, 0, and $-V_{dc}/2$, where V_{dc} is the dc-link voltage, and X represents each phase (X = A, B, or C).

B. Common-Mode Voltage Analysis

The CMV of the three-level T-Type NPC is defined as the voltage between load neutral point *n* and the mid-point of dc-link voltage *g*, as shown in Fig. 1. We assumed that the three-phase RL load is balanced. The CMV is derived from the following equations:

$$\begin{aligned} v_{Ag} &= v_{ng} + R_A i_A + L_A \frac{di_A}{dt} \\ v_{Bg} &= v_{ng} + R_B i_B + L_B \frac{di_B}{dt} \\ v_{Cg} &= v_{ng} + R_C i_C + L_C \frac{di_C}{dt} \end{aligned} \quad (1)$$

where v_{Ag}, v_{Bg}, and v_{Cg} are the three phase output voltages with respect to ground point *g*; and i_A, i_B, and i_C are the three phase output currents.

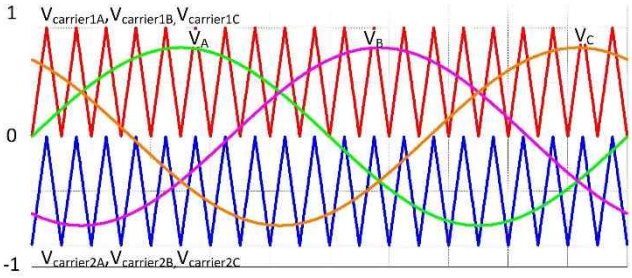


Fig. 2. Carrier and reference waveforms for three-level T-NPC inverter using PD PWM scheme.

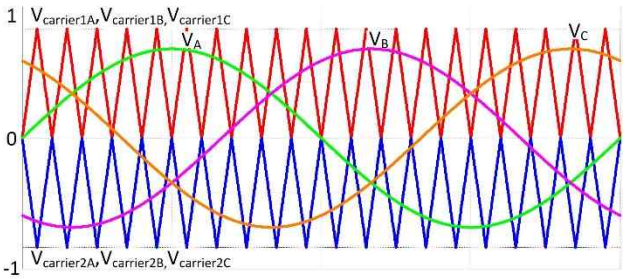


Fig. 3. Carrier and reference waveforms for three-level T-NPC inverter using POD PWM scheme.

Given that the three-phase load is balanced, the CMV becomes

$$v_{ng} = \frac{1}{3}\left(v_{Ag} + v_{Bg} + v_{Cg}\right). \tag{2}$$

The CMV depends on the switching states of the three-level T-type NPC inverter and can be determined using the following switching functions:

$$V_{ng} = \frac{V_{dc}}{6}\left(S_A + S_B + S_C\right) \tag{3}$$

Eq. (3) and Table I show that the CMV has seven values: 0, $\pm V_0/6$, $\pm V_0/3$, and $\pm V_0/2$. They are provided in detail in Table II. Regardless of the AC source, the CMV is determined by the output voltages, which depend only on the switching states of the three-level T-type NPC inverter.

C. Conventional Methods

1) Phase Disposition (PD) PWM Scheme: The PD PWM scheme is used in the carrier-based implementation [15],[16]. Fig. 2 shows the basic principle of the PD PWM scheme using double triangle carrier signals. The upper carrier signal ($V_{carrier1X}$) is used to generate the gate signal for switch IGBT1X, IGBT3X. The lower carrier signal ($V_{carrier2X}$) is used to generate the gate signal for the switch IGBT2X, IGBT4X. Two carrier waveforms are arranged so that every carrier is in phase; one is above zero and the other is below zero.

2) Conventional Reduced-CMV Method Based on Phase Opposition Disposition PWM Scheme: For POD schemes, the three carrier signals above zero are in phase, and the three carrier signals below zero are also in phase. However, the upper carrier signal and the lower carrier signal are in opposite phase, as shown in Fig. 3.

TABLE II
CMV ACCORDING TO SWITCHING STATES

Switching state ($S_AS_BS_C$)	CMV
000,-101,10-1,01-1, 0-11,1-10,-110	0
111	$V_{dc}/2$
-1-1-1	$-V_{dc}/2$
110, 101, 011	$V_{dc}/3$
-1-10, -10-1, 0-1-1	$-V_{dc}/3$
1-1-1,11-1,-11-1, -100,0-10,00-1	$-V_{dc}/6$
11-1,1-11,-111, 100,010,001	$V_{dc}/6$

As shown in Figs. 3 and 4, the upper triangle magnitude is normalized from 1 to 0, and the lower triangle magnitude is normalized from −1 to 0.

III. PROPOSED CARRIER PHASE-SHIFT PWM METHOD FOR CMV REDUCTION

Table II shows that by employing 19 switching states (000, −101, 10-1, 01-1, 0-11, 1-10, −110, 1-1-1, 11-1, −11-1, −100,0-10,00-1, 11-1, 1-11, −111, 100,010,001) to synthesize the reference output voltage, the peak value of CMV is limited at $V_{dc}/6$.

We assume that the normalized three-phase reference outputs are given as

$$V_A = m\sin\left(\omega t\right) \tag{4}$$

$$V_B = m\sin\left(\omega t - \frac{2\pi}{3}\right) \tag{5}$$

$$V_C = m\sin\left(\omega t + \frac{2\pi}{3}\right), \tag{6}$$

where m is the modulation index, and ω is the input angular frequency.

Two conditions are possible for the six different situations when the three phase output voltages are balanced. In the first condition, two input phase voltages are positive, and one phase voltage is negative. In the second condition, two input phase voltages are negative, and one phase voltage is positive. Without losing the generality of the analysis, we assume that the output voltage of Phase A is positive and the output voltages of Phases B and C are negative, as shown in Fig. 3. Therefore, the possible switching states for Phase A are 1 or 0, and the possible switching states for Phases B and C are 0 or −1. Fig. 4 shows that the switching state (0-1-1) causes the CMV to be at $-V_{dc}/3$. Thus, to reduce the CMV peak, we must avoid using this switching state to synthesize the reference output voltages. Two carrier signals are used in the conventional PD and POD methods. In this study, carrier phase-shift PWM is proposed based on six carrier signals that are used to generate a gating pulse for the three-level T-type NPC.

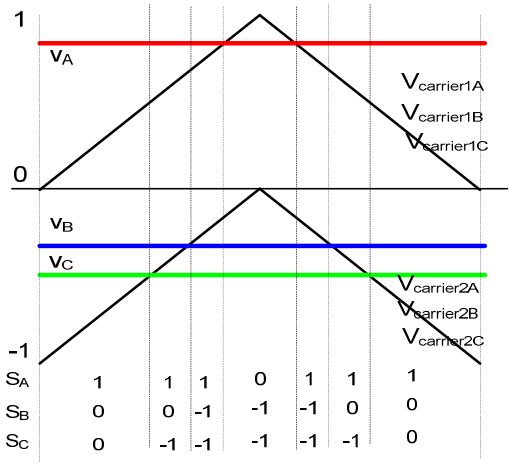


Fig. 4 Reference output voltage, triangle carrier signals, and switching states of the conventional PD PWM method.

The proposed carrier phase shift is developed based on the conventional PD PWM method. According to Table II, the peak CMV can be reduced from $V_{dc}/2$ to $V_{dc}/6$ if the switching states 111, −1-1-1, 110, 101, 011, −1-10, −10-1, and 0-1-1 are not used.

Given that the input voltages are balanced as shown in Eq. (7), two other conditions are possible: (1) Two input phase voltages are positive and one phase voltage is negative; and (2) Two input phase voltages are negative and one phase voltage is positive.

$$V_A + V_B + V_C = 0 \tag{7}$$

Without losing the generality of the analysis, we assume that $V_A > 0,\ V_B < 0,\ V_C < 0$. Table II and Fig. 1 shows that the switching stage becomes 0-1-1 and it causes the peak CMV to become higher than $V_{dc}/6$.

The relationship between the reference output voltage and the carrier signals are given in Eq. (8) for the switching state 0-1-1.

$$\begin{aligned} 0 < V_A < V_{carrier1A} \\ V_B < V_{carrier2B} < 0 \\ V_C < V_{carrier2C} < 0 \end{aligned} \tag{8}$$

From Fig. 2, the relationship between the upper and lower carrier signals is

$$V_{carrier1B} - V_{carrier2B} = 1; V_{carrier1C} - V_{carrier2C} = 1 \tag{9}$$

Substituting Eq. (9) into Eq. (8), we have

$$\begin{aligned} 0 < V_A < V_{carrier1A} \\ V_B < V_{carrier1B} - 1 < 0 \\ V_C < V_{carrier1C} - 1 < 0 \end{aligned} \tag{10}$$

From Eqs. (8) and (10), we can obtain Eq. (11):

$$0 < V_A + V_B + V_C < V_{carrier1A} + V_{carrier1B} + V_{carrier1C} - 2 \tag{11}$$

Therefore,

$$V_{carrier1A} + V_{carrier1B} + V_{carrier1C} > 2 \tag{12}$$

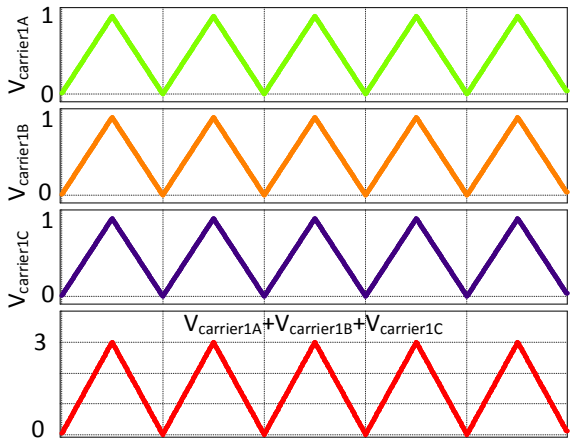


Fig. 5. Carrier waveforms for three-level T-type NPC inverter using PD PWM scheme.

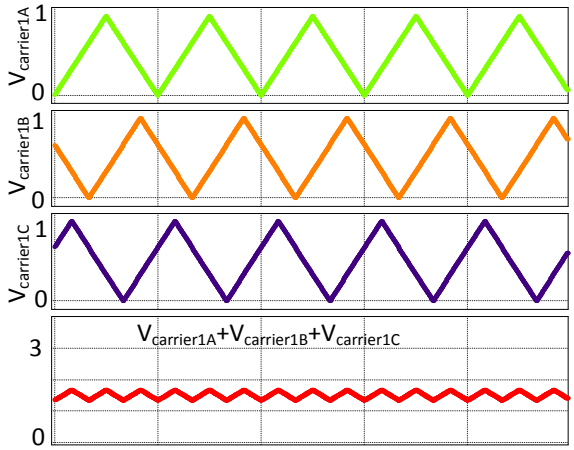


Fig. 6. Carrier waveforms for three-level T-type NPC inverter using proposed carrier phase shift PWM scheme.

To reduce CMV, the state 0-1-1 must be avoided. Therefore, the relationship between three carrier signals has to fully meet Eq. (13).

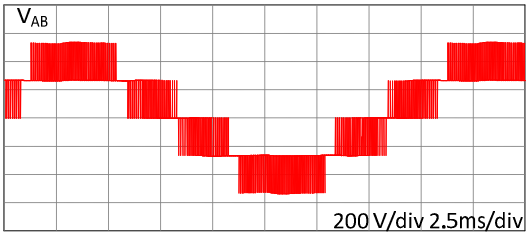
$$V_{carrier1A} + V_{carrier1B} + V_{carrier1C} < 2 \tag{13}$$

Fig. 5 shows the three upper carrier signals for legs A, B, and C through the conventional SPWM method. The sum of the three carrier signals is larger than 2. Therefore, a peak CMV with the value $V_{dc}/3$ is obtained.

If the three carrier signals for Phases A, B, and C are chosen with a displacement of 120°, as shown in Fig. 6, the sum of the three carrier signals is less than 2. Thus, the maximum CMV is $V_{dc}/6$. In the proposed carrier phase-shift method, the upper carrier signal and lower carrier signals for each leg are in phase. However, three upper and lower carrier signals for legs A, B, and C are out of phase by 120°.

IV. Simulation Results

We conducted simulations using PSIM 9.0 software to verify the effectiveness of the new SVM method. The system is simulated with the following parameters:



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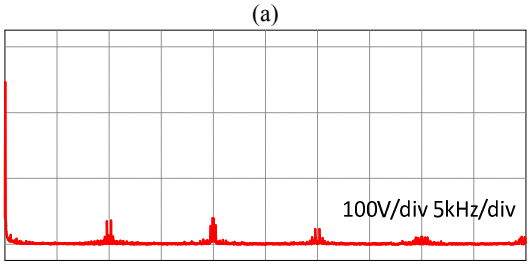

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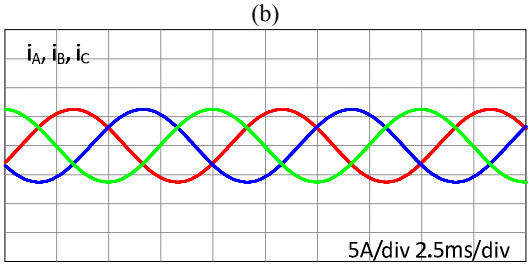
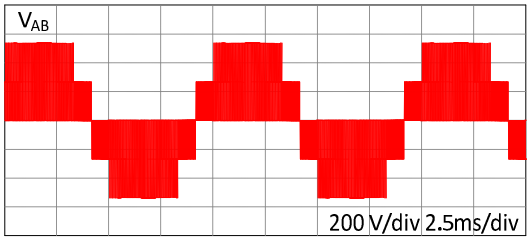


(c)

Fig. 7 (a) Line-to-line output voltage. (b) FFT of line-to-line output voltage. (c) Three phase output currents using the PD PWM method.



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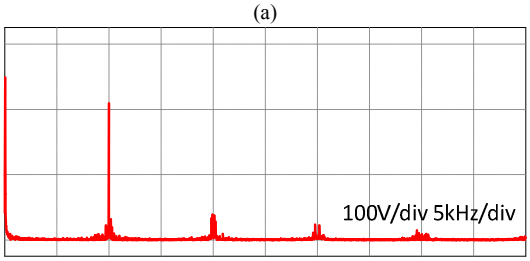

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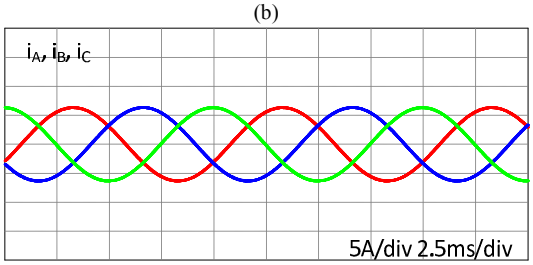


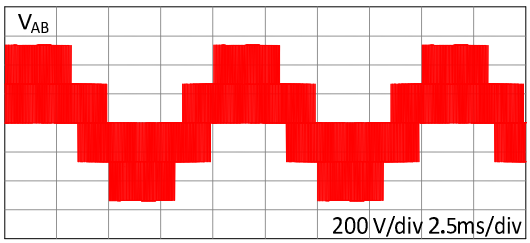
(c)

Fig. 8 (a) Line-to-line output voltage. (b) FFT of line-to-line output voltage. (c) Three phase output currents using the POD PWM method.

- Dc-link voltage V_{dc} = 530 V
- Three-phase RL load: R = 30 Ω, L = 15 mH
- Modulation index m = 0.8
- Output frequency: f_{out} = 50 Hz
- PWM frequency = 10 kHz

Figs. 7 to 9 show the line-to-line output voltage, its FFT, and the three-phase output currents for the modulation index m = 0.8 and output frequency 50 Hz using the PD, POD, and PWM schemes, respectively. The proposed PWM method provides the same sinusoidal output currents as those of the other PWM methods. The different output voltage waveforms result from different modulation methods. The fast Fourier transform (FFT) results of the line-to-line output voltage show fewer harmonics for the proposed method than for the conventional reduced-CMV-based POD method. However, the THD of the line-to-line output voltage with the proposed method slightly increases compared with that of the conventional PD PWM method.

Figs. 10 to 12 show the CMV waveforms and their FFT analysis when employing the PD, the conventional reduced-CMV-based POD method, and the proposed method, respectively, at an output frequency of 50 Hz and a modulation index of 0.8. The conventional reduced-CMV-based POD method and the new carrier phase-shift method provide the same CMV peak value (88 V). Fig. 10 shows the CMV pulses of magnitude $V_{dc}/3$ (177 V)



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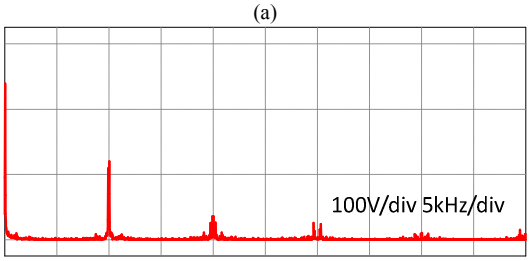

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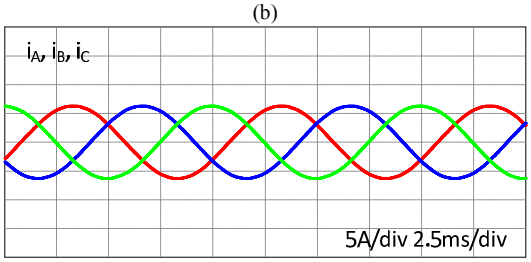
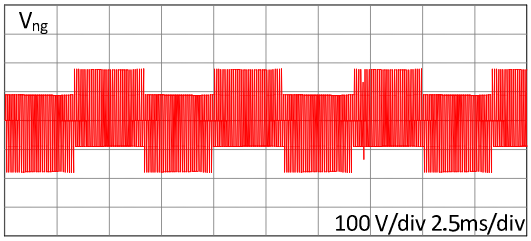


(c)

Fig. 9. (a) Line-to-line output voltage. (b) FFT of line-to-line output voltage. (c) Three phase output currents using the proposed carrier phase-shift PWM method.



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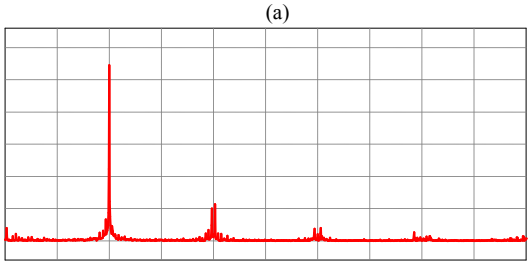

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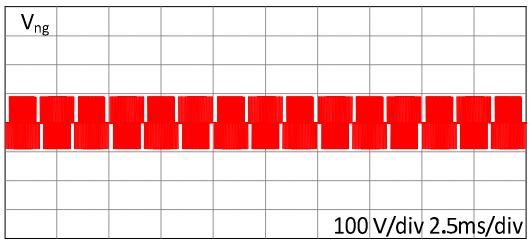
Fig. 10. (a) Common-mode voltage. (b) FFT using the PD PWM method with m = 0.8 and f_{out} = 50 Hz.



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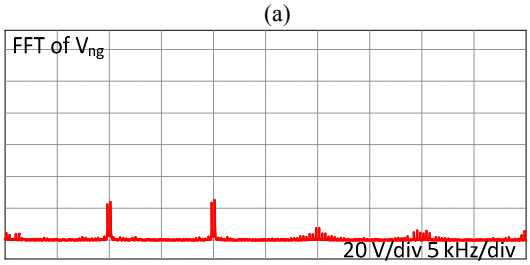


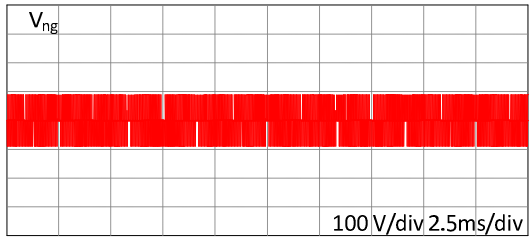
(b)

Fig. 11. (a) Common-mode voltage. (b) FFT using the POD PWM method with m = 0.8 and f_{out} = 50 Hz.

when the PD method is applied. Compared with the conventional PD method, the proposed method significantly reduces the CMV peak value by 50%. Furthermore, the spectrum analysis of the CMV shows that the CMV of the proposed PWM scheme contains fewer harmonic components compared with the conventional PD and POD PWM schemes.

V. Experimental Results

To validate the proposed theories and simulations, we designed an experimental setup in the laboratory. The experimental prototype is shown in Fig. 13. The half-bridge IGBT modules SEMiX202GB128Ds (1,200 V) were selected for switch pairs IGBT1X, IGBT4X. The bidirectional IGBT modules SK60GM123 (1,200 V) were chosen for the switch pairs IGBT2X, IGBT3X. The prototype is controlled with the use of a high-performance, floating-point digital signal



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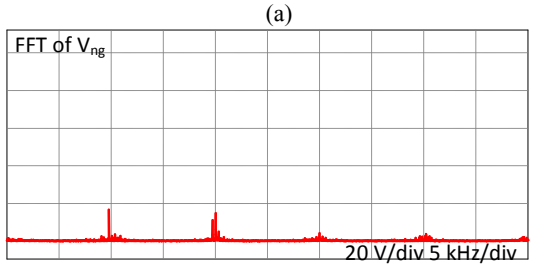


(b)

Fig. 12. (a) Common-mode voltage. (b) FFT using the proposed PWM method with m = 0.8 and f_{out} = 50 Hz.

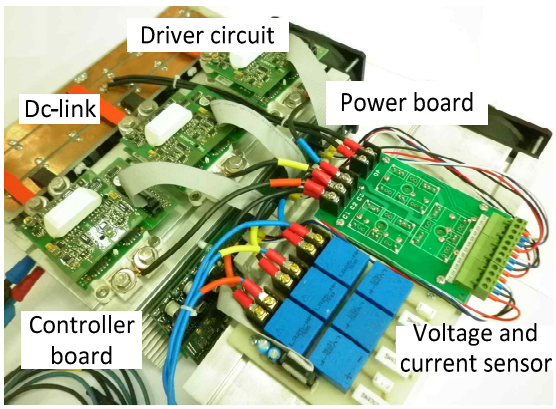
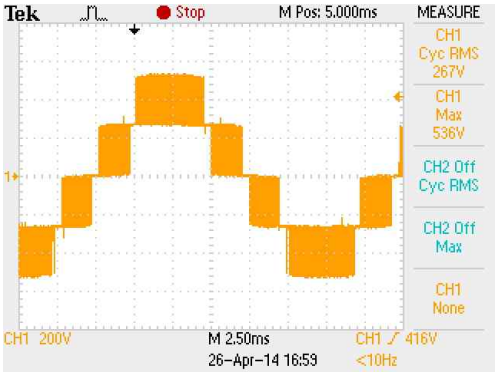


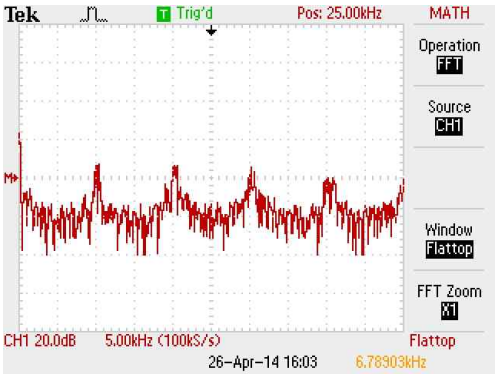
Fig. 13. Laboratory T-NPC prototype.

processor (DSP) 90 MHz TMS320F28069 from Texas Instruments. The parameters used in the experiment are the same as in the simulation. The PWM operates at 10 kHz.

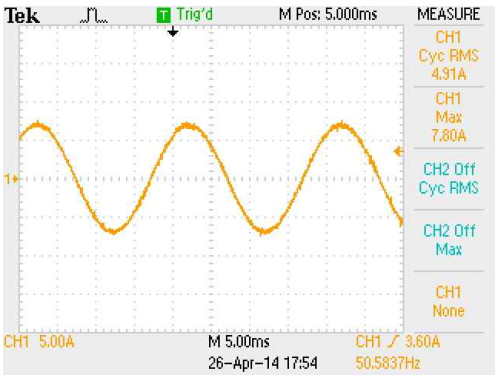
Figs. 14 to 16 show the experimental results for the line-to-line output voltage, its FFT, and the output currents of the conventional PD, POD, and proposed PWM methods, respectively. Every method provides almost pure sinusoidal output currents, and the proposed PWM method does not decrease the performance of the output currents. The spectrum and phase output voltage are comparable to the output performance for the two conventional methods and the proposed carrier phase-shift PWM method. Figs. 14b, 15b, and 16b show the harmonic spectrum of the output line-to-line voltage for the three PWM methods. The spectrums indicate that the proposed PWM method has good output voltage compared with the conventional reduced-CMV-based POD method. However, the proposed method has several drawbacks. The performance of the output voltage using the proposed method is worse than that of the PD PWM method and exhibits a trade-off between CMV reduction and output voltage performance.



(a)

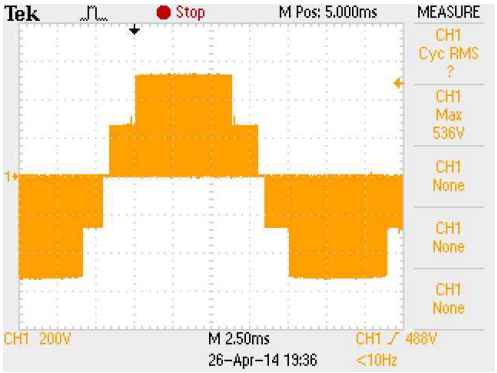


(b)

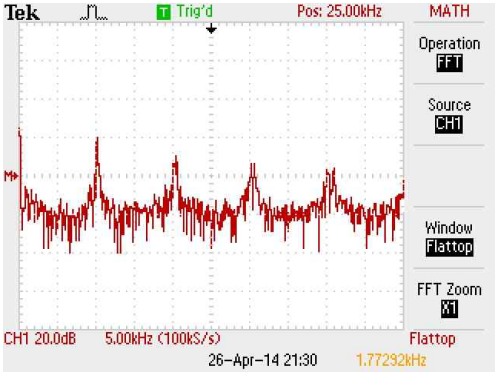


(c)

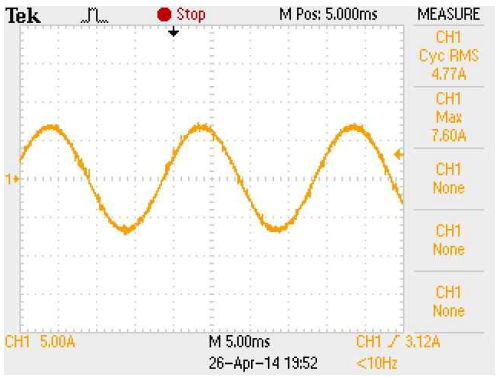
Fig. 14. (a) Line-to-line output voltage. (b) FFT of line-to-line output voltage. (c) Output current at an output frequency of 50 Hz and a modulation index of m = 0.8 using the PD method.



(a)



(b)

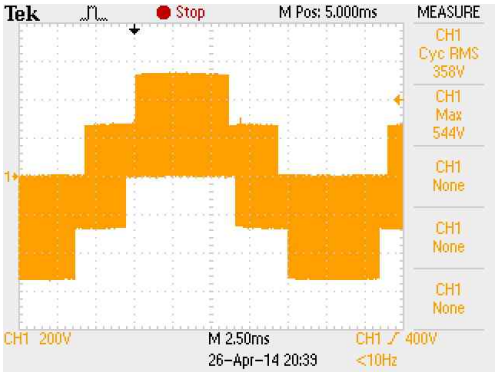


(c)

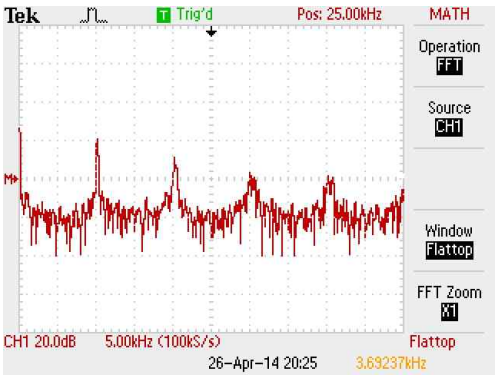
Fig. 15. (a) Line-to-line output voltage. (b) FFT of line-to-line output voltage. (c) Output current at an output frequency of 50 Hz and a modulation index of m = 0.8 using the POD method.

Fig. 17 shows the CMV waveforms of the three-level T-type NPC inverter when the PD PWM method is applied. The peak value of the CMV is achieved at 177 V, which corresponds to $V_{dc}/3$. Figs. 18 and 19 show the CMV of the three-level T-type NPC inverter when the conventional reduced-CMV method (POD method) and the proposed method are used, respectively. The two methods reduce the peak value of CMV. The peak value of CMV decreases from 177 V to 86 V, which corresponds to $V_{dc}/6$. Compared with the conventional PD method, the proposed method significantly reduces the CMV peak value by 50%. According to an FFT of the CMV, the new SVM method generates a smaller harmonic component than that of the PD PWM method.

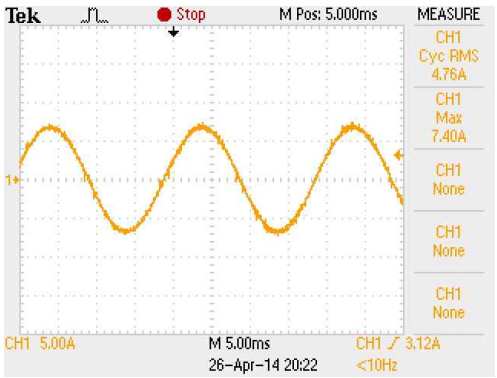
The performance of the proposed PWM method has been also tested by considering low modulation index and low frequency. The CMV with PD, POD, and the proposed carrier phase shift PWM methods at f=30Hz, m=0.6, and f=20Hz, m=0.3 are shown in Figs. 20 and 21, respectively. The POD and carrier phase shift PWM methods provides a 50% reduction in the CMV (peak value) compared with the conventional PD PWM method. Fig. 22 shows the RMS value of the CMV with the PD, POD, and the proposed PWM methods according to the modulation index. Compared with the conventional reduced CMV–POD PWM method, the proposed method provides a lower RMS value for the CMV



(a)

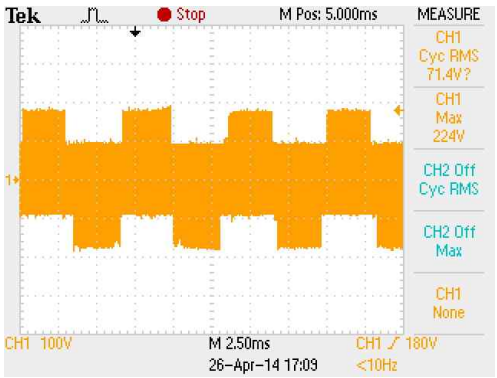


(b)

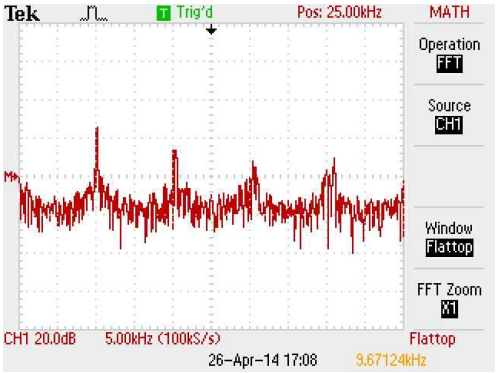


(c)

Fig. 16. Experimental results of (a) Line-to-line output voltage. (b) FFT of line-to-line output voltage. (c) Output current at an output frequency of 50 Hz and a modulation index of m = 0.8 using the proposed PWM method.

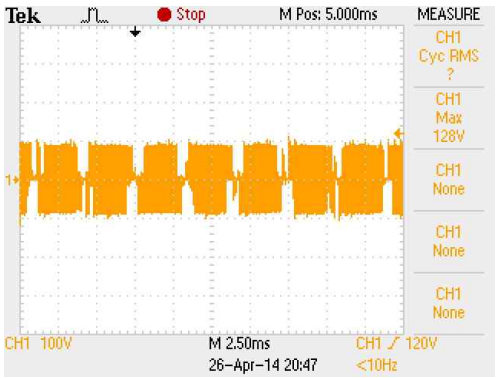


(a)

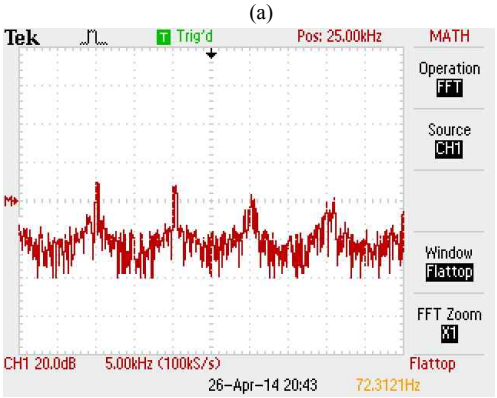


(b)

Fig. 17. (a) CMV waveforms and (b) its FFT with PD method at an output frequency of 50 Hz and a modulation index of m = 0.8.

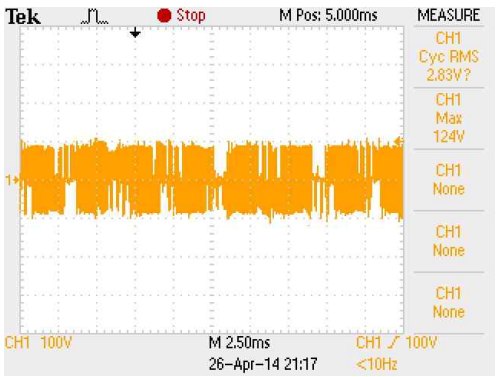


(a)

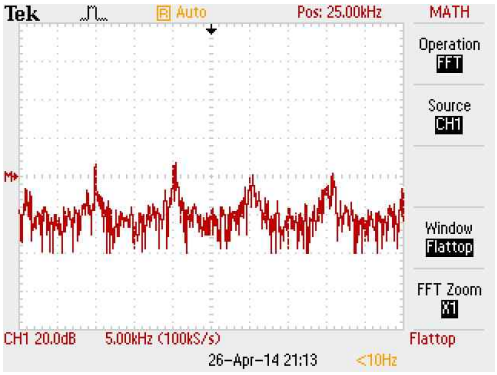


(b)

Fig. 18. (a) CMV waveforms. (b) Its FFT with POD method at an output frequency of 50 Hz and a modulation index of m = 0.8.

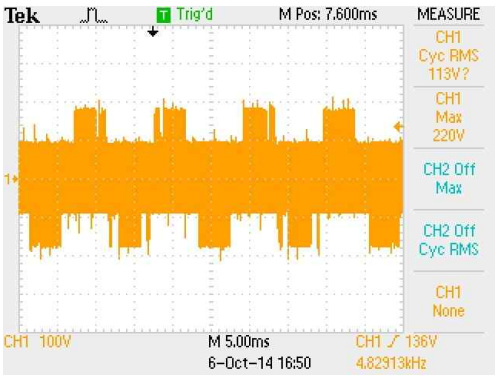


(a)

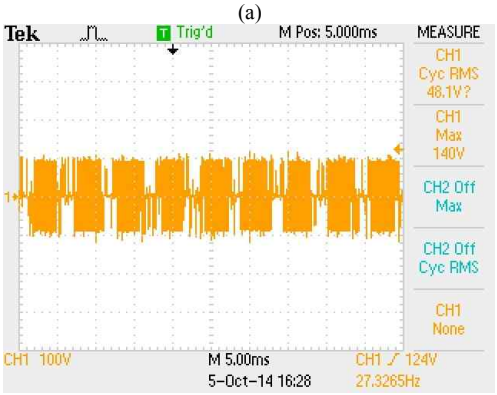


(b)

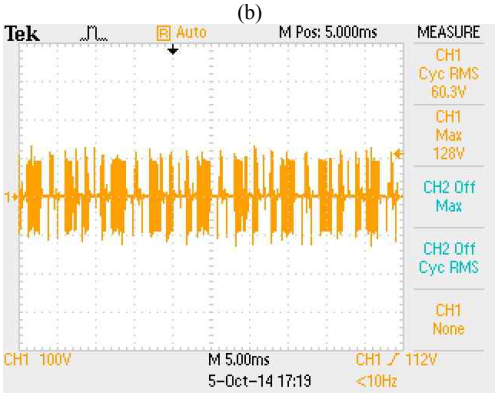
Fig. 19. (a) CMV waveforms. (b) Its FFT with proposed method at an output frequency of 50 Hz and a modulation index of m = 0.8.



(a)

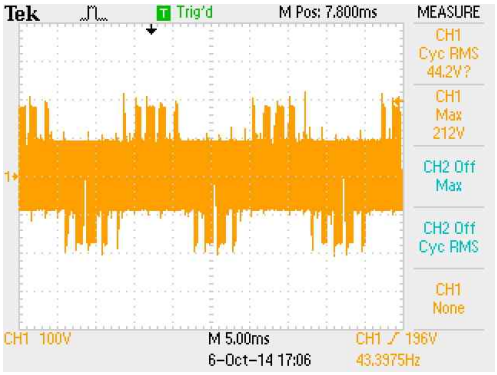


(b)

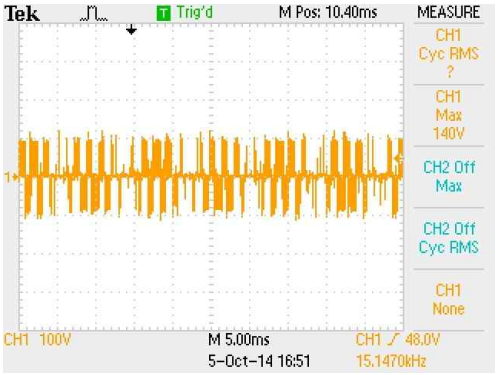


(c)

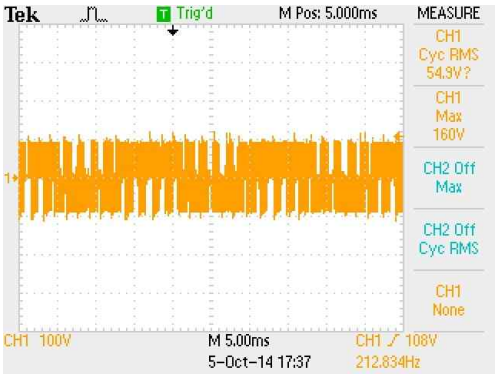
Fig. 20. CMV waveforms. (a) PD PWM. (b) POD PWM methods. (c) The proposed method at an output frequency of 30 Hz and a modulation index of m = 0.6.



(a)



(b)



(c)

Fig. 21. Experimental result of CMV waveforms. (a) PD PWM. (b) POD PWM methods. (c) The proposed method at an output frequency of 20 Hz and a modulation index of m = 0.3.

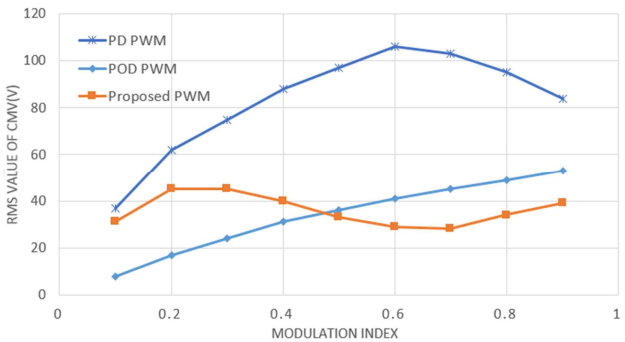


Fig. 22. Comparison with the RMS values for different CMV.

at the modulation index higher than 0.5. However, at a lower modulation index, the RMS value of the CMV with the proposed method becomes higher than that using the POD PWM method. Thus, using a combined PWM algorithm that uses the proposed POD PWM method with a low modulation index as well as using the proposed method at high modulation index to control full output voltage range is recommended.

VI. CONCLUSIONS

A carrier phase-shift PWM method is proposed in this study to reduce CMV for three-level T-type NPC inverters. The proposed method achieves a peak value of CMV, which is reduced by 50% compared with that of the conventional PD PWM method. The proposed method has a lower RMS value of CMV than the POD PWM method at a modulation index higher than 0.5. The proposed method is implemented simply, and no additional computations are needed beyond those of conventional PD and POD PWM schemes. Finally, experimental results have been provided to verify the theoretical analysis and simulation results.

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