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Half Load-Cycle Worked Dual Input Single Output DC/AC Inverter

Rong Chen† and Jia-Sheng Zhang*

†*College of Information and Control Engineering, China University of Petroleum (Huadong), Qingdao, China

Abstract

A novel half load-cycle worked dual input single output (DISO) DC/AC inverter is presented. The basic circuit consists of a dual buck regulator, which works in continuous current mode. The working principle of DISO DC/AC inverter has been used. The control method applied for half load-cycle worked DISO DC/AC inverter has been studied. The control effects of the open-loop proportional control and closed-loop proportional-integral control are compared by using PSIM software. The parameters are adopted in the realistic simulation and experiment test. Moreover, the waveforms, such as voltage of modulation reference signal and output voltage, were given. The simulation and experiment results proved that the half load-cycle worked DISO DC/AC inverter could achieve good performance, gain a line frequency of 50 Hz, and verify the correctness of theoretical analysis.

Key words: Buck regulator, Dual input single output, Half load-cycle worked, SPWM

I. INTRODUCTION

DC/AC inverter is a static inverter that takes power from a DC voltage source or DC current source as well as delivers power to a load by using power electronic devices. The output variable is a low-distortion AC voltage or AC current of single-phase or multi-phase, which is utilized to meet load power requirements [1]. As a branch of DC/AC inverter, the single-phase full-bridge DC/AC inverter for interfacing with the grid is needed with the increased penetration of distributed power-generation systems, such as small wind power [2], [3]. The conversion mechanism of the traditional single-phase DC/AC inverter is PWM modulation [4]. PWM is a modulation technique that conforms to the width of the pulse, formally the pulse duration, based on modulator signal information. The single-phase DC/AC inverter suffers from high total harmonic distortion (THD) of output voltage waveform, low efficiency, and large size [5]. The single-phase DC/AC inverter has low total harmonic distortion, high efficiency, and a small size. Two methods have been used to increase the operating frequency of the inverters and change the topology of the main circuit.

Hard switching restricts the switching frequency. Hence, abundant efforts have been made to realize several kinds of the soft-switched version of the inverters. A resonant DC link has been introduced, but it encountered problems such as high peak voltage and/or current stress in the switching devices [6]. These problems are solved at the cost of additional complexity in the controller and additional components. The best method is to employ some forms of zero-voltage switching (ZVS) and/or zero-current switching (ZCS) to increase the efficiency and decrease size. The output voltage waveform of conventional single-phase full-bridge inverter is PWM to synthesize PWM signals and high THD [7]-[9].

High operating frequency and/or better circuit is needed to reduce the proportion of harmonic distortion. As a DC/AC inverter, the output voltage should be AC power. In addition, the expected output voltage is sinusoidal. A single-phase full-bridge inverter through controlled capacitor charging is proposed, which also suffers from low operating frequency [10]. The output voltage of the buck regulator varies linearly with the duty cycle for a given input voltage and ZCS technology has been applied to the buck regulator successfully [11]–[15]. This paper presents a novel half load-cycle worked DISO DC/AC inverter, which is composed of positive and negative buck regulators. The output voltage waveform is close to sinusoidal, which can work with ZCS and/or ZVS easily. The inverter is verified by simulation technology with the use of PSIM software. The experiment is tested first. Moreover, the commonly used control strategy is studied.

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†Corresponding Author: chenrongjn@163.com
Tel: +86-153-7690-9720, Fax: +86-532-8315-4820, China Univ. of Petroleum (Huadong)
*College of Information and control Engineering, China University of Petroleum (Huadong), China

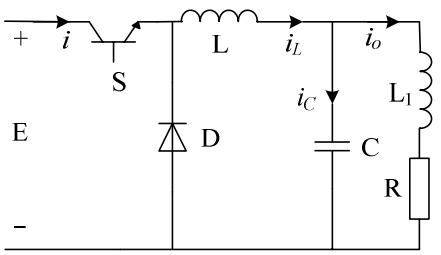


Fig. 1. Schematic of buck regulator.

II. Main Circuit Topology and Basic Working Principle

The DC/AC transform circuit is composed of the positive and negative buck regulators [16]. Figure 1 shows the schematic of the buck regulator.

Switch S is switched hard on and hard off in series with the DC input voltage E to produce a rectangular voltage at the anode side of the diode D. In the buck regulator, the on period of the power device (T_{on}) is adjusted to maintain regulation, while the total cycle period (T) is fixed. Hence, the frequency is fixed at $1/T$.

When switch S is on, a current builds up in the series inductor L that flows toward the output. The current transfers energy from E to the output capacitor and load. The output voltage U_o (U_o is the average output voltage) is less than E. Hence, the inductor L will impress a voltage across $u_L=E-U_o$. Current rises linearly with a constant voltage across the inductor. Inductive energy also rises. When switch S is off, inductive energy releases through the free-wheeling diode D. In addition, the current in the inductor decreases linearly with $u_L=-U_o$. In the on switching period, the net change of the inductor current is zero. This change is proportional to the integral of the inductor voltage over the interval. Therefore, the integral of the inductor voltage must be zero in steady state, which is the principle of inductor volt-second balance. Assuming the off period of the power device is T_{off}, $T_{on}+T_{off}=T$, Equation (1) will be obtained.

$$(E-U_o)T_{on}-U_oT_{off}=0 \tag{1}$$

The relationship of the input and output voltage of buck regulators is shown in Equation (2).

$$\frac{U_o}{E}=\frac{T_{on}}{T_{on}+T_{off}}=\frac{T_{on}}{T}=D \tag{2}$$

D is called the duty ratio, which can be controlled electronically in a range of 0–1. Generally, the output voltage is smaller than the input voltage.

When the switch S is on, the current through the inductor L is I_{L1}. Equation (3) will be obtained.

$$L\frac{di_{L1}}{dt}+U_o=E \tag{3}$$

Assuming that the initial value of the current through the inductor L is I_{L10}, then Equation (4) will be obtained.

$$i_{L1}(t)=\frac{E-U_o}{L}t+I_{L10} \tag{4}$$

When the switch S is off, the current through the inductor L is I_{L2}. Equation (5) will then be obtained.

$$L\frac{di_{L2}}{dt}+U_o=0 \tag{5}$$

Assuming that the initial value of the current through the inductor L is I_{L20}, then Equation (6) will be obtained.

$$i_{L2}(t)=I_{L20}-\frac{U_o}{L}(t-T_{on}) \tag{6}$$

and

$$I_{L20}=i_{L1}(T_{on}) \tag{7}$$

According to the law of conservation of energy, the power supplied to the load is equal to the load consumption during a cycle period, as shown in Equation (8).

$$\int_0^{T_{on}}E*i_{L1}(t)dt=\frac{U_o^2}{R}T \tag{8}$$

Therefore, I_{L10} can be written as Equation (9).

$$I_{L10}=\frac{U_o}{R}-\frac{E-U_o}{2L}T_{on} \tag{9}$$

and

$$i_{L1}(t)=\frac{U_o}{R}+\frac{E-U_o}{2L}(2t-T_{on}) \tag{10}$$

I_{L20} can be written as Equation (11).

$$I_{L20}=\frac{U_o}{R}+\frac{E-U_o}{2L}T_{on} \tag{11}$$

and

$$i_{L2}(t)=\frac{U_o}{R}+\frac{E-U_o}{2L}T_{on}-\frac{U_o}{L}(t-T_{on}) \tag{12}$$

The current through the inductor L ripple is as follows:

$$\frac{1}{2}\Delta i_L=\frac{E-U_o}{2L}T_{on}=\frac{U_o(1-D)}{2L}T \tag{13}$$

When the buck regulator works on the CCM/DCM boundary, Equation (14) is needed.

$$\frac{U_o(1-D)T}{2L}=\frac{U_o}{R} \tag{14}$$

Boundary value of L, D can be obtained as Equation (15).

$$K=1-D=\frac{2Lf}{R} \tag{15}$$

When $K=1-D<\frac{2Lf}{R}$, the buck regulator works on CCM.

When $K=1-D>\frac{2Lf}{R}$, the buck regulator works on DCM.

When the buck regulator works in CCM, the output voltage is proportional to the duty cycle D. To ensure that the output voltage of buck regulator is a sinusoidal voltage, the only thing needed is to control the duty cycle D according to SPWM law. Hence, the duty cycle D will vary according to the sine rule. The positive buck regulator must be used in conjunction with the negative buck regulator because of the unidirectional output voltage of the buck regulator.

The main circuit topology of the DC/AC inverter is shown in

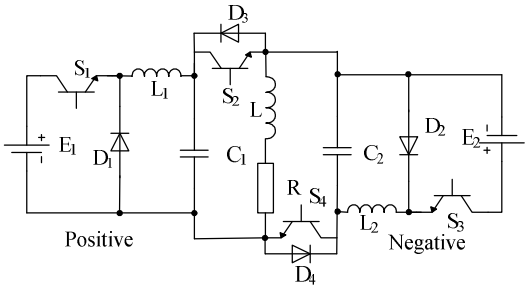


Fig. 2. Main circuit topology of DC/AC inverter.

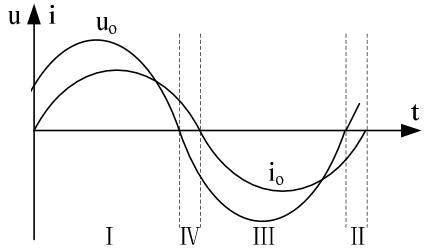


Fig. 3. Working quadrant of DC/AC inverter.

Fig. 2. The DC/AC inverter is composed of the positive and negative buck regulators. The positive buck regulator is used to provide the positive half cycle of the output. The negative buck regulator is used to generate the negative half cycle of the output. Hence, only one set of buck regulator is at work any time.

III. ANALYSIS OF WORKING PRINCIPLE

Fig. 3 shows the working quadrant of the DC/AC inverter.

In the first quadrant, the positive buck regulator works, while the negative buck regulator does not work. u_o>0, i_o>0. Unidirectional switch S_1 is controlled according to SPWM mode. Switch S_2 is still on. Control signals of switches S_2 and S_4 are complementary. Switches S_3 and S_4 are off. Two operating modes are found.

Mode1: Fig. 4(a) shows that unidirectional switch S_1 is on. The current that flows through inductor L_1 ramps up linearly and switch S_2 is still on. The positive buck regulator supplies the output capacitor C_1 and load.

Mode 2: Fig. 4(b) shows that the unidirectional switch S_1 is off. The current that flows through inductor L_1 decreases linearly and switch S_2 is still on. The output capacitor C_1 supplies the load.

In the second quadrant, the positive buck regulator works while the negative buck regulator does not work. u_o>0, i_o<0. The anti-parallel diode D_2 of switch S_2 works. The load current is freewheeling. Two operating modes are found. A schematic of the second quadrant is shown in Fig. 5.

Fig. 5(a) shows that when switch S_1 is on, the anti-parallel diode D_2 of switch S_2 is working. Fig. 5(b) shows that when switch S_1 is off, the anti-parallel diode D_2 of switch S_2 is also working.

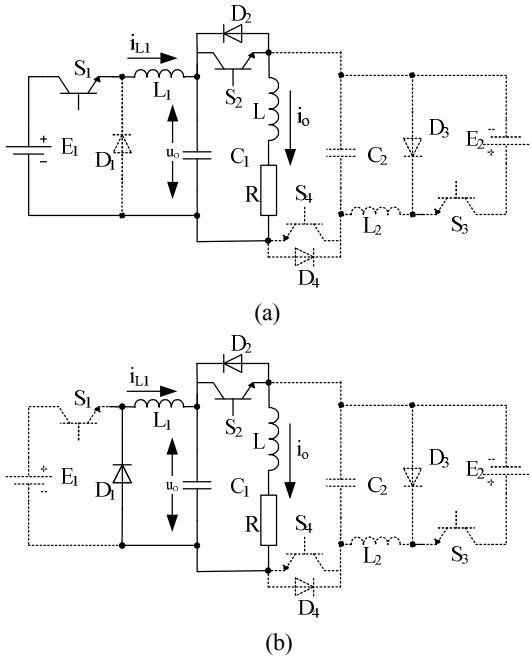


Fig. 4. Schematic of the first quadrant.

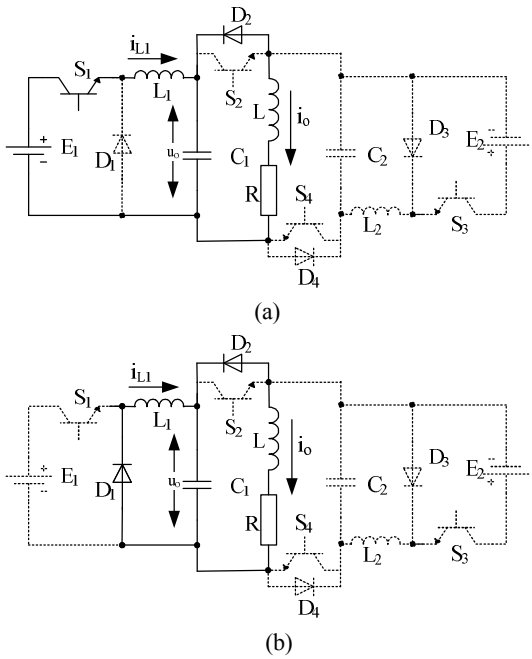


Fig. 5. Schematic of the second quadrant.

In the third quadrant, the negative buck regulator works while the positive buck regulator does not work. u_o<0, i_o<0. Unidirectional switch S_3 is controlled according to SPWM mode. Switch S_4 is still on, and switches S_1 and S_2 are off. Two operating modes are found.

Mode 3: Fig. 6(a) shows that unidirectional switch S_3 is on. The current that flows through inductor L_2 ramps up linearly and switch S_4 is still on. The negative buck regulator supplies for the output capacitor C_2 and load.

Mode 4: Fig. 6(b) shows that unidirectional switch S_3 is off.

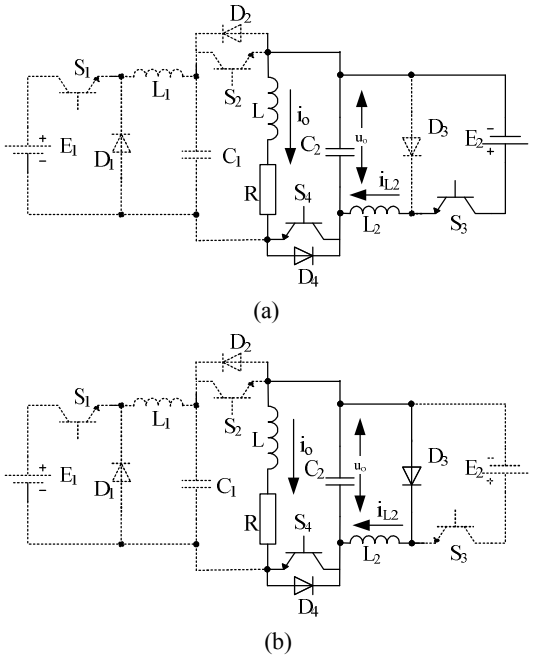


Fig. 6. Schematic of the third quadrant.

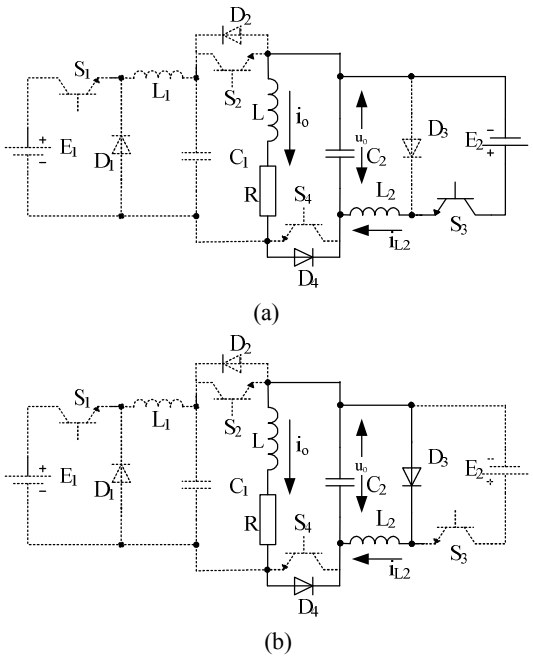


Fig. 7. Schematic of the fourth quadrant.

The current that flows through inductor L_2 decreases linearly and switch S_4 is still on. The output capacitor C_2 supplies the load.

In the fourth quadrant, the negative buck regulator works while the positive buck regulator does not work. $u_o<0$, $i_o>0$. The anti-parallel diode D_4 of switch S_4 works while the load current is freewheeling. Two operating modes are also found. A schematic diagram of the fourth quadrant is shown in Fig. 7. Fig. 7(a) shows that when switch S_3 is on, the anti-parallel diode D_4 of switch S_4 is working. Fig. 7(b) shows that when switch S_3 is off, the anti-parallel diode D_4 of switch S_4 is also working.

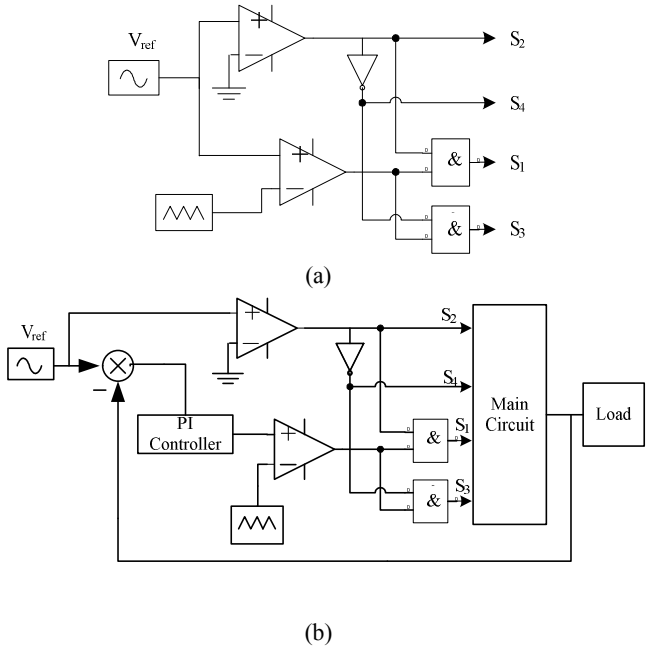


Fig. 8. System control diagram.

IV. Selection and Implementation of the System Control Strategy

In the most straightforward implementation of achieving high quality sinusoidal output, the desired sinusoidal output voltage is generated by comparing the desired sinusoidal reference waveform with a high-frequency triangular 'carrier' wave, which is the so-called SPWM control. The advantages of SPWM control are its fixed operating frequency and easily filtered harmonic signal. The positive half cycle and negative half cycle of the sine wave are realized by the positive and negative buck regulators, respectively. The voltage open-loop proportional-differential control can be accepted under the condition that the sinusoidal waveform quality requirements are not extremely high. In this manner, the quality of the sinusoidal output voltage can be ensured. However, the amplitude of the output voltage is controlled by the input voltage. If high quality sinusoidal output is needed, then voltage closed-loop proportional-integral control will be used. The amplitude of the output voltage will not be affected by the variation of the input voltage.

The system control diagram of open-loop P control is shown in Fig. 8(a), which is composed of the control signal generating circuit and pulse distribution circuit.

The system control diagram of closed-loop PI control is shown in Fig. 8(b), which is composed of the comparison calculation circuit and control signal generating circuit with the pulse distribution circuit.

When the unipolar SPWM modulation is used, limiting the

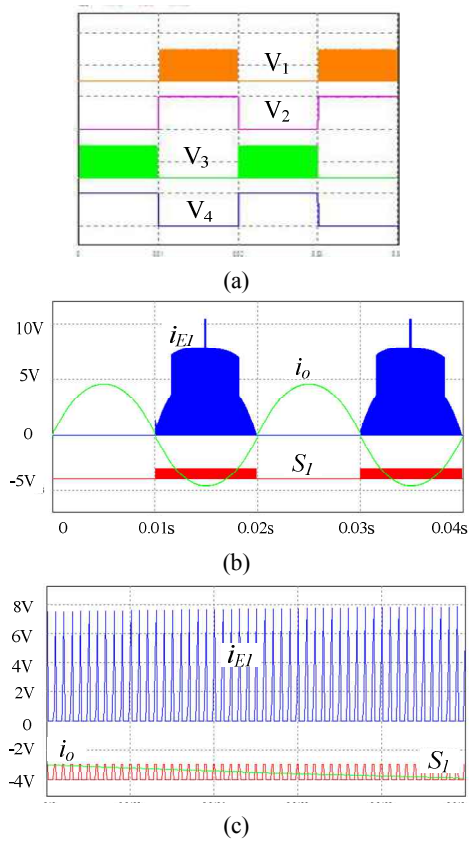


Fig. 9. Driving signal of V_1–V_4 with the PSIM.

value of the modulation ratio D is necessary to ensure that the positive and negative buck regulators can work in CCM. If the buck regulator works in the DCM mode, then the output voltage waveform will not be the perfect sinusoidal waveform.

V. Analysis of the Simulation Results

PSIM simulation software is used to verify the theoretical analysis above. The parameter values of DC/AC inverter used are listed below. Frequency of triangular carrier is 15.36 kHz. Frequency of sinusoidal reference waveform is 50 Hz, L_1=L_2=1 mH. C_1=C_2=22 μF, load resistor R=6Ω, and load inductance L=0.2 mH.

Fig. 9(a) shows the driving signal of S_1–S_4 with the PSIM. The special half load-cycle control mode is needed to obtain AC output, and S_1–S_4 must work in combination mode. Fig. 9(b) shows the waveform of load current i_o, source current i_{E1}, and driving signal of S_1. Fig. 9(c) shows a zoomed portion of Fig. 9(b).

Fig. 10 shows the simulation result of the open-loop P control implementation. The waveforms of sine wave "v_{ref}" and output voltage with the given reference is shown. The input voltage of Fig. 10(a) is 80 V. The input voltage of Fig. 10(b) is 120 V. Fig. 11 shows the simulation result of the closed-loop PI control implementation as well as the waveforms of the given reference sine wave. The output voltage is also shown.

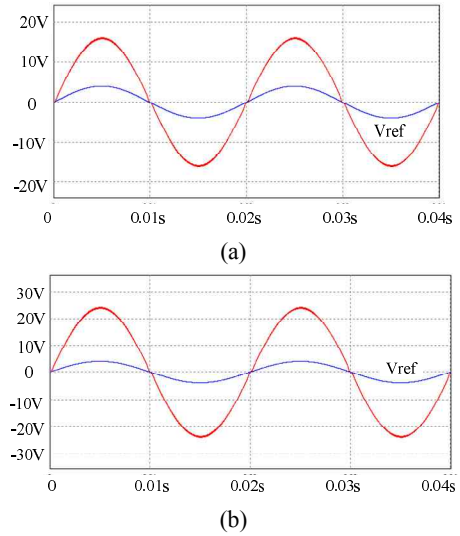


Fig. 10. Simulation result of the open-loop P control.

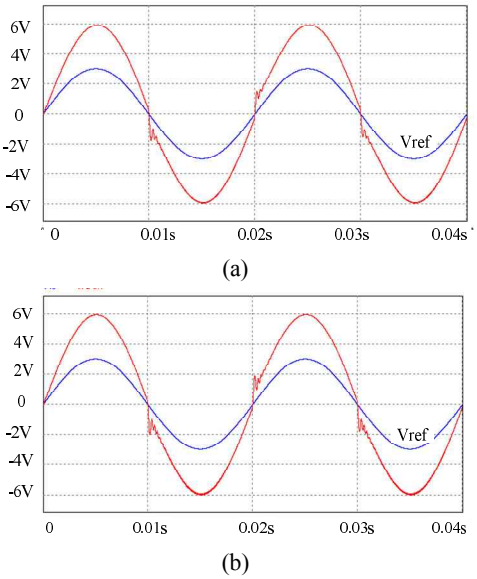


Fig. 11. Simulation result of the closed-loop PI control.

The input voltage of Figs. 11(a) and 11(b) is 80 and 120 V, respectively. The output voltage could follow the given reference sine wave well. The output voltage with the open-loop P control is affected by the input voltage. However, the output voltage with the closed-loop PI control is constant and unaffected by the input voltage.

Briefly, the control signal of the inverter with open-loop P control is SPWM, which derives Equation (2). In addition, the control signal of the inverter with closed-loop PI control is PWM and not SPWM. When the voltages of capacitors C_1 and C_2 are controlled by the closed-loop PI voltage control, the system has a stronger anti-interference ability on the input side of the DC voltage disturbances compared with the case in which it is controlled by the open-loop P control. Switches S_1 and S_3 can be adjusted dynamically by adjusting the duty cycle of the drive signal. Hence, the positive and negative output

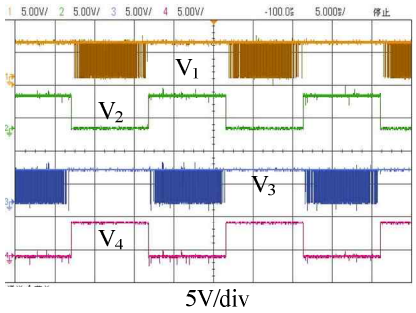


Fig. 12. Experiment control pulses of switches S_1–S_4.

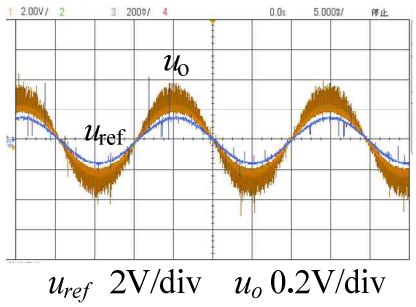


Fig. 13. Waveform of the output voltage and given reference signal.

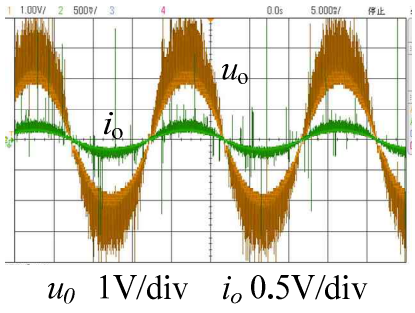
voltages will return to their normal values to overcome the input DC voltage disturbances.

VI. Analysis of the Experiment Results

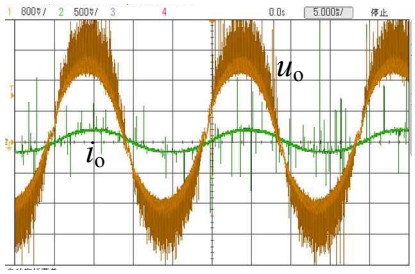
The dsPIC30F4011 microcontroller is used to develop an experimental prototype with a positive and negative buck regulators for photovoltaic power generation to verify the theoretical analysis and practical results. The parameter values of experiment prototype are as follows: the frequency of the triangular carrier is 15.36 kHz, the frequency of the sinusoidal reference waveform is 50 Hz, L_1=L_2=1 mH, C_1=C_2=22 μF, load resistor R=6Ω, and load inductance L=0.2 mH.

MOSFET IRF740 and fast recovery diode MUR8100E series combination are used as unidirectional switches S_1 and S_3 to meet the input voltage of 100 V. Switches S_2 and S_4 use MOSFET IRF740.

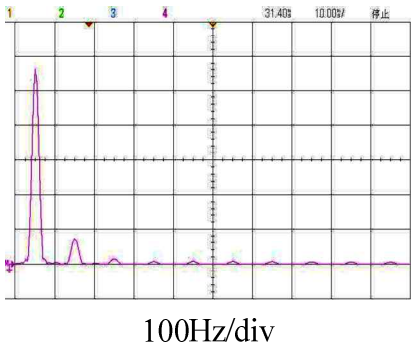
Experiment waveforms are shown in Figs. 12, 13, and 14. Fig. 12 shows the control pulses of switches S_1–S_4. Switches S_2 and S_4 are controlled by the complementary control signals V_2 and V_4 to achieve the operation of the positive buck regulator and the negative buck regulator, respectively. Fig. 13 is the experiment waveform of the output sinusoidal voltage and the given reference sinusoidal signal waveform. Fig. 14 is the experiment waveform of the output sinusoidal voltage and the load current waveform. Load inductance of Fig. 14(a) is 0.2 mH. Load inductance of Fig. 14(b) is 1 mH. The experimental waveforms of the output voltage are evidently consistent with the previous simulation results. The



(a)



(b)



(c)

Fig. 14. Waveform of the output voltage and load current.

harmonic component of the output voltage u_o in Fig. 14(b) is shown as Fig. 14(c). All experiment results verify that the output voltage can track the given signal dynamically. Moreover, the freewheeling effect of the load current is good.

VII. Conclusions

A novel half load-cycle worked DISO DC/AC inverter is presented based on the relationship between the input and output voltage of the buck regulator in continuous conduction mode (CCM). CCM is composed of a dual buck regulator, namely, positive buck regulator and negative buck regulator. The dual buck regulator works in half-cycle control and its output terminal works in anti-parallel mode. CCM features a dual power supply, single power output, and voltage step-down output. The simulation of the DC/AC inverter was presented through PSIM. The experiment is conducted on the experimental prototype. The simulation and experiment results

verified the correctness of the analytical theory of DC/AC inverter and feasibility of the novel inverter. The DC/AC inverter can track the input sinusoidal in real time.

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Rong Chen was born in Shandong, China in 1976. He received his B.S. degree in industrial automation in 1998 and M.S. degree in control theory and control engineering in 2001 from Shandong University of Science and Technology, Shandong, China. He is currently working toward a Ph.D. degree in control theory and control engineering at China University of Petroleum (UPC). His research interests include electric machine drives, power electronics, high frequency soft switching converters, and power factor correction.

Jia-Sheng Zhang was born in Shandong, China in 1957. He received his B.S. degree in applied electronic technology from China University of Petroleum, Shandong, China in 1982 and M.S. and Ph.D. degrees in electrical and electronic engineering from Beijing Jiaotong University, Beijing, China in 1988 and 1998, respectively. In 1982, he joined the Department of Electrical Engineering at China University of Petroleum, Shandong, China, where he is currently employed full time as a professor. His current research interests include power electronics, motor drives, power quality control, renewable distributed power sources, and DSP-based control of power converters.