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Transformer-Less Single-Phase Four-Level Inverter for PV System Applications

Saeed Yousofi-Darmian* and Seyed Masoud Barakati†

*†Faculty of Electrical and Computer Engineering, University of Sistan and Baluchestan, Zahedan, Iran

Abstract

A new inverter topology for single-phase photovoltaic (PV) systems is proposed in this study. The proposed inverter offers a four-level voltage in its output terminals. This feature results in easier filtering in comparison with other conventional two-level or three-level inverters. In addition, the proposed four-level inverter (PFLI) has a transformer-less topology, which decreases the size, weight, and cost of the entire system and increases the overall efficiency of the system. Although the inverter is transformer-less, it produces a negligible leakage ground current (LGC), which makes this inverter suitable for PV grid-connected applications. The performance of the proposed inverter is compared with that of a four-level neutral point clamped inverter (FLNPCI). Theoretical analysis and computer simulations verify that the PFLI topology is superior to FLNPCI in terms of efficiency and suitability for use in PV transformer-less systems.

Key words: Four-level inverter, Leakage ground current, Photovoltaic system, Single-phase, Transformer-less

I. INTRODUCTION

Among the photovoltaic (PV) systems, grid-connected PV systems and single-phase systems of up to 5 kW play an important role. It is attempted to determine the benefits of these systems. As most of these systems are private, efficiency and reliability should be maximized and size, weight, and cost should be minimized [1], [2]. Depending on the isolation between the PV panels and the grid, the inverter can be either isolated or non-isolated. Isolation is usually achieved using a transformer, which significantly affects the efficiency of the PV system [3]. Isolation occurs in two ways: first, by using a step-up low-frequency transformer in the grid side [Fig. 1(a)]; second, by using a high-frequency transformer in the direct current (DC) side [Fig. 1(b)]. A transformer-less inverter can decrease the weight, size, cost, and installation complexity of the entire PV system (see Fig. 2). A drawback of using transformer-less PV systems is that omitting the transformer induces DC current in the output AC terminal. Semiconductor parameter variations and filter elements may affect the increase in DC current. However, some manufacturing techniques decrease such effects to an acceptable level [4]. One of the important advantages of the transformer-less inverters is an increase in overall system efficiency of up to 2% [5]. Various inverter topologies are proposed in the literature for grid-connected PV systems, such as full-bridge (FB) based or neutral point clamped (NPC)-based [4], [6]-[12].

The paper is organized as follows: The proposed topology is studied in Section II. A single-phase four-level NPC inverter (FLNPCI) is considered in Section III. The analysis of losses and LGC are presented in Sections IV and V, respectively. The simulation results are presented in section VII. Section VIII concludes this study.

II. PFLI TOPOLOGY

The proposed four-level inverter (PFLI) has ten IGBTs along with freewheeling diodes and three PV sources that have the same voltages. This topology is FB-based and can generate a four-level and symmetrical voltage on its output terminals. The PFLI topology is shown in Fig. 3, where C_{PV} is the parasitic capacitance between the PV panels and ground [13]. This topology is composed of two FB structures with outputs connected to each other. One of them is connected to the middle of the DC bus through two switches (S_{31} and S_{32}). These two switches enable the middle DC bus voltage to

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†Corresponding Author: smbaraka@ece.usb.ac.ir
Tel.: +98-541-8056400, Fax: +98-541-2445707, University of Sistan and Baluchestan
*Faculty of Electrical and Computer Engineering, University of Sistan and Baluchestan, Iran

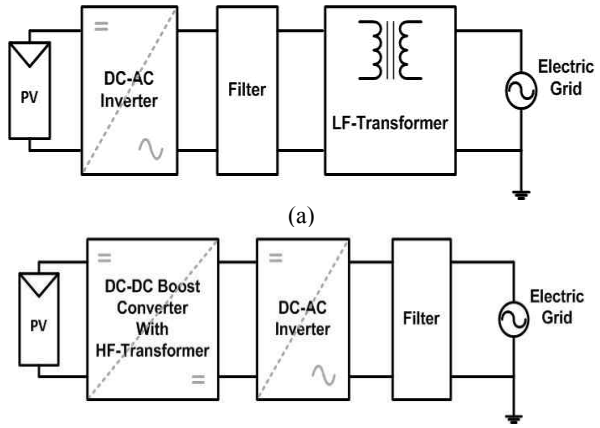

Fig. 1. Isolation in a grid-connected PV system. (a) Low-frequency transformer in the AC side. (b) High-frequency transformer in the DC side.

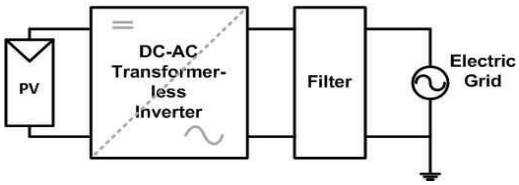

Fig. 2. Grid-connected PV system with a transformer-less inverter.

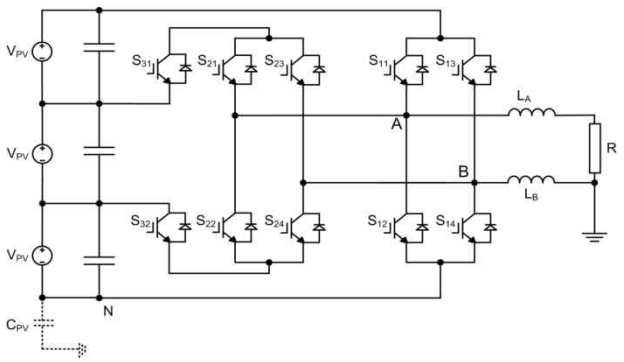

Fig. 3. PFLI topology.

connect to the output directly or inversely without necessarily changing the direction of the output current. Switching states of the PFLI topology for generating a four-level output voltage are listed in Table I. The switches states for each voltage level (++, +, −−, −) are shown in Fig. 4, where the switches states are drawn for positive sign of the current in levels ++ and + and the negative sign of the current in levels − and −−. In voltage level ++ [Fig. 4(a)], switches S_{11} and S_{14} are on and the current flows through their IGBTs. When the sign of the current reverses (in non-unity power factors), the current flows through freewheeling diodes of S_{11} and S_{14}. In voltage level + [Fig. 4(b)], the output current flows through the IGBTs of S_{21} and S_{24} and freewheeling diodes of S_{31} and S_{32}. However, in the case that the power factor is non-unity or in the negative half-cycle of the output current, the current will flow through the freewheeling diodes of S_{21} and S_{24} and

TABLE I
SWITCHING STATES FOR THE PFLI TOPOLOGY

Switches	Voltage levels			
	++	+	−	−−
S_{11}	1	0	0	0
S_{12}	0	0	0	1
S_{13}	0	0	0	1
S_{14}	1	0	0	0
S_{21}	0	1	0	0
S_{22}	0	0	1	0
S_{23}	0	0	1	0
S_{24}	0	1	0	0
S_{31}	0	1	1	0
S_{32}	0	1	1	0

IGBTs of S_{31} and S_{32}. In voltage level −− [Fig. 4(c)], switches S_{12} and S_{13} are on and the current flows through the IGBTs. In non-unity power factors, where the sign of the current reverses, the current will flow through their corresponding freewheeling diodes. In voltage level – [Fig. 4(d)], the output current flows through the IGBTs of S_{22} and S_{23} and the freewheeling diodes of S_{31} and S_{32}. However, in the case that the power factor is non-unity or in the positive half-cycle of the output current, the current will flow through the freewheeling diodes of S_{22} and S_{23} and IGBTs of S_{31} and S_{32}. To modulate the PFLI switches, a pulse-width modulation (PWM)-based method is used. The modulating and carrier signals of the PWM method are shown in Fig. 5(a). In this figure, CS1, CS2, and CS3 are the carrier signals and MS is the modulating signal. Fig. 5(b) switches gate signals of the PFLI topology in one cycle of fundamental frequency.

The desired output voltage from the modulation procedure is shown in Fig. 6. As shown in Fig. 6, the inverter output voltage has four modes. In this figure, modes I and III are derived from modulating CS2 with MS, which results in a switch between + and − levels. The only difference between these modes is the direction of the output current.

Mode II is also derived from modulating CS1 with MS, which results in a switch between ++ and + levels. Mode IV is derived from modulating CS3 with MS, which results in a switch between −− and − levels. The voltages of all switches of the PFLI are demonstrated in Table II. As shown in Table II, the maximum voltage that should be tolerated by switches is $3V_{PV}$, which is related to S_{11} to S_{14}. By contrast, switches with the lowest stress are S_{31} and S_{32}, which have a voltage of $1/4V_{PV}$.

III. FLNPCI TOPOLOGY

The NPC topology was introduced by Nabae et al. [14] in 1981. In this topology, switch stress is improved and it can be used in single-phase and three-phase systems [15]. High voltage requirement in the DC bus is the main disadvantage

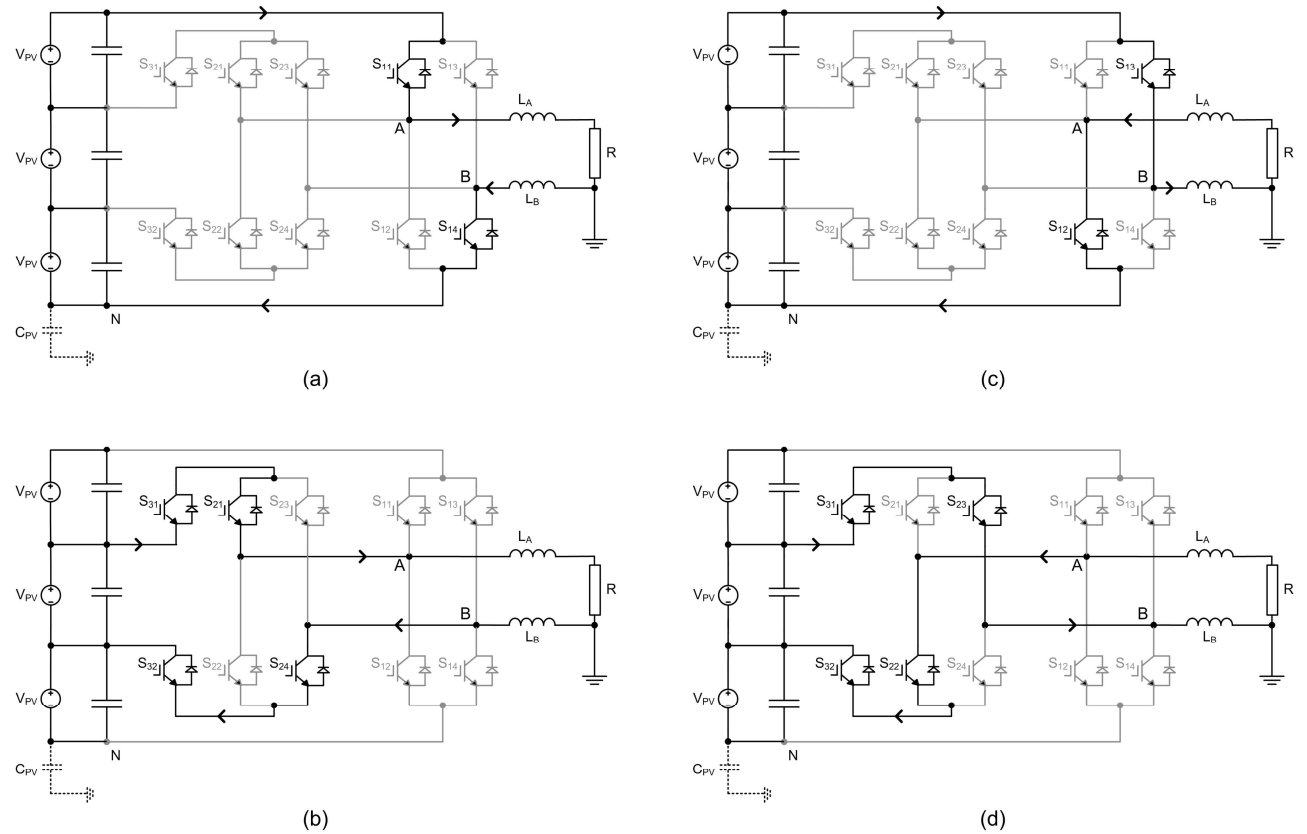

Fig. 4. Switches states of the PFLI topology in voltage levels. (a) ++. (b) +. (c) −−. (d) −.

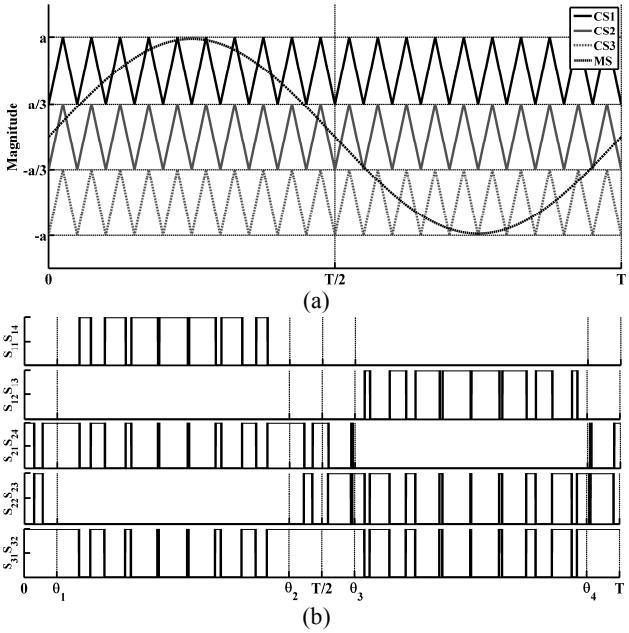

Fig. 5. Modulation signals of PFLI switches. (a) Modulating and carrier signals. (b) Switches gate signals.

of this topology. If high DC voltage is unavailable, then a boost stage will be required. Thus, the overall efficiency of the system decreases considerably [4]. In this topology, the transient voltage across the inner switches is greater than the outer switches. This finding is due to the fact that the inner

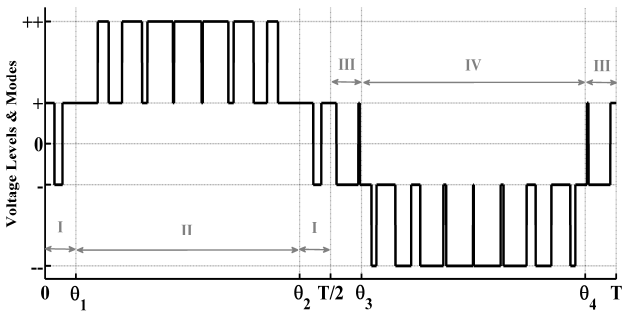

Fig. 6. Desired output voltage from PWM.

switches are not clamped to DC link capacitors same as the outer switches. The inner switches are also directly affected by parasitic components in the system layout [16], [17]. In this section, the topology of single-phase FLNPCI is analyzed.

Unlike the three-phase types of NPC inverters, the single-phase types (in structures with an even number of output voltage levels) encounter the neutral point problem because the neutral wire cannot be connected directly to DC link capacitors.

To solve this problem, bidirectional (four quadrants) switches have to be used to connect the neutral wire to the middle capacitor of the DC link. The FLNPCI topology with asymmetrical DC sources (FLNPCI-ASDC) is shown in Fig. 7. In this topology, the voltage of the middle DC source is

TABLE II
SWITCH VOLTAGES OF THE PFLI TOPOLOGY

Operating modes	Modes I and III		Mode II		Mode IV	
Output level	+	−	++	+	−−	−
V_{S11}	$3/2V_{PV}$	$3/2V_{PV}$	0	$3/2V_{PV}$	$3V_{PV}$	$3/2V_{PV}$
V_{S12}	$3/2V_{PV}$	$3/2V_{PV}$	$3V_{PV}$	$3/2V_{PV}$	0	$3/2V_{PV}$
V_{S13}	$3/2V_{PV}$	$3/2V_{PV}$	$3V_{PV}$	$3/2V_{PV}$	0	$3/2V_{PV}$
V_{S14}	$3/2V_{PV}$	$3/2V_{PV}$	0	$3/2V_{PV}$	$3V_{PV}$	$3/2V_{PV}$
V_{S21}	0	V_{PV}	$1/4V_{PV}$	0	$1/4V_{PV}$	V_{PV}
V_{S22}	V_{PV}	0	$1/4V_{PV}$	V_{PV}	$1/4V_{PV}$	0
V_{S23}	V_{PV}	0	$1/4V_{PV}$	V_{PV}	$1/4V_{PV}$	0
V_{S24}	0	V_{PV}	$1/4V_{PV}$	0	$1/4V_{PV}$	V_{PV}
V_{S31}	0	0	$1/4V_{PV}$	0	$1/4V_{PV}$	0
V_{S32}	0	0	$1/4V_{PV}$	0	$1/4V_{PV}$	0

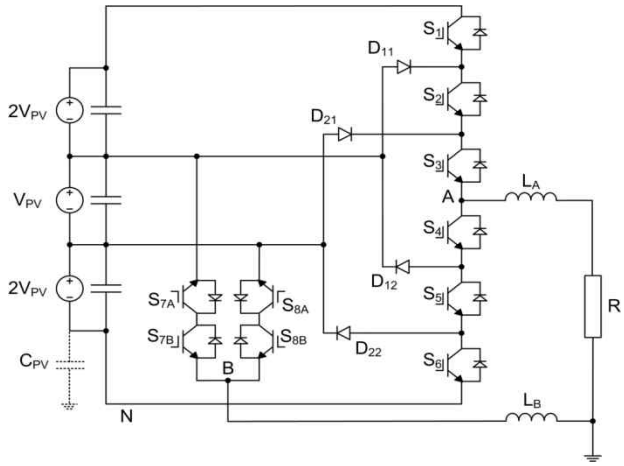

Fig. 7. Single-phase FLNPCI-ASDC topology.

half of the other ones. This property allows the FLNPCI-ASDC to provide a symmetrical four-level voltage to its output terminal. By contrast, the FLNPCI topology with symmetrical DC sources (FLNPC-SDC) has identical DC sources in its input. In this case, the magnitude of the levels in the output four-level voltage will not be the same. The FLNPCI-ASDC topology consists of 10 IGBTs with freewheeling diodes and four diodes for clamping. As shown in Fig. 7, the output voltage of PV sources is not identical. If the PV source voltages are equal (FLNPCI-SDC), the low-order current harmonics will be increased, which are difficult to filter, and the levels of the output four-level voltage will not be the same. To resolve this problem, the upper and lower sources should be identical and the middle source should be half the other sources (FLNPCI-ASDC). As a result, the magnitude of the output voltage in each mode will be the same. The FLNPCI-ASDC has five DC sources, whereas the FLNPCI-SDC has three DC sources in its input.

The modulation method for the FLNPCI topology is phase

TABLE III
SWITCH VOLTAGES OF THE FLNPCI-ASDC TOPOLOGY

Operating modes	Modes I and III		Mode II		Mode IV	
Output level	+	−	++	+	−−	−
V_{S1}	$2V_{PV}$	$3/2V_{PV}$	0	$2V_{PV}$	$5/3V_{PV}$	$3/2V_{PV}$
V_{S2}	0	$3/2V_{PV}$	0	0	$5/3V_{PV}$	$3/2V_{PV}$
V_{S3}	0	0	0	0	$5/3V_{PV}$	0
V_{S4}	0	0	$5/3V_{PV}$	0	0	0
V_{S5}	$3/2V_{PV}$	0	$5/3V_{PV}$	$3/2V_{PV}$	0	0
V_{S6}	$3/2V_{PV}$	$2V_{PV}$	$5/3V_{PV}$	$3/2V_{PV}$	0	$2V_{PV}$
V_{D7A}	$1/2V_{PV}$	0	$1/2V_{PV}$	$1/2V_{PV}$	0	0
V_{S7B}	$1/2V_{PV}$	0	$1/2V_{PV}$	$1/2V_{PV}$	0	0
V_{S8A}	0	$1/2V_{PV}$	0	0	$1/2V_{PV}$	$1/2V_{PV}$
V_{D8B}	0	$1/2V_{PV}$	0	0	$1/2V_{PV}$	$1/2V_{PV}$
V_{D11}	0	$-1/2V_{PV}$	$-2V_{PV}$	0	$-1/3V_{PV}$	$-1/2V_{PV}$
V_{D12}	0	$-V_{PV}$	$1/3V_{PV}$	0	$-3V_{PV}$	$-V_{PV}$
V_{D21}	$-V_{PV}$	0	$-3V_{PV}$	$-V_{PV}$	$1/3V_{PV}$	0
V_{D22}	$-1/2V_{PV}$	0	$-1/3V_{PV}$	$-1/2V_{PV}$	$-2V_{PV}$	0

disposition PWM (PDPWM) [18]. Modulating and carrier waveforms for this method are shown in Fig. 5(a). Switching signals generated by the PDPWM method are applied to S_1, $S_2(S_8)$, and S_3, and complimentary signals are applied to S_4, $S_5(S_7)$, and S_6, respectively. Thus, a four-level voltage will be obtained as output of the inverter. The voltages of all switches in each operational mode are shown in Table III. Based on Table III, the maximum voltage of the switches is $3V_{PV}$, which is associated with D_{12} and D_{21}. Switches with the lowest stress are S_7 and S_8, which have the voltage of $1/2V_{PV}$.

IV. ANALYSIS OF LOSSES

A. Switching Losses

1) Switching Losses of the FLNPCI-ASDC: Given the non-uniform PV resources and switches gate signals, switching losses will differ. The average switching losses of a switch can be approximately expressed as follows [19]:

$$P_{SW} = \frac{1}{2} V_{off} I_{on} f_s \left(t_{c(on)} + t_{c(off)} \right). \quad (1)$$

In (1), $t_{c(off)}$ and $t_{c(on)}$ are the times that the switch is turned off and on completely, respectively, f_s is the switching frequency, and I_{on} and V_{off} are the current and voltage of the on-state and off-state of the switch, respectively. Assuming that all switches are identical and based on the same switching frequency and current of all switches, the difference factor of switching losses is the difference between off-state voltages (V_{off}) of the switches; one can write.

$$P_{SW} = cV_{off}. \quad (2)$$

According to Table III, in mode I, the switching losses of back to back switches (S_{7i} and S_{8i}, where i = A, B) are related to the 7A (7B) and 8A (8B) IGBTs (diodes). By contrast, in mode III, they are related to the 7B (7A) and 8B (8A) IGBTs (diodes).

Imposing $V_{off} = V_{PV}$, we derive the following equation:

$$P_{SW} = cV_{PV} = P. \tag{3}$$

In relation to Fig. 5, we observed that

$$\begin{cases} \theta_1 = \dfrac{T}{2} - \theta_2 = \theta_3 - \dfrac{T}{2} = T - \theta_4 \\ \theta_2 - \theta_1 = \theta_4 - \theta_3 \end{cases}. \tag{4}$$

With regard to (4), the operating time of modes I and III (II and IV) are identical. Based on Table III, the switching losses in mode I are the same as those in mode III and those in mode II are the same as those in mode IV. Based on Table I and

$$t = \frac{\theta}{\omega}, \tag{5}$$

the switching losses of IGBTs (P_{SWI}) in t_1 and t_2-t_1 can be represented as follows:

$$\begin{cases} P_{SWI_{t_1}} = 4P \\ P_{SWI_{(t_2-t_1)}} = \dfrac{11}{3}P \end{cases}. \tag{6}$$

According to the switching losses of diodes (P_{SWD}), we derive the following equation:

$$\begin{cases} P_{SWD_{t_1}} = 4P \\ P_{SWD_{(t_2-t_1)}} = \dfrac{7}{3}P \end{cases}. \tag{7}$$

With regard to (3) and (4) and Table III, the average switching losses in one cycle of fundamental frequency (see Fig. 5) can be expressed as follows:

$$P_{SW} = 4\frac{\omega t_1}{T}P_{SW_{t_1}} + 2\frac{\omega(t_2 - t_1)}{T}P_{SW_{(t_2-t_1)}}, \tag{8}$$

Also, it can be deduced,

$$\begin{cases} \dfrac{\omega t_1}{T} = \dfrac{\sin^{-1}\left(\frac{1}{3}\right)}{2\pi} \\ \dfrac{\omega(t_2 - t_1)}{T} = \dfrac{1}{2} - \dfrac{\omega t_1}{\pi} \end{cases}. \tag{9}$$

Thus, based on (7), (8), and (9), we will have:

$$\begin{cases} P_{SWI_{FLNPC\text{-}ASDC}} = \left[\dfrac{11}{3} + \dfrac{2}{3\pi}\sin^{-1}\left(\frac{1}{3}\right)\right]P \\ P_{SWD_{FLNPC\text{-}ASDC}} = \left[\dfrac{7}{3} + \dfrac{10}{3\pi}\sin^{-1}\left(\frac{1}{3}\right)\right]P \end{cases}. \tag{10}$$

In (10), $P_{SWI_{FLNPC\text{-}ASDC}}$ and $P_{SWD_{FLNPC\text{-}ASDC}}$ are the switching losses of the IGBTs and diodes, respectively.

2) Switching Losses of the FLNPC-SDC: In this case, the procedure of obtaining the switching losses equations is similar to the FLNPC-ASDC. The voltages of all switches of the FLNPCI-SDC in each operational mode are shown in Table IV. The switching losses of the IGBTs in t_1 and (t_2-t_1) are expressed as follows:

TABLE IV
SWITCH VOLTAGES OF THE FLNPCI-SDC TOPOLOGY

Operating modes	Modes I and mode III		Mode II		Mode IV	
Output level	+	−	++	+	−−	−
V_{S1}	V_{PV}	V_{PV}	0	V_{PV}	V_{PV}	V_{PV}
V_{S2}	0	V_{PV}	0	0	V_{PV}	V_{PV}
V_{S3}	0	0	0	0	V_{PV}	0
V_{S4}	0	0	V_{PV}	0	0	0
V_{S5}	V_{PV}	0	V_{PV}	V_{PV}	0	0
V_{S6}	V_{PV}	V_{PV}	V_{PV}	V_{PV}	0	V_{PV}
V_{D7A}	$1/2V_{PV}$	0	$1/2V_{PV}$	$1/2V_{PV}$	0	0
V_{S7B}	$1/2V_{PV}$	0	$1/2V_{PV}$	$1/2V_{PV}$	0	0
V_{S8A}	0	$1/2V_{PV}$	0	0	$1/2V_{PV}$	$1/2V_{PV}$
V_{D8B}	0	$1/2V_{PV}$	0	0	$1/2V_{PV}$	$1/2V_{PV}$
V_{D11}	0	0	$-V_{PV}$	0	0	0
V_{D12}	0	$-V_{PV}$	0	0	$-2V_{PV}$	$-V_{PV}$
V_{D21}	$-V_{PV}$	0	$-2V_{PV}$	$-V_{PV}$	0	0
V_{D22}	0	0	0	0	$-V_{PV}$	0

$$\begin{cases} P_{SWI_{t_1}} = 3P \\ P_{SWI_{(t_2-t_1)}} = 2P \end{cases}. \tag{11}$$

The switching losses of the diodes in t_1 and (t_2-t_1) are:

$$\begin{cases} P_{SWD_{t_1}} = 3P \\ P_{SWD_{(t_2-t_1)}} = P \end{cases}. \tag{12}$$

The switching losses of all semiconductors in one cycle of output fundamental frequency are expressed as follows:

$$\begin{cases} P_{SWI_{FLNPCI\text{-}SDC}} = \left[2 + \dfrac{2}{\pi}\sin^{-1}\left(\frac{1}{3}\right)\right]P \\ P_{SWD_{FLNPCI\text{-}SDC}} = \left[1 + \dfrac{4}{\pi}\sin^{-1}\left(\frac{1}{3}\right)\right]P \end{cases}. \tag{13}$$

3) Switching Losses of the PFLI: According to Table II, the switching losses of S_{22} (S_{21}) and S_{23} (S_{24}) in mode I (mode III) and switching losses of S_{31} and S_{32} in modes II and IV are due to their corresponding freewheeling diodes. Based on Table II, the switching losses of IGBTs in t_1 and t_2-t_1 can be expressed as follows:

$$\begin{cases} P_{SWI_{t_1}} = 2P \\ P_{SWI_{(t_2-t_1)}} = \dfrac{7}{2}P \end{cases}. \tag{14}$$

The switching losses of diodes are:

$$\begin{cases} P_{SWD_{t_1}} = 2P \\ P_{SWD_{(t_2-t_1)}} = \dfrac{1}{2}P \end{cases}. \tag{15}$$

Based on (8), (14), and (15), the average switching losses of this topology in one cycle of fundamental frequency can be expressed as follows:

$$\begin{cases} P_{SWI_{PFLI}} = \left[\frac{7}{2} - \frac{3}{\pi}\sin^{-1}\left(\frac{1}{3}\right)\right]P \\ P_{SWD_{PFLI}} = \left[\frac{1}{2} + \frac{3}{\pi}\sin^{-1}\left(\frac{1}{3}\right)\right]P \end{cases}, \quad (16)$$

where, $P_{SWI_{PFLI}}$ and $P_{SWD_{PFLI}}$ are the switching losses of IGBTs and diodes of the PFLI, respectively.

From (10) and (16), we derive the following equation:

$$\begin{cases} \frac{P_{SWI_{PFLI}}}{P_{SWI_{FLNPC\text{-}ASDC}}} \cong 85\% \\ \frac{P_{SWD_{PFLI}}}{P_{SWD_{FLNPC\text{-}ASDC}}} \cong 30.6\% \end{cases}. \quad (17)$$

We deduced from (17) that the switching losses of the PFLI topology are lower than those of the FLNPCI-ASDC topology. Based on (13) and (16), one can write,

$$\frac{P_{SWI_{PFLI}}}{P_{SWI_{FLNPCI\text{-}SDC}}} \cong 143.3\% , \quad \frac{P_{SWD_{PFLI}}}{P_{SWD_{FLNPCI\text{-}SDC}}} \cong 57.6\%. \quad (18)$$

As shown in (18), the switching losses of the IGBTs of the PFLI are higher than those of the FLNPCI-SDC. However, the switching losses of the diodes of the PFLI are lower than those of the FLNPCI-SDC.

B. Conduction Losses

Conduction losses of a switch can be calculated as follows [19]:

$$P_{cond} = V_{on} I_{on} \frac{t_{on}}{T_s}, \quad (19)$$

where t_{on} is the on-state time, T_s is the switching period, and I_{on} and V_{on} are the on-state current and voltage of the switch, respectively. As I_{on} is identical for all conducting switches and assuming that V_{on} is the same for all conducting switches, the conduction losses of studied topologies can be approximately compared with each other by averaging the conducting switches in one cycle of fundamental frequency.

All conducting switches are shown in Table V for each voltage level of the FLNPCI topology. Based on Table V, the number of conducting switches should be counted in each operational mode. So, we have:

$$\begin{cases} \text{Mode I} \begin{cases} + \text{ with } I_{on} > 0, \\ - \text{ with } I_{on} > 0. \end{cases} \\ \text{Mode II} \begin{cases} ++, \\ + \text{ with } I_{on} > 0. \end{cases} \\ \text{Mode III} \begin{cases} + \text{ with } I_{on} < 0, \\ - \text{ with } I_{on} < 0. \end{cases} \\ \text{Mode IV} \begin{cases} --, \\ - \text{ with } I_{on} < 0. \end{cases} \end{cases} \quad (20)$$

TABLE V
CONDUCTING SWITCHES OF THE FLNPCI TOPOLOGY

Inverter voltage levels	++	+		−		−−
		$I_o > 0$	$I_o < 0$	$I_o < 0$	$I_o > 0$	
Conducting IGBTs	S_1, S_2, S_3, S_{8A}	S_2, S_3, S_{8A}	S_4, S_{8B}	S_4, S_5, S_{7B}	S_3, S_{7A}	S_4, S_5, S_6, S_{7B}
Conducting diodes	D_{8B}	D_{11}, D_{8B}	D_{12}, D_{8A}	D_{7A}, D_{22}	D_{7B}, D_{21}	D_{7A}

TABLE VI
CONDUCTING SWITCHES OF THE PFLI TOPOLOGY

Inverter voltage levels	++	+		−		−−
		$I_o > 0$	$I_o < 0$	$I_o < 0$	$I_o > 0$	
Conducting IGBTs	S_{11}, S_{14}	S_{21}, S_{24}	S_{31}, S_{32}	S_{23}, S_{22}	S_{31}, S_{32}	S_{13}, S_{12}
Conducting diodes	0	D_{31}, D_{32}	D_{21}, D_{24}	D_{31}, D_{32}	D_{23}, D_{22}	0

From (20), Table V, and the fact that modes I and III repeat twice in each cycle of fundamental frequency, it can be written as:

$$P_{cond_{FLNPC}} = \frac{56}{12} P_{cond}. \quad (21)$$

In Table VI, all conducting switches are shown for the PFLI topology in each voltage level. Based on (20), Table V, and the fact that modes I and III repeat twice in each cycle of fundamental frequency, we derive the following equation:

$$P_{cond_{PFLI}} = \frac{44}{12} P_{cond}. \quad (22)$$

Finally, from (21) and (22), we derive the following equation:

$$\frac{P_{cond_{PFLI}}}{P_{cond_{FLNPC}}} \cong 79\%. \quad (23)$$

Equation (23) shows that the PFLI topology has lower conduction loss in comparison with the FLNPCI topology. We noted that (20) to (23) are valid for the FLNPCI-ASDC and FLNPCI-SDC topologies. However, I_{on} in (19) is different in these topologies.

V. ANALYSIS OF THE LGC

Most PV panels have a metallic frame that should be grounded to satisfy standards. This frame with wide surface of PV panel constructs a parasitic capacitor. As such, one of its electrodes is PV cells and the other is grounded frame. The value of this parasitic capacitance depends on factors such as PV array and grounded frame surface, distance between PV cell and module, dust, and weather conditions. Parasitic capacitance ranges between some nanofarads and some

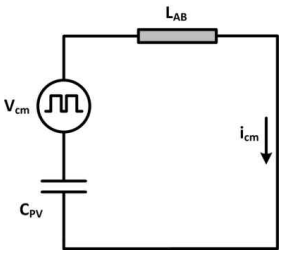

Fig. 8. Common mode model of the studied PV systems.

TABLE VII
COMMON MODE VOLTAGES OF THE PFLI TOPOLOGY

Voltages	V_{AN}	V_{BN}	V_{AB}	V_{cm}
++	$3V_{PV}$	0	$3V_{PV}$	$3/2V_{PV}$
+	$2V_{PV}$	V_{PV}	V_{PV}	$3/2V_{PV}$
−	V_{PV}	$2V_{PV}$	$-V_{PV}$	$3/2V_{PV}$
−−	0	$3V_{PV}$	$-3V_{PV}$	$3/2V_{PV}$

TABLE VIII
COMMON MODE VOLTAGES OF THE FLNPCI-ASDC TOPOLOGY

Voltages	V_{AN}	V_{BN}	V_{AB}	V_{cm}
++	$5V_{PV}$	$2V_{PV}$	$3V_{PV}$	$7/2V_{PV}$
+	$3V_{PV}$	$2V_{PV}$	V_{PV}	$5/2V_{PV}$
−	$2V_{PV}$	$3V_{PV}$	$-V_{PV}$	$5/2V_{PV}$
−−	0	$3V_{PV}$	$-3V_{PV}$	$3/2V_{PV}$

microfarads [20], [21]. When the transformer-less PV system is used to increase efficiency and decrease weight, size, and cost, the isolation between PV panels and grid will be lost. Based on the type of inverter, PV panel, and modulation method, the LGC may exceed the allowed value. This leakage current causes safety problems, increases losses and electromagnetic interference, and injects harmony to the grid [20]-[22]. In other words, the LGC is a common mode current that flows in the ground through a loop. This loop includes PV panel parasitic capacitance, filter elements, inverter, load (grid), and ground. The common mode current and voltage (V_{cm} and i_{cm}) are defined as follows:

$$\begin{cases} i_{cm} = i_A + i_B \\ V_{cm} = \dfrac{V_{AN} + V_{BN}}{2} \end{cases}. \quad (24)$$

Differential mode current and voltage (V_{dm} and i_{dm}) are defined as follows:

$$\begin{cases} i_{dm} = \dfrac{i_A - i_B}{2} \\ V_{dm} = V_{AN} - V_{BN} \end{cases}. \quad (25)$$

In (24) and (25), V_{AN} and V_{BN} are the voltages of A and B terminals related to DC link neutral (N is indicated in Figs. 3 and 7), respectively. In [13] and [23], the common mode model of a PV system is proposed, of which the common mode voltage (CMV) of the system should be constant for non-generating LGC. Equivalent common mode circuit of the

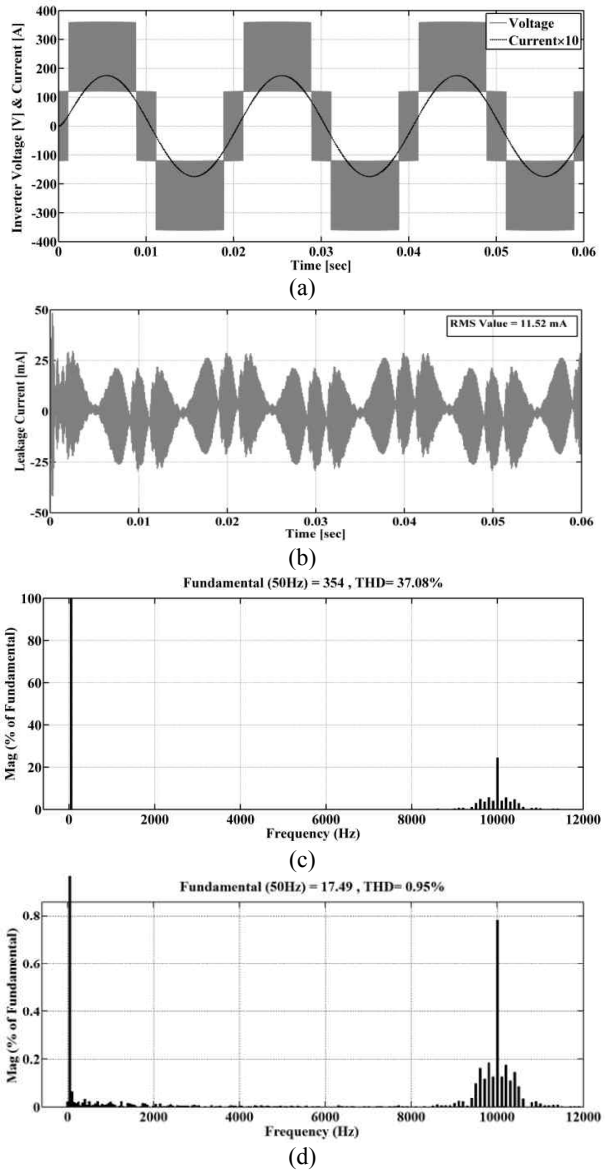

Fig. 9. PFLI waveforms. (a) The inverter voltage and current. (b) The LGC. (c) The THDv. (d) The THDi.

studied topologies is shown in Fig. 8, in which $L_{AB} = L_A \| L_B$. The CMVs of the PFLI and FLNPCI topologies are shown in Tables VII and VIII, respectively. Based on Table VII, we observed that the CMV of the PFLI topology is constant at all times and its LGC is expected to be low. According to Table VIII, the CMV of the FLNPCI-ASDC topology fluctuates at a high frequency and its LGC is expected to be high.

VI. SIMULATION RESULTS

In this section, the PFLI and FLNPCI topologies are compared with each other in terms of output quality, LGC value, and losses. The specifications of the simulated system are shown in Table IX. The PV panel voltages are controlled by means of maximum power point tracker (MPPT). In all simulations, the PV panels are replaced by the ideal DC voltage sources to mitigate the need for MPPT. Based on the

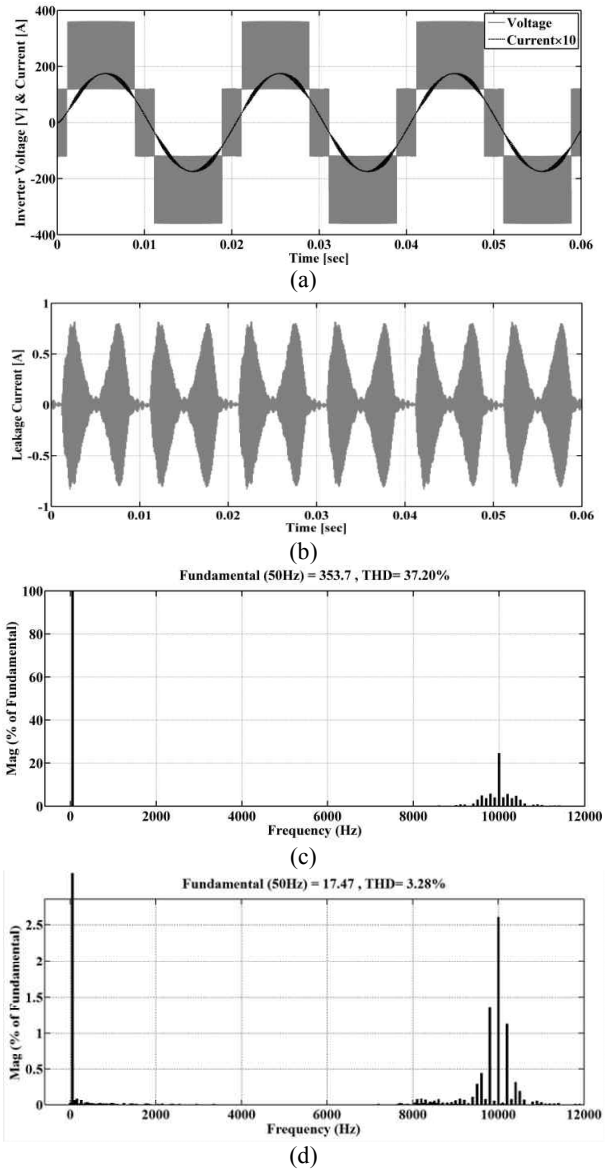

Fig. 10. FLNPCI-ASDC waveforms. (a) The inverter voltage and current. (b) The LGC. (c) The THDv. (d) The THDi.

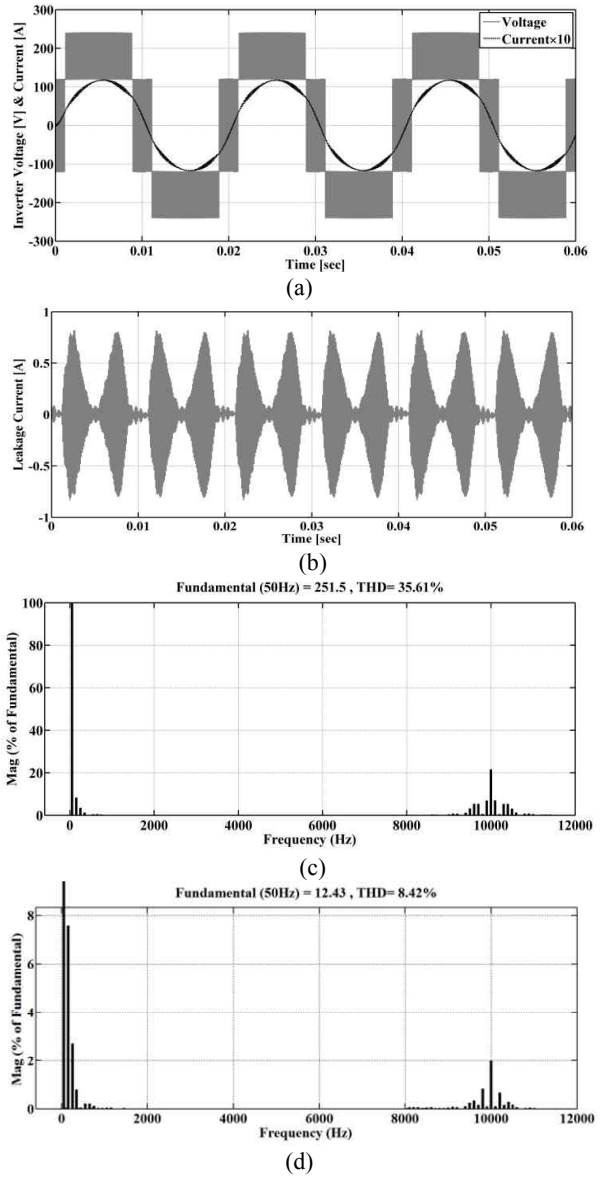

Fig. 11. FLNPCI-SDC waveforms. (a) The inverter voltage and current. (b) The LGC. (c) The THDv. (d) The THDi.

VDE 0126-1-1 German standard, the leakage current must have an amplitude less than 300 mA and a root mean square value of up to 30 mA [24]. Fig. 9(a) shows the voltage and current of the PFLI topology. We observed that this topology could produce a four-level voltage in its output terminals. The LGC of this topology is depicted in Fig. 9(b). As expected, the LGC is low, which can evidently satisfy the VDE 0126-1-1 German standard. As such, the PFLI topology can be used in a transformer-less PV system. Figs. 9(c) and 9(d) show the voltage THD (THDv) and current THD (THDi) of the PFLI topology. We observed that the THDi of the PFLI topology is low. The voltage and current of the FLNPCI-ASDC topology are shown in Fig. 10(a). This topology also produces a four-level voltage in its output terminals. Fig. 10(b) shows the LGC. As expected, the LGC is high, which cannot satisfy the standard. Thus, the FLNPCI-ASDC topology cannot be used in transformer-less PV systems. Figs. 10(c) and 10(d) show the THDv and THDi of the FLNPCI-ASDC topology, respectively. The THDi of the FLNPCI-ASDC topology is higher than that of the PFLI topology. The voltage and the current of the FLNPCI-SDC topology are shown in Fig. 11(a). This topology also produces a four-level voltage in its output terminals, but the magnitudes of the operational modes are not identical. In addition, the maximum output voltage of the FLNPCI-SDC topology is lower than that of the PFLI topology.

In Fig. 11(b), the LGC is illustrated. As expected, the LGC is high, which cannot satisfy the standard. Thus, the FLNPCI-SDC topology cannot be used in transformer-less PV systems. Figs. 11(c) and 11(d) show the THDv and THDi of the FLNPCI-SDC topology. The THDi in the FLNPCI-SDC topology is higher than that of other topologies because

TABLE IX
SIMULATED SYSTEM SPECIFICATIONS

Simulation characteristics	
Voltage of each PV panel (V_{PV})	120 V
PV panel parasitic capacitance (C_{PV})	0.1 μF
DC link capacitors (C)	470 μF
Filter inductance ($L_A = L_B$)	5 mH
Load (R)	20 Ω
Switching frequency (f_s)	10 kHz
Simulation step size	1 μS

TABLE X
SWITCHING, CONDUCTION, AND TOTAL LOSSES

Topology	PFLI	FLNPCI-ASDC	FLNPCI-SDC
P_{swQ} (W)	5.225182	5.97753	2.94375
P_{swD} (W)	0.566537	2.04374	0.802265
P_{cond} (W)	55.8973	81.0395	59.57258
Total losses (W)	61.69	89.061	63.32

the magnitudes of the voltage in operational modes are not identical. To simulate the switching and conduction losses of the studied topologies, the PSIM software (from Powersim Inc.) is used. For IGBTs with freewheeling diodes, the characteristics of IKW30N60T (600 V, 30 A) are used. For diodes, the characteristics of CS240650 (600 V, 50 A) are used. The simulation results of the switching and conduction losses are shown in Table X. Based on Table X, we derive the following equations:

$$\frac{P_{swI\_PFLI}}{P_{swI\_FLNPCI\text{-}ASDC}} = 87.41\%, \tag{26}$$

$$\frac{P_{swD\_PFLI}}{P_{swD\_FLNPCI\text{-}ASDC}} = 27.23\%, \tag{27}$$

$$\frac{P_{cond\_PFLI}}{P_{cond\_FLNPCI\text{-}ASDC}} = 69\%, \tag{28}$$

$$\frac{P_{swI\_PFLI}}{P_{swI\_FLNPCI\text{-}SDC}} = 177.5\%, \tag{29}$$

$$\frac{P_{swD\_PFLI}}{P_{swD\_FLNPCI\text{-}SDC}} = 69.37\%, \tag{30}$$

$$\frac{P_{cond\_PFLI}}{P_{cond\_FLNPCI\text{-}SDC}} = 93.83\%. \tag{31}$$

Notably, the value of (26) is slightly different from (17). However, (27) and (28) have more significant differences from their theoretical values [(17) and (23)]. This finding is due to the fact that the characteristics of the diodes are different from the characteristics of the freewheeling diodes of the IGBTs in the FLNPCI topology. Comparing (29) to (31) and their corresponding theoretical values [(18) and (23)], a high discrepancy between power losses is observed because the output current of the FLNPCI-SDC topology is lower than that of other topologies (see Figs. 9, 10, and 11).

TABLE XI
COMPARISON OF THE STUDIED TOPOLOGIES

Topology	PFLI	FLNPCI -ASDC	FLNPCI -SDC
Number of PV panels	3	5	3
Number of semiconductor devices	20	24	24
Maximum blocking voltage of switches	$3V_{PV}$	$3V_{PV}$	$2V_{PV}$
Maximum output voltage	360 V	360 V	240 V
Switching losses of IGBTs related to PFLI*	1	1.176 (1.144)	_ (0.563)
Switching losses of diodes include freewheeling diodes related to PFLI*	1	3.268 (3.672)	_ (1.441)
Conduction losses related to PFLI*	1	1.266 (1.45)	_ (1.065)
Leakage current	Low	High	High
Current THD (%)	0.95	3.28	8.42

*Values in parentheses are based on the simulation results.

From Table X, we deduced that the total losses of the PFLI topology is lower than those of other topologies.

VII. CONCLUSIONS

In this study, a new inverter topology is proposed for transformer-less PV systems. This topology can generate a four-level voltage in its output terminals, which, in comparison with conventional two-level and three-level topologies, has better quality and easier filtering. Based on the theoretical calculations and simulation results (Table XI), the PFLI topology is superior to the FLNPCI-ASDC topology. The PFLI topology is better than the FLNPCI-SDC topology in terms of the number of semiconductor devices, the maximum output voltage, the conduction and switching losses of diodes, the LGC, and the THDi. The number of PV panels in the PFLI topology is the same as that of the FLNPCI-SDC topology. The maximum switch voltage and switching losses of the IGBTs of the FLNPCI-SDC topology are lower than that of the PFLI topology. Overall, the PFLI topology is superior to the FLNPCI topology because of low construction costs (because of the lower number of switches), low losses, high quality of output waveforms, and suitability for use in transformer-less PV applications (because of low LGC, which decreases the overall losses of the system considerably). In practice, we suggest the use of the previously mentioned semiconductor devices in constructing the PFLI. To control the PFLI, a microcontroller, such as AT91SAM7S256 (ARM-based Flash MCU), is suggested.

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Saeed Yousofi-Darmian was born in Birjand, Iran, in 1989. He received his B.S. and M.S. degrees in Electrical Engineering from the University of Sistan and Baluchestan, Zahedan, Iran, in 2011 and 2013, respectively, graduating with first class honors. He is currently pursuing his Ph.D. degree in the Department of Electrical and Computer Engineering at the University of Sistan and Baluchestan, Zahedan. His research interests include power electronic converters, control of inverters, and photovoltaic systems.

Seyed Masoud Barakati received the B.Sc. and M.Sc., and Ph.D. degrees from Mashhad University, Mashhad, Tabriz University, Tabriz, Iran, and University of Waterloo, Waterloo, Ontario, Canada, in 1993, 1996, and 2008, respectively. He is presently Assistant Professor with the Faculty of Electrical and Computer Engineering at the University of Sistan and Baluchestan, Zahedan, Iran. He had Associate Research position in University of Wisconsin-Madison, USA (2008–2009) and extended visiting Professor positions at the Universities of Ryerson in Toronto and Ecole Polytechnique de Montréal, Canada. His current research interests include power electronic circuits, control systems, renewable energy, FACTS devices, matrix and multilevel converters, and mechatronic systems.