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Mitigation of Voltage Sag and Swell Using Direct Converters with Minimum Switch Count

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Abstract

A new simplified topology for a dynamic voltage restorer (DVR) based on direct converter with a reduced number of switches is presented. The direct converter is fabricated using only three bi-directional controlled switches. The direct converter is connected between the grid and center-tapped series transformer. The center-tapped series transformer is used to inject the compensating voltage synthesized by the direct converter. The DVR can properly compensate for long-duration, balanced, and unbalanced voltage sag and swell by taking power from the grid. The switches are driven by ordinary pulse width modulation signals. Simulation and hardware results validate the idea that the proposed topology can mitigate sag of 50% and swell of unlimited quantity.

Key words: Direct converter, Dynamic voltage restorer (DVR), Pulse width modulation (PWM), Voltage sag, Voltage swell

I. Introduction

Electronic equipment in modern automated industries is generally sensitive to power quality disturbances, such as voltage sag, swell, flicker and harmonics. These disturbances may cause sensitive loads to malfunction or even shut down the entire industrial process, which results in heavy production loss [1]-[3]. One of the major power quality issues is voltage sag caused by the starting of heavy induction motors and short circuit faults [4]-[8]. Voltage sag is a momentary decrease in RMSAC voltage from 0.9p.u. to 0.1 p.u. of the nominal value [4]. Voltage swell is a short-term increase in the RMS value of the AC supply voltage, which ranges from 1.1 p.u. to 1.8 p.u. of the nominal value [7]. Switching large capacitors, the removal of large loads and single phase to ground faults may cause voltage swells [8].

Dynamic voltage restorers (DVR) have been extensively reported in technical literature to investigate their ability to

Manuscript received Mar. 25, 2013; accepted Jul. 13, 2014 Recommended for publication by Associate Editor Kyeon Hur. regulate terminal voltage at critical loads. The basic operation of DVR is to inject a voltage of a required magnitude, phase angle, and frequency in series with the load voltage to mitigate sag and swell [9]-[13].

DVRs can be classified into two major groups with respect to the source of energy employed for compensation. The first group is a conventional DVR with AC/DC/AC converter or DC/AC converter, which requires energy storage elements, such as battery or capacitor banks. These DVRs suffer from disadvantages, such as limited time of compensation, high cost, and bulky energy storage devices [14]-[17]. The second group of DVRs is realized without a DC link using direct AC/AC converters. In [18], a direct converter-based DVR with a boosting transformer ratio of 1:1 was presented in which, five bidirectional switches are used along with the series transformer. Power is fed from all three phases to compensate for voltage sag in any phase. To compensate for swell in one phase, power is fed from the other two phases. A digital signal processor (DSP) was used to compute the compensating voltage and duty ratio of the switches at every sampling instant. The compensation range of voltage sag and swell was only 33% and 100%, respectively.

Among the many direct converter-based DVRs that have been proposed, a matrix converter-based DVR with four bidirectional switches in [19] is a particularly important

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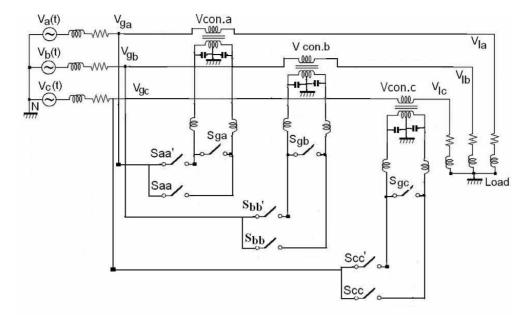


Fig. 1. Proposed DVR topology.

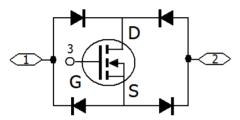


Fig. 2. Bidirectional switch topology.

development because it can compensate for a maximum voltage sag of 25% and a swell of 50% with a 3:1 boosting transformer. In [19], three switches were used during the compensation process to generate the compensating voltage.

II. DVR TOPOLOGY

The proposed DVR topology consists of a direct converter with LC filter and a center-tapped series transformer with a turns ratio of 1:1, as shown in Fig. 1. The direct converter is connected between the grid and center-tapped series transformer such that the direct converter takes the power required for compensation from the grid. The compensating voltage synthesized by the direct converter will be added to the grid through the center-tapped series transformer. Two different output voltages are obtained from the primary of the center-tapped series transformer such that one output voltage will be in phase with the grid voltage and the other output voltage will be out of phase with the grid voltage. In the proposed topology, Saa' is the switch connected in one terminal of the center-tapped series transformer for phase 'a'. When switch Saa' is closed, the output voltage of the centertapped series transformer will be in phase with the phase 'a' voltage. Saa is the switch connected in the other terminal of the center-tapped series transformer. Hence, when the switch Saa' is closed, the output voltage of the center-tapped series transformer will be out of phase with the phase 'a' voltage. Sga is the switch connected across the center-tapped series transformer. When the phase 'a' voltage is at the rated condition, switch Sga is in closed condition to shorten the primary side of the series transformer. If phase 'a' has sag, then the switches Saa' and Sga are alternatively modulated to generate the compensating voltage which is in phase with the grid voltage. If swell is found, then switches Saa and Sga are alternatively modulated to generate the compensating voltage, which will be out of phase with the grid voltage. The compensating voltage is added to the grid through the centertapped series transformer. Each DVR has three bidirectional controlled switches. The topology of the bidirectional switch that was used is shown in Fig. 2. The switches are controlled by a simple pulse width modulation (PWM) technique.

Considering Fig. 1, the following equation can be obtained:

$$v_{ik} = v_{ga} + v_{con.a}$$

 $v_{b} = v_{gb} + v_{con.b}$ (1)
 $v_{ic} = v_{gc} + v_{con.c}$

In (1), l, g, and con subscripts are used for the load, grid, and compensating quantities, respectively. The second subscript refers to the corresponding phases. Assuming sinusoidal waveforms and considering only phase 'a', the voltages can be expressed as follows:

$$\begin{array}{rcl} & v_{i\! k} &= V_{i\! k} & \sin(\omega t\,) \\ & v_{ga} &= V_{ga} & \sin(\omega t\,) \end{array} \tag{2} \\ v_{\varpi n\,,a} &= V_{\varpi n\,,a} & \sin(\omega t\,+\,\emptyset) \end{array}$$

In the aforementioned equations, V_{h} , V_{ga} , and $V_{con,a}$ show the peak values of load, grid, and injected voltages,

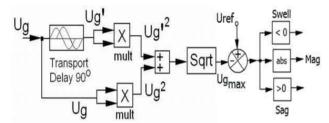


Fig. 3. Sag and swell identification method.

respectively. Ø is the phase angle of the injected voltage and defined as follows:

$$\emptyset = \begin{cases} 0, & \text{for sag} \\ 180 & \text{for swell} \end{cases}$$

III. CONTROL PROCEDURE

A. Sag and Swell Detection

Single-phase d-q theory is used to quantify the voltage sag and swell in each phase. The grid voltage is measured using a potential transformer. This measured grid voltage is given as input to the analog to digital converter (ADC) of the microcontroller. The ADC output is expressed in two forms. One form is the true output as in (4). The other output is delayed by 5ms (or 90°) and can be expressed as in (5).

$$U_g = U_{gm ax} \sin \omega t$$
 (4)

$$U'_{g} = -U_{gm ax} \cos \omega t \tag{5}$$

$$U_{\text{gm ax}} = \sqrt{U_g^2 + U_g'^2}$$
 (6)

 U_{gmax} is computed in the microcontroller using (6), which is illustrated in Fig. 3. U_{gmax} is compared with the reference value to detect voltage sag or swell instantaneously.

B. Voltage Sag Mitigation

In order to compensate the voltage sag, it is necessary to inject voltage in phase with the grid voltage. The centertapped transformer produces two output voltages of different polarities such that one will be in phase and the other will be out of phase with the grid voltage. Therefore, the switches that correspond to synthesis voltage in phase with the grid voltage are chosen. Hence, if voltage sag occurred in phase 'a' then the bidirectional switches Saa' and Sga will be alternatively modulated to mitigate the sag.

A detailed block diagram for switching pulse generation to mitigate voltage sag is shown in Fig. 4. The peak value of grid voltage U_{gmax} is already computed from single-phase d-q transform. U_{ref} is the peak value of the rated voltage, which is a user specified constant value set in the microcontroller program. The difference between the reference voltage U_{ref} and peak value of the grid voltage U_{gmax} provides the amount of voltage sag or swell in the grid. The error signal is compared with the triangular carrier signal to generate the switching pulses. The switching pulses are given to the

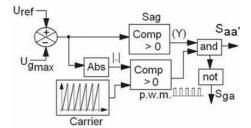


Fig. 4. Block diagram of switching pulse generation.

corresponding switches through the logic gates, as shown in Fig. 4.

C. Voltage Swell Mitigation

Injecting voltage out of phase with the grid voltage is necessary to compensate for voltage swell. Hence, if voltage swell in phase 'a' is observed, then the bidirectional switches Saa and Sga will be alternatively modulated to mitigate the swell. The process of switching pulse generation is the same as that for sag.

IV. COMPENSATING RANGE OF THE DVR

In this section, the compensating range of voltage sag and swell for the proposed topology is calculated. The phase shift from V_g to V_{con} is assumed to be negligible. Moreover, the phase shift from V_{con} to V_l is negligible. The relation between V_g and V_{con} (the filtered output voltage of the converter) can be expressed as follows:

$$V_{con} = DV_{g} \tag{7}$$

In (7), 'D' is the voltage transfer ratio of the direct converters. The above equation is valid because the transformation ratio of the series transformer is 1:1.

A. Voltage Sag Compensating Range

According to Fig. 1, the following is presented for the voltage sag condition:

$$v_l = v_g + v_{con}$$
 (8)

Considering (7), (8) can be rewritten as follows:

$$v_l = v_g (1 + D)$$
 (9)

The voltage sag percentage is defined by

SAG % =
$$\frac{V_l - V_g}{V_l} \times 100$$
 (10)

From (9) and (10), the voltage sag percentage can be simplified to

SAG % =
$$\frac{D}{1+D} \times 100$$
 (11)

TABLE I
SWELL COMPENSATION FOR VARIOUS VALUES OF D

% of Swell	Value of D	% of Swell	Value of D	% of Swell	Value of D
11	0.1	100	0.5	1000	0.91
20	0.17	200	0.67	1150	0.92
30	0.23	300	0.75	1329	0.93
40	0.285	400	0.8	1567	0.94
50	0.335	500	0.835	1900	0.95
60	0.375	600	0.857	2400	0.96
70	0.41	700	0.875	3233	0.97
80	0.445	800	0.89	4900	0.98
90	0.475	900	0.9	9900	0.99

From (11), the maximum value of sag that can be compensated is verified to be 50% for a maximum value of D=1.

B. Voltage Swell Compensation Range

According to Fig. 1, the following is presented for the voltage swell condition:

$$v_l = v_g - v_{on} \tag{12}$$

Considering (7), (12) can be simplified to

$$v_l = v_g (1 - D)$$
 (13)

The voltage swell percentage is defined as follows:

SWELL % =
$$\frac{V_g - V_l}{V_l} \times 100$$
 (14)

From (13) and (14), the voltage swell percentage is simplified as follows:

$$SWELL \% = \frac{D}{1 - D} \times 100 \tag{15}$$

From (15), the unlimited amount of swell can be compensated for a maximum value of D=1. In this method, swell is compensated by feeding the voltage from the same phase. From Table I and (15), the increase in the value of D allows the topology to mitigate a greater amount of swell. Choosing D=1to mitigate an infinite amount of swell is not required because more voltage is available in the phase where swell occurred.

V. SIMULATION RESULTS

The MATLAB/SIMULINK software was used for simulation. Three phase RL load (0.8 power factor lag, 240 VA per phase) were connected to the lines. The desired terminal voltage was set at 60 V rms (1 p.u), 50 Hz.

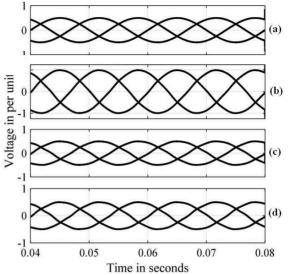


Fig. 5. Mitigation of balanced voltage sag. (a) Grid voltage. (b) Load voltage. (c) Compensation voltage produced by the DVR (PWM). (d) Filtered compensation voltage produced by the DVR.

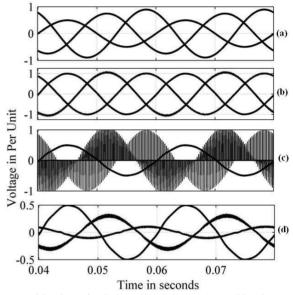


Fig. 6. Mitigation of unbalanced voltage sag.(a) Grid voltage. (b) Load voltage. (c) Compensation voltage produced by the DVR (PWM).(d) Filtered compensation voltage produced by the DVR.

The switching frequency of the converters is 8 kHz. The filter is designed for a cutoff frequency of 1000 Hz with an inductance value of 1.732 mH and capacitance of 15 uF according to the formula $f = 1/(2\pi^*\sqrt{LC})$. The ability of the DVR to mitigate balanced voltage sag of 50% in all the phases is shown in Fig. 5.

Mitigation of 50% unbalanced voltage sag in the 'a' phase, 25% in the 'b' phase, and 10% in the 'c' phase is shown in Fig. 6.

The compensation of balanced swell of 100% is illustrated in Fig. 7. The ability of the DVR to mitigate unbalanced voltage swell of 100% in the 'a' phase, 50% in the 'b' phase, and 25% in the 'c' phase can be observed in Fig. 8.

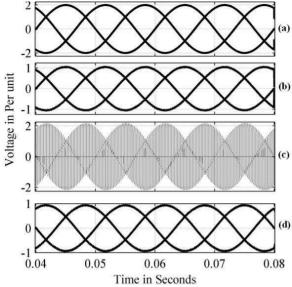


Fig. 7. Mitigation of balanced voltage swell. (a) Grid voltage. (b) Load voltage. (c) Compensation voltage produced by the DVR (PWM). (d) Filtered compensation voltage produced by the DVR.

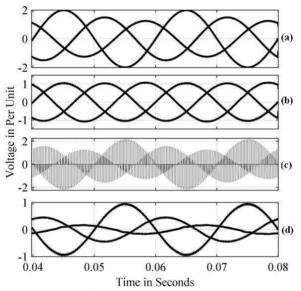


Fig. 8. Mitigation of unbalanced voltage swell. (a) Grid voltage. (b) Load voltage. (c) Compensation voltage produced by the DVR (PWM). (d) Filtered compensation voltage produced by the DVR.

VI. EXPERIMENTAL RESULTS

A three-phase DVR described in this paper was fabricated to verify the design procedure. A photograph of the experimental prototype is shown in Fig. 9. The PIC16F877A microcontroller was used to generate switching pulses. The rating of the center-tapped series transformer is 720 VA, 120 V with a transformation ratio of 1:1. IRFP460 power MOSFET switches with a rating of 500 V, 20 A were used to synthesize the direct converter. The hardware prototype was designed for a normal voltage of 60 V (rms).



Fig. 9. Laboratory prototype.

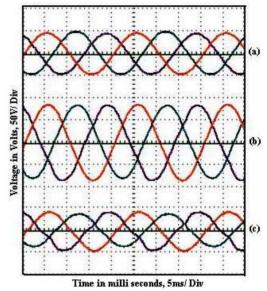


Fig. 10. (a) Grid voltage (balanced sag). (b) Compensated load voltage. (c) Compensating voltage produced by the DVR.

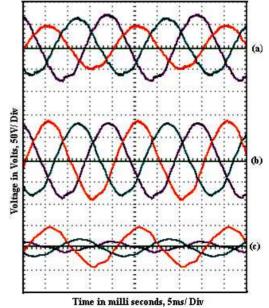


Fig. 11. (a) Grid voltage (unbalanced sag). (b) Compensated load voltage. (c) Compensating voltage produced by the DVR.

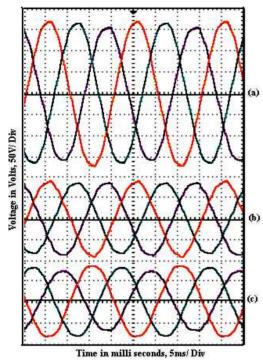


Fig. 12. (a) Grid voltage (balanced swell). (b) Compensated load voltage.(c) Compensating voltage produced by the DVR.

The ability of the DVR to mitigate balanced voltage sag of 50% in all phases is shown in Fig. 10. The compensation for unbalanced voltage sag of 50% in the 'a' phase, 25% in the 'b' phase, and 10% in the 'c' phase can be seen in Fig. 11.

The ability of the DVR to mitigate unbalanced voltage swell of 50% in the 'a' phase, 25% in the 'b' phase, and 100% in the 'c' phase can be observed in Fig. 13. The transient response of the DVR is shown in Fig. 14. The grid voltage is observed to vary instantaneously, while the load voltage remains constant.

VII. PERFORMANCE ANALYSIS

This section compared the proposed topology with the conventional DVR topology and topologies based on direct converters. A topology based on energy storage devices is presented in [17], which has disadvantages, such as a large, bulky, and costly DC link capacitor that requires maintenance and its inability to compensate for long-duration sag and swell. However, the proposed topology is able to compensate for sag and swell for a long time as power is taken from the grid. Moreover, this topology does not need large, bulky, and costly equipment and maintenance as that needed in the DC link capacitor.

In [18], a topology based on direct converters is proposed. This topology has five switches per phase. The switches are controlled based on sampling process as well as require computations throughout the compensation. Using the control algorithm explained in [18], the compensation range of

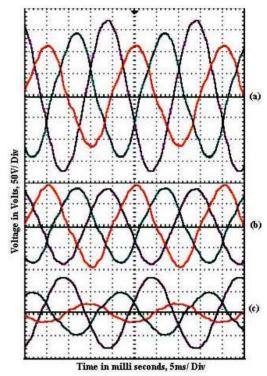


Fig. 13. (a) Grid voltage (unbalanced swell). (b) Compensated load voltage. (c) Compensating voltage produced by the DVR.

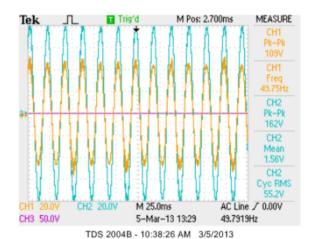


Fig. 14. Transient response of the DVR. (a) Grid voltage (inner waveform). (b) Compensated load voltage.

voltage sag is 33% and voltage swell is 100%.

In [19], a topology for a single-phase DVR based on a single-phase matrix converter was presented with four switches per phase. The compensation range is 25% for voltage sags and 50% for swells. In this topology, during compensation three switches are modulated. So generation of switching pulses is complicated and switching losses are also increased.

In [20], a DVR based on an indirect matrix converter was presented for balanced voltage sag compensation of 60%. This topology needs flywheel energy storage element.

S.No	Converter Topology	Compensation Range		PWM Technique Used	No. of Switches
		Sag	Swell	r www rechnique Osed	No. of Switches
1	Direct converter [18]	33%	100%	Pulse width is computed during each switching period	5
2	Matrix converter [19]	25%	50%	Ordinary PWM	4
3	Indirect matrix converter with flywheel energy storage [20]	60%	Nil	Ordinary PWM	5
4	Proposed converter	50%	Unlimited	Ordinary PWM	3

TABLE II
COMPARISON AMONG VARIOUS DVR TOPOLOGIES

However, the capability of the topology in voltage swell compensation has not been investigated.

In this work, a center-tapped series transformer is used with three bidirectional switches such that only two switches are modulated during compensation. Hence, switching loss is less and switching pulse generation is easier. In this topology, switches are controlled by ordinary PWM. Consequently, computation is avoided and control is simpler. The compensating range of voltage sag is 50% and voltage swell is unlimited, as mentioned in Table II. This paper proposes a new, simplified, rugged, effective, and practical method of sag and swell mitigation. This method involved a reduced number of switches without energy storage systems. Only a few publications on topologies with direct converters are available despite the many literature surveys on topologies based on energy storage devices. The proposed topology is a novel, simplified, rugged, and reliable topology based on direct converters with reduced switches reported in the literature surveys.

VIII. CONCLUSIONS

A three-phase DVR based on direct converters was presented. This DVR does not require the DC link unlike conventional DVRs. The absence of the DC link reduces the cost, weight, and volume of the DVRs as well as avoids maintenance of energy storage devices. The DVR in each of the three-phase lines is constructed using only three bidirectional switches. The DVR is controlled by using a simple PWM procedure. The DVR can effectively mitigate 50% of balanced and unbalanced voltage sagas well as an unlimited amount of balanced and unbalanced voltage swell. The presented topology uses only three switches, with one center-tapped series transformer for each phase for effective compensation with simple control logic.

REFERENCES

- [1] J. Arrillaga, N. R. Watson, and S. Chen, *Power System Quality Assessment*, Wiley, 2000.
- [2] W. E. Brumsickle, R. S. Schneider, G. A. Luckjiff, D. M. Divan and M. F. McGranaghan, "Dynamic sag correctors: Cost-effective industrial power line conditioning," *IEEE*

- Trans. Ind. Applicat., Vol. 37, No.1, pp.212-217, Jan./Feb. 2001
- [3] M.H.J.Bollen, Understanding Power Quality Problems: Voltage Sags and Interruptions, IEEE Press, 1999.
- [4] J. G. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," *IEEE Trans. Power Electron.*, Vol. 19, No.3, pp. 806-813, May2004.
- [5] N. H. Woodley, "Field experience with dynamic voltage restorer (DVRTMMV) systems," in *Proc. IEEE Power Eng. Soc.*, *Winter Meeting. Conf.*, pp. 2864-2871, 2000.
- [6] N. H. Woodley, L. Morgan, and A. Sundaram, "Experience with an inverter-based dynamic voltage restorer," *IEEE Trans. Power Del.*, Vol. 14, No. 3, pp. 1181-1186, Aug. 1999.
- [7] C. Zhan, A. Arulampalam, and N. Jenkins, "Four-wire dynamic voltage restorer based on a three-dimensional voltage space vector PWM algorithm," *IEEE Trans. Power Electron.*, Vol.18, No. 4, pp. 1093-1102, Jul. 2003.
- [8] B. Wang, G. Venkataramanan, and M. Illindala, "Operation and control of a dynamic voltage restorer using transformer coupled H bridge converters," *IEEE Trans. Power Electron.*, Vol. 21, No. 4, pp.1053-1061, Jul. 2006.
- [9] P. R. Sanchez, E. Acha, J. E. O. Calderon, V. Feliu, and A. G. Cerrada, "A versatile control scheme for a dynamic voltage restorer for power-quality improvement," *IEEE Trans. Power Del.*, Vol. 24, No. 1, pp. 277-284, Jan. 2009.
- [10] P. Boonchiam and N. Mithulananthan, "Dynamic control strategy in medium voltage DVR for mitigating voltage sags/swells," in *Proc. PST*, pp. 1-5, 2006.
- [11] B. Singh, P. Jayaprakash, and D. P. Kothari, "Adaline-based control of capacitor supported DVR for distribution system," *Journal of Power Electronics*, Vol. 9, No. 3, pp. 386-395, May 2009.
- [12] G. Teng, G. Xiao, L. Hu, Y. Lu, and Y. R.Kafle, "Control strategy based on equivalent fundamental and odd harmonic resonators for single-phase DVRs," *Journal of Power Electronics*, Vol. 12, No. 4, pp. 654-663, Jul. 2012.
- [13]M.-B.Kim, S.-H.Lee, G.-W.Moon and M.-J.Youn, "Synchronous PI decoupling control scheme for DVR against a voltage sag in the power system," *Journal of Power Electronics*, Vol. 4, No. 3, pp. 180-187, Jul. 2004.
- [14] H. K. Al-Hadidi, A. M. Gole, and D. A. Jacobson, "A novel configuration for a cascade inverter-based dynamic voltage restorer with reduced energy storage requirements," *IEEE Trans. Power Del.*, Vol. 23, No. 2, pp. 881-888, Apr. 2008.
- [15] Y. W. Li, D. M. Vilathgamuwa, F. Blaabjerg, and P. C. Loh, "Investigation and improvement of transient response of

- DVR at medium voltage level," *IEEE Trans. Ind. Appl.*, Vol. 43, No. 5, pp.1309-1319, Sep./Oct. 2007.
- [16] C. Meyer, R. W. De Doncker, Y. W. Li, and F. Blaabjerg, "Optimized control strategy for a medium-voltage DVR-Theoretical investigations and experimental results," *IEEE Trans. Power Electron.*, Vol. 23, No.6, pp. 2746-2754, Nov. 2008.
- [17] D. M. Vilathgamuwa, A. A. D. R. Perera, and S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer," *IEEE Trans. Power Del.*, Vol. 18, No. 3, pp. 928-936, Jul. 2003.
- [18] E. Babaei, M. F. Kangarlu, and M. Sabahi, "Mitigation of voltage disturbances using dynamic voltage restorer based on direct converters," *IEEE Trans. Power Del.*, Vol. 25, No. 4, pp.2676-2683, Oct. 2010.
- [19] J. Perez, V. Cardenas, L. Moran, and C. Nunez, "Single phase ac-ac converter operating as a dynamic voltage restorer (DVR)," in *Proc. IECON*, pp. 1938-1943, 2006.
- [20] B. Wang and G. Venkataramanan, "Dynamic voltage restorer utilizing a matrix converter and flywheel energy storage," *IEEE Trans. Ind. Appl.*, Vol. 45, No. 1, pp. 222-231, Jan./Feb. 2009.



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