JPE 14-6-28

http://dx.doi.org/10.6113/JPE.2014.14.6.1345
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Experimental Investigations for Thermal Mutual Evaluation in Multi-Chip Modules

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Abstract

The thermal behavior of power modules is an important criterion for the design of cooling systems and optimum thermal structure of these modules. An important consideration for high power and high frequency design is the spacing between semiconductor devices, substrate structure and influence of the boundary condition in the case. This study focuses on the thermal behavior of hybrid power modules to establish a simplified method that allows temperature estimation in different module components without decapsulation. This study resulted in a correction of the junction temperature values estimated from the transient thermal impedance of each component operating alone. The corrections depend on mutual thermal coupling between different chips of the hybrid structure. A new experimental technique for thermal mutual evaluation is presented. Notably, the classic analysis of thermal phenomena in these structures, which was independent of dissipated power magnitude and boundary conditions in the case, is incorrect.

Key words: 3D numerical simulation, Hybrid power module, Superposition method, Thermal influence measurement, Transient thermal impedance measurement

I. INTRODUCTION

Power semiconductor devices are currently undergoing rapid evolution. The compactness and power handling capability of power converting circuits in modern power electronics is currently being improved by hybrid power integration and related packaging techniques.

Shammas et al. [1] proposed a 1D method to determine the junction temperatures of different components in the module without considering the thermal influences between them. Hamidi et al., Khatir et al., and Carubelli et al. [2]-[4] developed a method that can determine the temperature distribution in a module by supposing that thermal resistance is constantly independent of the boundary conditions at the module baseplate and powers dissipated in the components.

This paper presents these problems to establish a simplified method based on an experimental study that can estimate the temperature in different components of the module by considering the boundary conditions and thermal influences without decapsulation.

We studied the thermal behavior of each component and hybrid structure operating alone in the first part of this paper. The numerical simulator COSMOS/M [5] is then used to perform 3D finite element simulations. The thermal impedance Z_{th} (t) between the junction and case of each module device is compared with the thermal impedance deduced from the manufacturer data sheet to validate the proposed technique.

The thermal behavior of each component according to the device boundary conditions at the module case is studied in the second part of the paper.

An experimental technique is proposed to estimate the maximum junction temperature (in the IGBT and the DIODE) based on thermo-sensitive parameter measurements. The 3D finite element thermal simulations were conducted to observe and analyze the temperature evolution in the IGBT and DIODE under study.

The third part of the paper considers the thermal behavior of the global hybrid power module. The thermal interaction

Manuscript received Feb. 23, 2014; accepted Jul. 11, 2014
Recommended for publication by Associate Editor Trillion Q. Zheng.
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between the module devices is studied. An experimental technique for thermal mutual evaluation between different chips of the hybrid structure is developed. This technique is based on the measurement of the IGBT and DIODE thermo-sensitive parameters. The superposition technique is proposed to approximate the device temperature value increase caused by the thermal mutual phenomenon.

The presented results validate the introduced technique to estimate the exact temperature even in the presence of several components that work simultaneously.

II. THERMAL BEHAVIOR OF THE STUDIED MODULE

A. IGBT Module Structure

IGBT and diode chips in classical IGBT modules are soldered onto the metallized ceramic substrates (alumina or AlN) by using soft solders. These ceramics provide electrical insulation to the underlying baseplate, which is usually pressure mounted onto a heat sink by peripheral bolts.

The construction features of the IGBT module is summarized as follows:

- Subassembly: Many small IGBT and diode devices have to be connected in parallel to reach high current levels. Therefore, building a fully functional subassembly first is mandatory. This subassembly contains only several devices (IGBTs and diodes) soldered to the ceramic substrate. The subassembly can be fully tested for all static and dynamic parameters. Yield losses, which can occur because of insufficient switching properties, will thus lead to material loss in the early stage of the assembly process. Only fully functional subassemblies will be used to build a module.

- Substrate: The thickness of the ceramic substrate, which isolates electrical and thermal contacts, has to be larger than 1 mm to achieve high isolation and partial discharge voltage. This condition excludes the widely used DCB aluminum oxide. AlN is preferable and has higher thermal conductivity by a factor of 5 to 10.

- Baseplate: The baseplate usually consists of thick copper or a relatively thin aluminum silicon carbide plate. The thickness of the baseplate is considered to ensure that the baseplate remains in shape during the assembly process (i.e., when soldering the subassemblies to the base) and later in the mechanical assembly sequence of the power electronic system. The contact impedance between the IGBT module and heat sink is also considered for selection of the baseplate thickness.

Our study was conducted on a Semikron module SKM 75 GB 123D (75 A/1200 V) shown in Fig. 1.

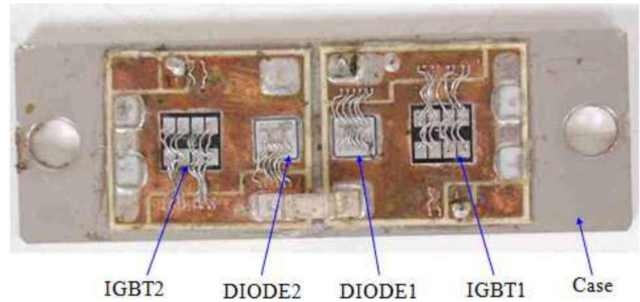

Fig. 1. Numerical photo of the studied IGBT module (SKM75GB123D) layout.

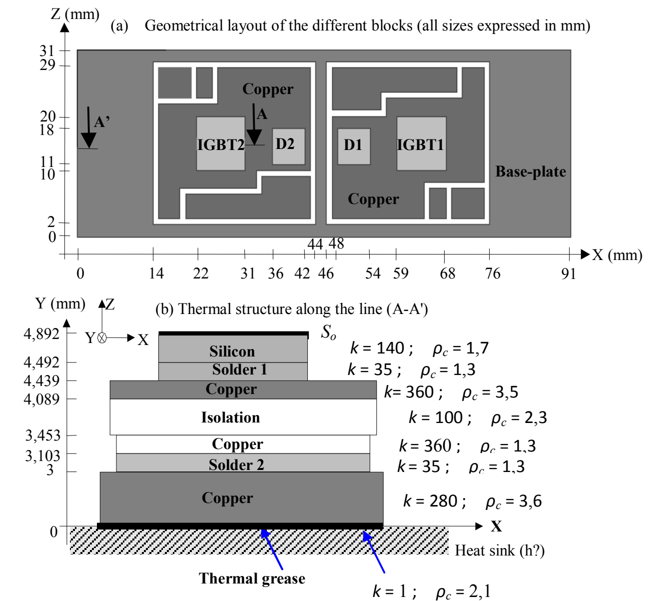

Fig. 2. Geometrical description and thermal structure of the studied IGBT module (SKM75GB123D). k : in $W.K^{-1}.m^{-1}$ and ρ_C : in $j.K^{-1}.cm^{-3}$.

Each component is made up of a silicon chip. The components set of the module is distributed exactly as shown in Fig. 2(a).

The module structure (SEMIPACK) [6] contains seven layers of different materials. Each layer is characterized by its thickness L_i, its thermal conductivity k_i, and its thermal capacity ρ_{Ci} [Fig. 2(b)] [7]-[10].

B. Transient Thermal Impedance of Each Component

The essential input value that characterizes the thermal behavior in the power component is the transient thermal impedance $Z_{th}(t)$ between the junction and case. This value can be derived from the following formula based on the power dissipation [11], [12]:

$$\Delta T(t) = \int_0^t P(\tau)\, \dot{Z}th(t-\tau) \tag{1}$$

where $\Delta T = T_{j\,max}(t) - T_c$, $T_{j\,max}(t)$ is the hot spot temperature (junction temperature), T_c is the bottom temperature of the

case, $P(t)$ is the dissipated power on the top surface of the device, and $Z_{th}(t)$ is the time derivative of $Z_{th}(t)$. The concept of Eq. (1) can be used to correlate the junction temperature rise at any instant and amount of the average power dissipating level. Z_{th} reaches the junction-to-case thermal resistance, R_{th} in the steady-state conditions.

The thermal impedance can be written as follows [13]–[15] in the particular but practical cases of power losses with rectangular waveforms featuring amplitude P and linear assumption:

$$Z_{th}(t) = \frac{T_{j\max}(t) - T_c(t)}{P} \tag{2}$$

1) Conventional Study of Module Thermal Impedance: The manufacturer's technical data were used to determine the thermal impedances of the different module elements (Fig. 3, curves 2). These curves are provided for isothermal conditions and working alone. Considering the boundary conditions and thermal influence, the structure was generated by using the module shown in Fig. 2 in the 3D simulator to highlight the inadequacy of using these impedances. This model will be proposed as a reference in future work.

The 3D finite element simulations are investigated to observe the transient evolutions of the thermal impedance and study the thermal behavior of each module component that operates alone. The obtained results are compared with those provided by the manufacturer data sheet.

COSMOS/M numerical simulator is used to implement the studied module, and a module region of 91 mm × 31 mm × 4,892 mm is modeled. This software is based on calculations with the finite element method.

COSMOS/M is used as a suitable simulation tool to calculate the junction temperature and the transient thermal impedance evolution of devices. Mesh size is selected carefully to resolve the internal details of the IGBT module. Numerical tests that use different refinement methods are executed to determine the optimum mesh size. Manual mesh refinement is performed in the high gradient temperature region such as silicon devices and solder layers.

The top area of the device is divided into 91 × 31 cells that can discretize the (0,9 × 0,9) cm^2 active area of the IGBT chip into 81 (9 × 9) elementary cells and (0,6 × 0,6) cm^2 active area of the DIODE chip into 36 (6 × 6) elementary cells.

Power is assumed to be dissipated on the top surface of the chip (device active region) in the case of the studied devices (vertical structure). Heat flows from the top surface to other directions especially in a perpendicular direction.

A variable "discretization" step value is used, which is weak in the most active parts of the module (around the active chip) and much higher. The thickness of the module is divided into 60 elements. The final structured mesh of the module has 51884 elements and 57290 nodes.

Thermal conductivity in silicon is assumed to be non-linear and equal to the following [16]:

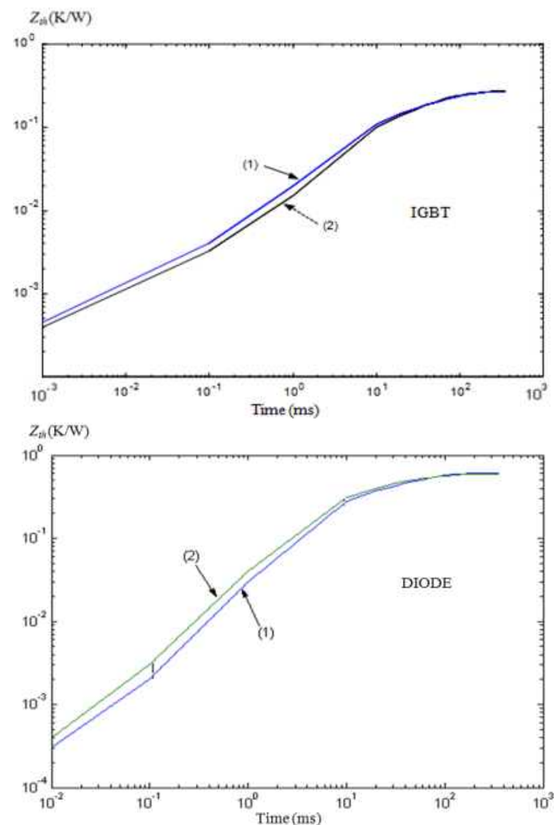

Fig. 3. IGBT and DIODE thermal impedance responses, (1): obtained by 3D numerical simulations; (2): deduced from the manufacturer data sheet.

$$k_S(T) = k_0 \left(\frac{300}{T} \right)^{\frac{4}{3}} \tag{3}$$

where

k_0: Silicon thermal conductivity at 300 K (= 1,548 Wcm^{-1}K^{-1}).

T: Absolute temperature (K).

First, the isothermal condition is assumed at the copper pad of the module and the lower surface of the device is fixed at 300 K. This condition is consistent with the conditions used by the manufacturer to provide transient thermal impedance evolutions in the data sheet. The dissipated power in the IGBT is equal to 90 W and uniformly distributed in the active surface of the device (operating alone in the module). Adiabatic conditions are imposed on the other module area.

Fig. 3 shows the evolution of the thermal impedance Z_{th} between the junction and baseplate obtained by numerical simulations. This evolution is similar to the thermal impedance evolution provided by the manufacturer data sheet.

The thermal impedance response of the diode is shown in Fig. 3 in the same boundary condition and with a step of dissipated power in the diode equal to 40 W. These results indicate considerable agreement between the 3D numerical simulation and manufacturer data sheet in the case of isothermal conditions. The difference between the two results (Fig. 3) is due not only to the dissipated power being uniformly distributed on the top surface of the device, but also to the thermal characteristics of the module's superposed

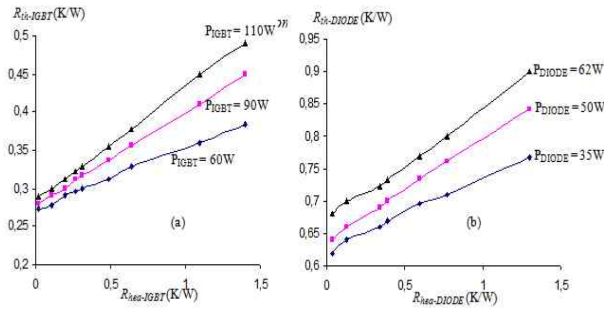

Fig. 4. Junction to baseplate thermal resistance evolution according to the component dissipated powers and case boundary conditions obtained by 3D numerical simulations (a): IGBT, (b): DIODE.

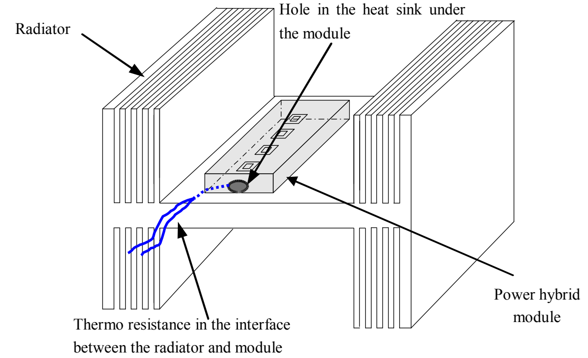

Fig. 5. Used cooling system and case temperature measurements procedure.

materials that are almost unknown. The obtained results are acceptable, and the thermal behavior of the simulated structure is correct despite these differences.

C. Effects of Boundary Conditions and Power Dissipation of Thermal Resistances

We proposed the 3D model already presented in Section §.II.2.1 to highlight the effects of boundary conditions and power dissipation on thermal impedances. The proposed methodology involves calculating the thermal resistance for a fixed condition while varying the boundary conditions on the base module power. The same calculations are made for different dissipated powers.

Fig. 4 shows the effect of the boundary conditions at the module baseplate on the effective thermal resistance of each device. These characteristics are deduced from different device-dissipated powers and obtained through 3D numerical simulations. The thermal resistances of the devices increase when the dissipated power and equivalent heat sink resistance increases.

The heat sink resistance values of $R_{hea\text{-}IGBT}$ and $R_{hea\text{-}DIODE}$ correspond to the equivalent thermal resistance between the baseplate (just below the component under test) and ambient air.

The thermal resistance can be approximated by the following simple polynomial function as follows based on the characteristic of Fig. 4:

$$R_{th\text{-}IGBT} = a_1 P_{IGBT} R_{hea\text{-}IGBT} + a_2 \quad (°C/W) \tag{4}$$

$$R_{th\text{-}DIODE} = b_1 P_{DIODE} R_{hea\text{-}DIODE} + b_2 \quad (°C/W) \tag{5}$$

where

$R_{th\text{-}IGBT}$ and $R_{th\text{-}DIODE}$: Thermal resistance between the junction and case of the IGBT and DIODE, respectively (°C /W).

P_{IGBT} and P_{DIODE}: Dissipated power in the IGBT and DIODE, respectively (W).

$a_1 = 1{,}3 \times 10^{-3}(W^{-1})$; $a_2 = 0{,}28(°C/W)$; $b_1 = 3{,}2 \times 10^{-3}(W^{-1})$; $b_2 = 0{,}6(°C/W)$.

D. Proposed Technical Measure of the Thermal IGBT Transient Thermal Impedance

Maintaining the module case temperature at a constant value (isothermal condition) during the module operation is difficult in practice because it is performed with numerical simulations. The transient thermal impedance evolutions in the case of isothermal conditions at the module baseplate are then not useful given the manufacturer data sheet. Subsequently, the module will be fixed to a heat sink as shown in Fig. 5. A thermo-resistance is placed in a hole in the heat sink at the interface with the module baseplate. The experimental estimation of the hottest area temperature inside an IGBT is based on suitable and measurable parameters. The hottest area that leads to device destruction is located at the end of the IGBT channel region with a high current density. The threshold voltage V_{th} is proposed in [17], [18] as a parameter depending on the channel temperature. A critical problem of this technique is the small dependence on temperature, i.e., a small variation range. The measurement of V_{th} also implies fine control of the voltage V_{GS} to ensure low current density inside the device.

The channel temperature can also be estimated by measuring the saturation current for a high gate-to-source voltage value [19]. The results are not unique because they depend on circuit parameters. Temperature calibration of the saturation current may not be performed without power losses in the self-heating process of the device. A third method is proposed and is based on IGBT saturation current (I_{sat}) measurement but at a low voltage V_{GS} (slightly larger than V_{th} at room temperature). This technique produces an accurate result [20]. Thus, this method is considered to estimate the maximal junction temperature in the IGBT. This measurement method requires temperature calibration of saturation current I_{sat} without including self-heating in the device.

An essential characteristic to estimate the hottest temperature in the IGBT is in the calibration curve, which involves taking the saturation current for different temperatures in the component. The module is heated from the outside by an electric oven. The ambient temperature is measured by a thermocouple that is fixed inside the oven. All

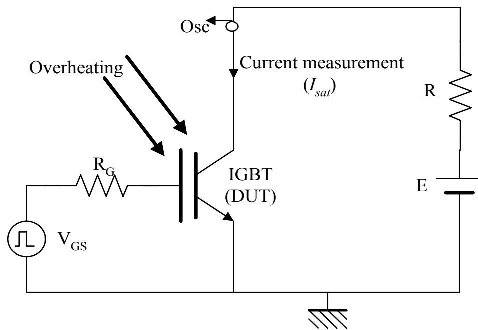

Fig. 6. Experimental electric circuit proposed for the IGBT thermo-sensitive parameter calibration (E = 18 V and R = 2,2 Ω, V_{GS} = 6 V).

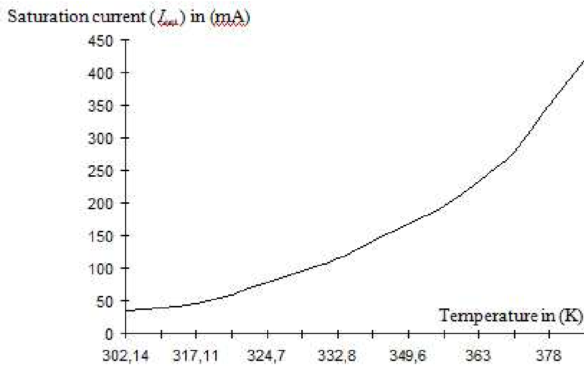

Fig. 7. Experimental evolution of the calibration curve corresponding to the IGBT saturation current (I_{sat}) (V_{GS} = 6 V).

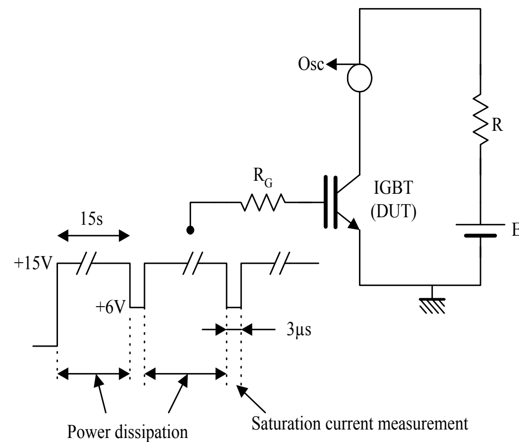

Fig. 8. Experimental circuit proposed for the IGBT saturation current measurements during the heating phase (E = 18 V and R = 2,2 Ω).

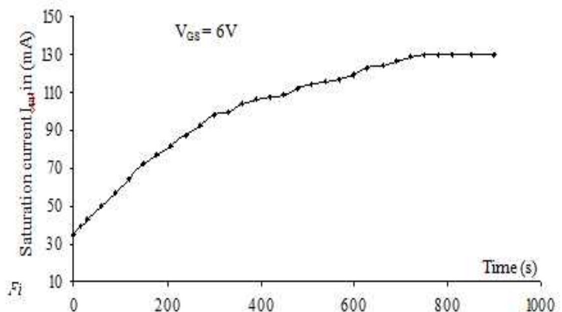

Fig. 9. Experimental response of the IGBT saturation current during the heating phase.

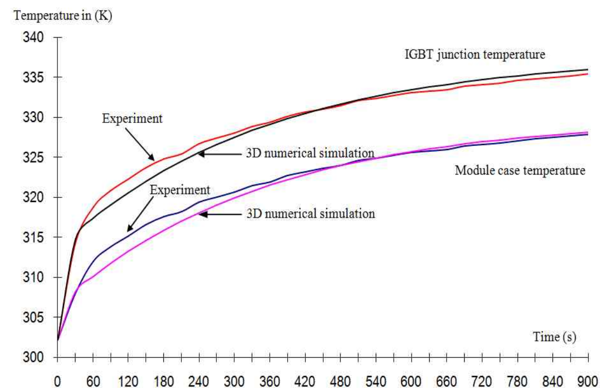

Fig. 10. IGBT junction temperature and case temperature evolutions obtained by experiments and 3D numerical simulations (dissipated power in IGBT = 27 W).

points of the module IGBT have the same temperature under these conditions. Fig. 6 shows the measurement setup for thermo-sensitive parameter I_{sat}. A heated flow generator controls the module temperature by maintaining the temperature in the IGBT homogeneous. Fig. 7 shows the experimental temperature calibration curve for: $I_{sat} = i_A$ (E = 18 V, R = 2.2 Ω, V_{GS} = 6 V).

We proposed a simple technique based on the measurement of the saturation current and principle shown in Fig. 8 to measure the thermal impedance of the IGBT.

The driving signal of the device under test is a periodic signal with a high duty cycle value. If the V_{GS} voltage magnitude is equal to 15 V, the IGBT is in the ON state (linear region of the I(V) characteristic) and power is dissipated on it. The magnitude of the dissipated power in our case is approximately 27 W. The device under test is biased in the saturation region with a low V_{GS} (V_{GS} = 6 V) every 15 seconds and during a very short duration (several microseconds).

The saturation currents of the IGBT and case temperature are registered during this period. The maximum temperature reached in the IGBT can be deduced from the calibration curve in Fig. 7. The variation of the internal averaged temperature on the top surface of the component is neglected for a few microseconds. The saturation current response because of the power dissipation of 27 W in the IGBT is shown in Fig. 9.

Fig. 10 shows the transient temperature evolutions at the IGBT junction and module case (under the tested chip) obtained by experiments and 3D numerical simulations. Good agreement is shown between these two results. This scenario proves that the simulated structure of the studied module is correctly modeled in the COSMOS/M simulator. The results obtained from these numerical simulations can also be considered a reference in our study.

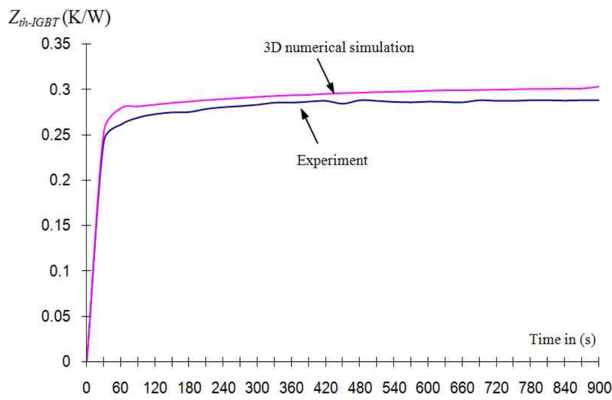

Fig. 11. IGBT transient thermal impedance evolutions obtained by experiments and 3D numerical simulations (dissipated power in IGBT = 27 W).

Fig. 11 shows the IGBT transient thermal impedance evolutions deduced from the junction and case temperature responses.

Comparing the transient thermal impedance evolutions obtained by using our technique with those deduced from the module data sheet (with 333 K isothermal condition at the module case shown in Fig. 3), we can conclude that the transient thermal impedance value in the steady-state phase in the first case is higher than that obtained by the data sheet. Thus, the transient thermal impedance between the junction and case of the IGBT in the multi-chip structure depends mainly on boundary conditions at the module case. This condition is due to the importance of the 3D thermal phenomenon in the module structure. Thermal investigations in the module structure using the manufacturer data sheet and thermal characteristics are incorrect.

E. Proposed Technical Measure of the Thermal DIODE Transient Thermal Impedance

The experimental estimation of the diode's highest temperature is based on the measure of electric thermo-sensitive parameters. This estimation is considered to measure the drop voltage in the on-state (V_j) during the heating phase of the device [20]. The electric circuit proposed for this experiment is shown in Fig. 12. When the switch (*I*) is turned on, an important current (heating phase) flows in the diode. The diode's dissipated power step value is equal to 9.5 W in our case. The driving signal of the switch (*I*) is periodic (15 seconds) with a high duty cycle value. The switch (*I*) is opened during a short time, the diode is biased with a very low current value (few milliamperes), and the drop voltage across the diode (V_j) is registered every 15 seconds. The baseplate temperature (case temperature) is simultaneously performed with the thermo-resistance.

An essential characteristic required to estimate the junction temperature in the diode is the drop voltage calibration curve. Fig. 13 shows the proposed circuit to measure the thermo-sensitive parameter V_j as function of device

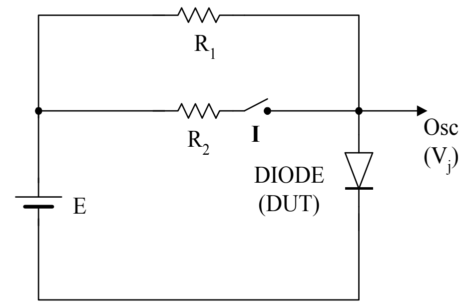

Fig. 12. Electric circuit proposed to measure the diode drop voltage during the heating phase (R_1 = 300 Ω, R_2 = 1,8 Ω and E = 12 V).

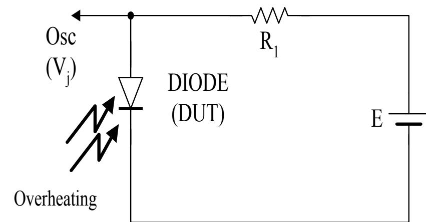

Fig. 13. Proposed electric circuit for diode thermo-sensitive parameter calibration (R_1 = 300 Ω and E = 12 V).

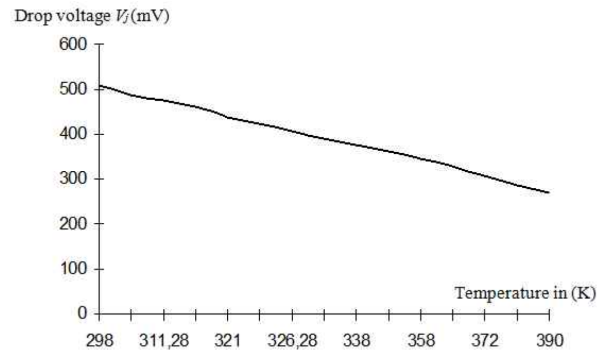

Fig. 14. Experimental evolution of the diode on-state drop voltage against temperature.

temperature. A heat flow generator controls the module temperature that is supposed to be homogeneous in the structure.

Fig. 14 shows the experimental (thermal resistance) and thermal response time temperature calibration curve for the following:

V_j (E = 12 V, R_1 = 300 Ω).

Fig. 15 shows the thermal responses of the diode junction temperature and case temperature evolutions obtained by the fine simulations (3D) and experiments. Good agreement between both results is observed. The obtained results prove that the simulated structure (in COSMOS/M simulator) corresponds mainly to the real module structure. The transient thermal impedances between the junction and case of the diode deduced from Fig. 15 are shown in Fig. 16.

Through a comparison of the transient thermal evolutions obtained with our technique, the 3D numerical simulations,

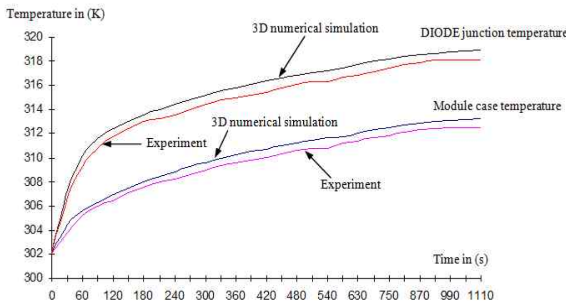

Fig. 15. DIODE junction temperature and case temperature evolutions obtained by experiments and 3D numerical simulations (dissipated power in the DIODE = 9.5 W).

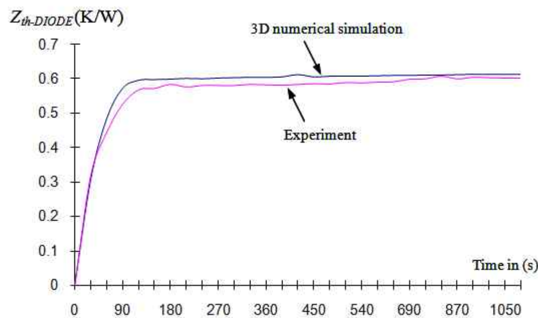

Fig. 16. DIODE transient thermal impedance evolutions obtained by experiments and 3D numerical simulations (Dissipated power in the DIODE = 9,5 W).

and those provided by the data sheet (with isothermal condition at the module baseplate), a discrepancy between the two types of evolutions is observed. The thermal impedance provided by the manufacturer does not present any benefit for users. The module baseplate temperature varies when the module operates. The classical thermal analysis of the thermal behavior in the power devices independent of boundary conditions on the case is incorrect. An experimental setup and multidimensional thermal analysis in multi-chip structure are necessary to determine the real value of different temperatures.

III. THERMAL INFLUENCES IN HYBRID STRUCTURES

The second objective of our study is to study thermal influence in the module. We introduced a simple technique to accurately estimate the thermal influences between components without module decapsulation.

A. *Proposed Technical Measure of Thermal Influence*

The heating flow spreads out vertically to the module baseplate and laterally from the heating source during power feeding into the chip.

Thus, mutual coupling of the different chip occurs inside the module. Fig. 17 shows the temperature map on the top surface of the module obtained by 3D numerical simulations.

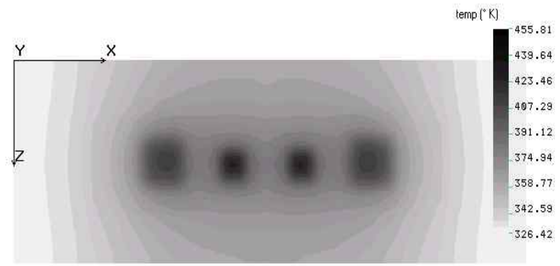

Fig. 17. Temperature map on the top surface of the module (operating in inverter condition) obtained by 3D numerical simulation *(P_{IGBT1} = P_{IGBT2} = 200 W; P_{DIODE1} = P_{DIODE2} = 120 W).*

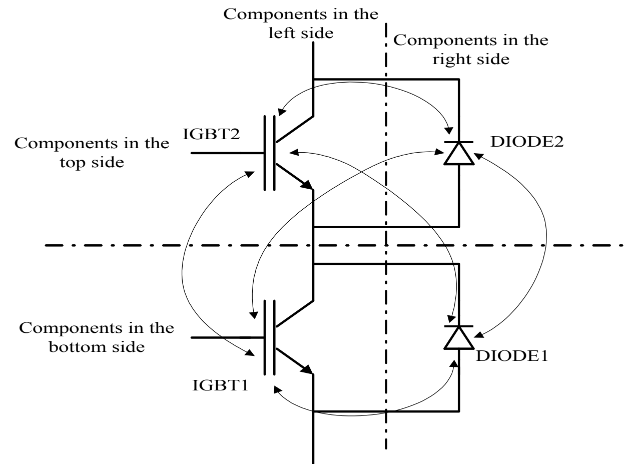

Fig. 18. Different thermal influences between the module components.

The thermal influences between components can exist when the adjacent devices operate together. This thermal interaction depends mainly on the following [21]-[31]:

- Dissipated power value in the different components
- Silicon chip disposition
- Boundary condition at the heat spreader

Fig. 18 shows the possible thermal influences between the different components of the studied module. These influences are as follows:

- Between the components on the top side of the circuit and others on the bottom side
- Between the components on the right side and others on the left side of the circuit

3D finite element simulations were conducted to study the thermal influences between the different module components. The obtained results will be the device-dissipated power and different cases of boundary conditions. The developed experimental technique for estimating the thermal influences caused by the different chips in the hybrid structure is based on the measure of the IGBT and DIODE thermo-sensitive parameters. The component under the dissipated power causes the heating of its neighborhood. The thermo-sensitive

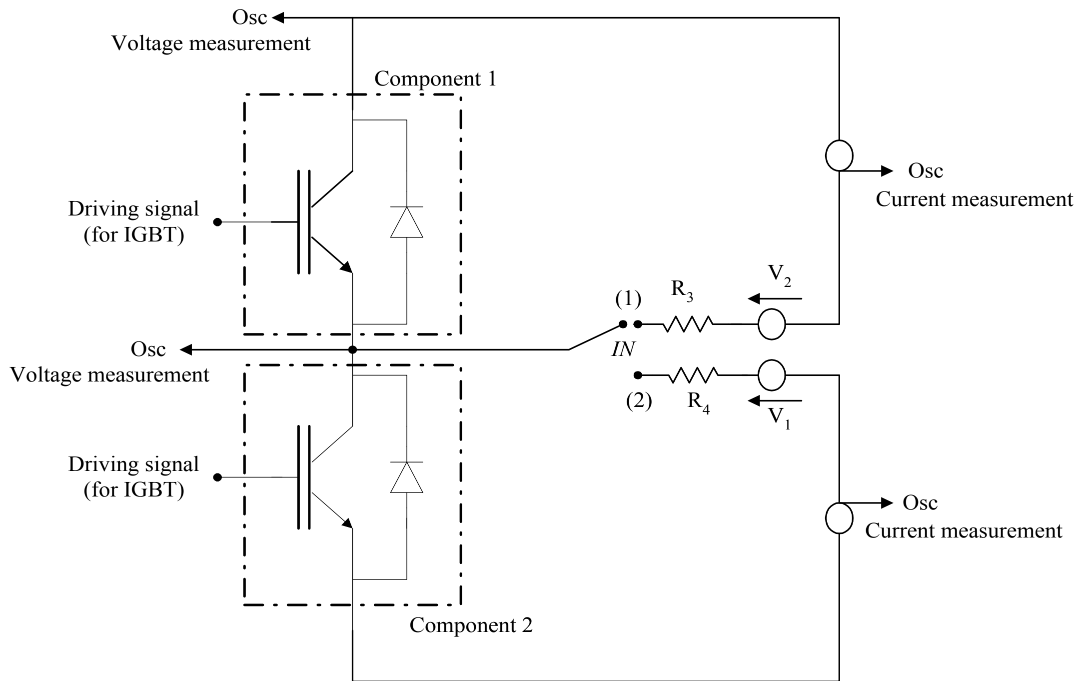

Fig. 19. Experimental circuit proposed to measure the thermal influences between the components on the top and bottom sides of the hybrid structure layout.

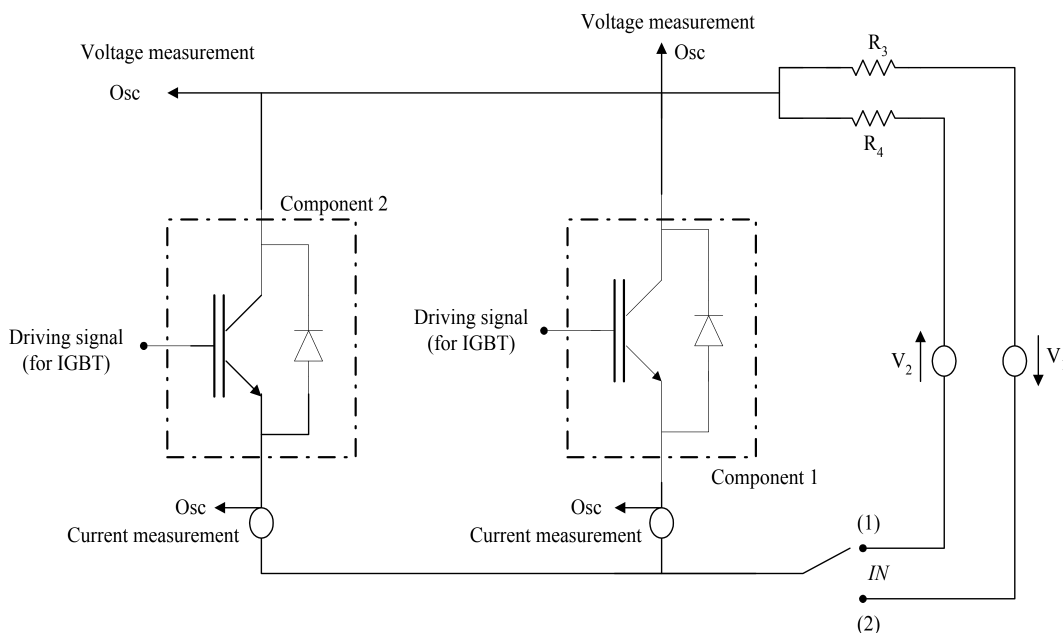

Fig. 20. Experimental circuit proposed to measure the thermal influences between the lateral components of the hybrid structure.

parameter of the other components under this influence is measured. Fig. 19 shows the experimental circuit proposed to measure the thermal influences between the components on the top and bottom sides of the hybrid structure layout. When the switch *IN* is in position (1), the component 1 is traversed by an important current (heating phase) and component 2 is turned off. The case temperature in the steady-state is measured by a thermocouple, the switch *IN* commutes to position (2), and the thermo-sensitive parameter of component 2 is measured according to the circuit (V_1, R_4, component 2) conditions. If component 2 is the IGBT or DIODE, a saturation current parameter measurement and drop voltage measurement are performed, respectively. The thermal influence value between components is deduced with the use of the calibration characteristics shown in Figs. 7 and 14.

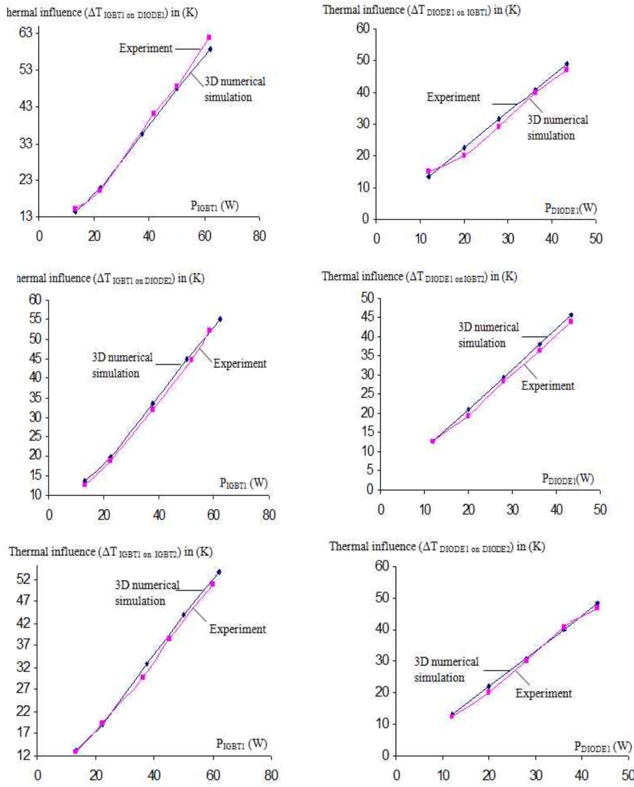

Fig. 21. Evolutions of the thermal influences between the module components against dissipated powers obtained by experimental and 3D numerical simulations.

The experimental circuit proposed in [4], [32] to measure the thermal influences between the lateral components of the hybrid structure is illustrated in Fig. 20. When the switch *IN* is in position (1), component 1 dissipates power (heating phase) and component 2 is turned off. The switch *IN* commutes to position (2) and the thermo-sensitive parameter of component 2 is measured in a steady-state condition.

Fig. 21 shows the thermal influence evolutions between the different components as a function of dissipated power magnitudes. These results are obtained by experiments and 3D numerical simulations. Good agreement between the two types of evolutions is observed. The thermal influence evolution between the different components as a function of the boundary conditions in the case is shown in Fig. 22. Good agreement between the results obtained by 3D numerical simulations and those by the experimental technique is observed. The thermal influence evaluation between two devices in a multi-chip structure is experimentally possible in the steady-state condition.

The proposed technique enables the adjustment of the devices' average junction temperature values obtained by simple use of the transient thermal impedance. Module structure users should use the devices' thermal impedance obtained by experimental measurement in practice. These characteristics depend mainly on the dissipated power magnitude and case boundary conditions. Further

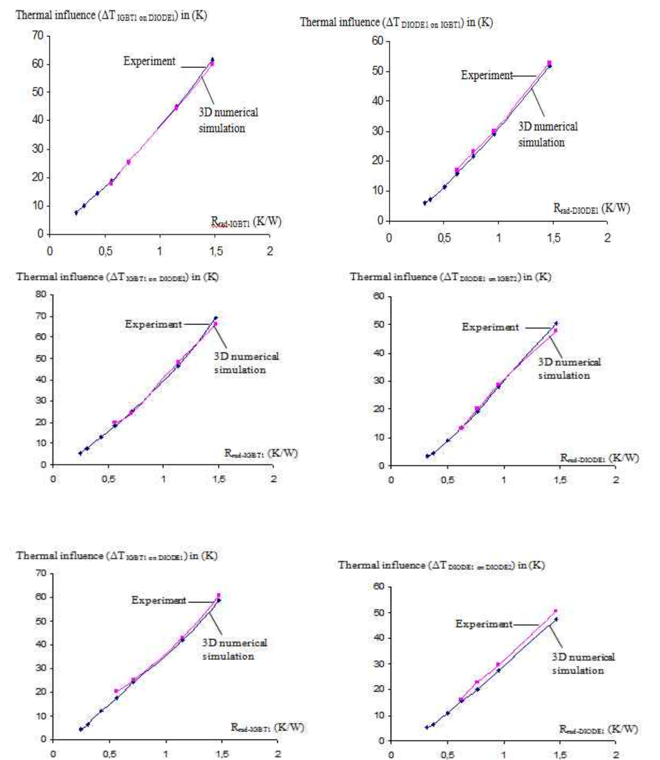

Fig. 22. Evolutions of the thermal influences between the components against the case boundary conditions obtained by experiments and numerical simulations.

experiments are necessary to predict the thermal influence values between the different devices.

B. Validation of the Proposed Technique

We proposed the layering technique to make deductions from the junction temperature of the IGBT and DIODE when the unit is a chopper and then used an inverter to validate the results.

The superposition technique is useful for effective thermal resistance characterization of thermal models on multi-chip modules, hybrid devices, or devices with multiple heat sources [33], [34]. This method requires only one test for each independent heat source present. During each test, junction temperatures for all devices must be measured.

The experimental results shown in Figs. 21 and 22 are used to deduce the global thermal mutual in the different module devices by using the superposition technique. When the studied module operates in a chopper condition, only two devices (an IGBT and diode) dissipate power.

Applying the superposition method, using experimental results (Figs. 21 and 22), and performing 3D numerical simulations of the studied structure provides the data listed in Table I. ΔT_{IGBT1} corresponds to the increase in the IGBT1 temperature value caused by all other devices of the module. This condition, in turn, corresponds to the case of the chopper operation on the effect of the DIODE2 thermal influence on the IGBT1 module. The thermal influence values listed in this

TABLE I
THERMAL INFLUENCE VALUES IN THE IGBT AND DIODE: CHOPPER CONDITION (AMBIENT TEMPERATURE: 306 K; REQU-HEAT SINK = 1.1 K/W)

Dissipated power in the IGBT	Dissipated power in the DIODE	Power ratio P_{IGBT}/P_{DIODE}	ΔT_{IGBT} (K) experimental (result with superposition concept)	ΔT_{IGBT} (K) 3D simulation	ΔT_{DIODE} (K) experimental (result with superposition concept)	ΔT_{DIODE} (K) 3D simulati-on
13,14	12	1	13	11	12	12
22,35	20	1	20	22	19	21
22,35	12	1,8	13	14	19	20
37,7	12	3	13	19	33	37

TABLE II
THERMAL INFLUENCE VALUES IN THE IGBT AND DIODE: INVERTER CONDITION (AMBIENT TEMPERATURE: 306 K; $R_{EQU\text{-}HEAT\ SINK}$ = 1 K/W).

Dissipated power in the IGBT	Dissipated power in the DIODE	Power ratio P_{IGBT}/P_{DIODE}	ΔT_{IGBT} (K) experimental (result with superposition concept)	ΔT_{IGBT} (K) 3D simulation	ΔT_{DIODE} (K) experimental (result with superposition concept)	ΔT_{DIODE} (K) 3D simulat-on
13,14	12	1	40	35	42	39
22,35	20	1	60	65	61	66
22,35	12	1,8	47	48	51	57
37,7	12	3	60	62	81	87

table are provided for different device dissipated power values in the steady-state condition.

Table II shows the obtained thermal influence values when the studied module operates in an inverter condition. All the devices (two IGBTs and two DIODEs) dissipate power in this case. The thermal influence phenomenon is more important in this configuration, and the increase in the devices' temperature caused by the thermal mutual is high. $R_{equ\text{-}heat\text{-}sink}$ is the heat sink resistance that corresponds to the equivalent thermal resistance between the case and ambient air.

Minimal temperature discrepancy between case temperature values under each device is observed in these experimental tests. An averaged value of the case temperature at the interface between the module baseplate and heat sink is considered.

The experimental evaluation of the increase in each device junction temperature is assumed to be the sum of three thermal influences as supposed by the superposition technique. For example, the junction temperature rise in the IGBT1 is provided by the following:

$$\Delta T_{IGBT1} = \Delta T_{DIODE1\ on\ IGBT1} + \Delta T_{IGBT2\ on\ IGBT1} + \Delta T_{DIODE2onIGBT1} \quad (6)$$

The superposition assumption obtains the following:

$$T_{IGB} = T_{IGBT11} + \Delta T_{IGBT1} \quad (7)$$

where T_{IGBT1} is the IGBT1 junction temperature when all module devices operate, and T_{IGBT11} is the IGBT1 junction temperature when it operates alone with the same dissipated baseplate (i.e., the same heat sink, convection coefficient, and power value and the same boundary condition at the module reference temperature T_a).

Minimal temperature discrepancy between case temperature values under each device is observed in these experimental tests. An averaged value of the case temperature at the interface between the module baseplate and heat sink is considered. The two tables show considerable estimated correction of the device junction temperature values obtained by the experimental investigations and superposition assumption. The thermal influences obtained by the experiments and 3D numerical simulations are in good agreement. The errors between the two results increase when the dissipated power in the device under test increases (i.e., at the same dissipated power conditions in the other devices). This discrepancy is due to the measurement error and principle of the superposition technique.

The obtained results show that the estimation of the devices' junction temperature in the multi-chip structure by considering the thermal impedance of each device is insufficient. The increase in device temperature caused by the thermal mutual phenomena is considerable.

The proposed experimental technique allows an significant reduction of the averaged junction temperature errors in the module devices for thermal investigations in the multi-chip structures. The proposed technique can be recommended to develop a simplified thermal model of the multi-chip structures based on a 1D thermal model of each structure device.

IV. CONCLUSIONS

The thermal interaction between devices has been studied in thermal investigations in multi-chip structures.

The thermal behavior of each module component condition on the module baseplate as well as the thermal impedance between the junction and case of each device obtained by 3D numerical simulation are in good agreement with the thermal impedance deduced from the manufacturer data sheet.

Experimental techniques to estimate the transient thermal impedance of the IGBT and diode are presented. Classical thermal analysis based on the thermal impedance provided by the manufacturer data sheet independent of cooling system characteristics and dissipated power magnitude is incorrect.

Components under the dissipated power in the multi-chip structures cause heating of its neighborhood. An experimental technique is proposed to estimate the thermal influences caused by the different chips in the hybrid structure. The proposed technique is based on the measure of the IGBT and DIODE thermo-sensitive parameters in our case.

Experimental characteristics that provide the variation of the device's thermal mutual as a function of the case boundary conditions and dissipated power magnitude are determined.

The device temperature estimation is generally based only on the thermal impedance characteristic of each device. This method introduces high error values on the estimated temperature in multi-chip structures. Thus, a simplified assumption based on the superposition concept is proposed to rectify the estimated averaged hottest temperature value in the different device modules. The corrected temperature variation is in the range of 70% to 100% of the real temperature error made when the classical technique is proposed.

The proposed techniques can be extended to develop a simplified thermal model of different multi-chip structures based on a 1D thermal model such as MOS and bipolar.

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