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Regulated Peak Power Tracking (RPPT) System Using Parallel Converter Topologies

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Abstract

Regulated peak power tracking (RPPT) systems such as the series structure and the series-parallel structures are commonly used in satellite space power systems. However, these structures process the solar array power or the battery power to the load through two cascaded regulators during one orbit cycle, which reduces the energy transfer efficiency. Also the battery charging time is increased due to placement of converter between the battery and the solar array. In this paper a parallel structure has been proposed which can improve the energy transfer efficiency and the battery charging time for satellite space power RPPT systems. An analogue controller is used to control all of the required functions, such as load voltage regulation and solar array stabilization with maximum power point tracking (MPPT). In order to compare the system efficiency and the battery charging efficiency of the proposed structure with those of a series (conventional) structure and a simplified series-parallel structure, simulations are performed and the results are analyzed using a loss analysis model. The proposed structure charges the battery more quickly when compared to the other two structures. Also the efficiency of the proposed structure has been improved under different modes of solar array operation when compared with the other two structures. To verify the system, experiments are carried out under different modes of solar array operation, including PPT charge, battery discharge, and eclipse and trickle charge.

Key Words: Band Width (BW), Battery Power (PBA), Buck Power (PBUCK), Buck Power at Maximum Power Point (PB(MPP)), Buck Power at Trickle Charge Mode (PB(TC)), Bus Regulator (BR), Maximum Power Point (MPP), Regulated Peak PowerTracking (RPPT), Solar Array (SA), Solar Array Regulator (SAR)

I. INTRODUCTION

The series configured SAR systems that are widely used for Low-Earth-Orbit (LEO) satellites, consist of a solar array (SA), a battery, a solar array regulator (SAR) and a battery discharge regulator (BDR), as shown in Fig. 1. However, these systems **process** the SA power to the load through two regulators, the SAR and the BDR, during the sunlight period. As a result, power conversion loss occurs twice [1], [2].

The simplified series-parallel structure shown in Fig. 2 contains an additional switch, which improves the power conversion efficiency. However, the additional diode in the BR increases the losses during eclipses and the PPT discharge mode. In addition, the power transfer to the battery is still through one converter, which increases the charging time [3].

In this paper, a parallel structure consisting of two regulators is proposed. Using a simple control technique, the proposed parallel structure for satellite space power RPPT systems can improve the energy transfer efficiency and the battery charging time when compared to the series and the simplified series-parallel structures.

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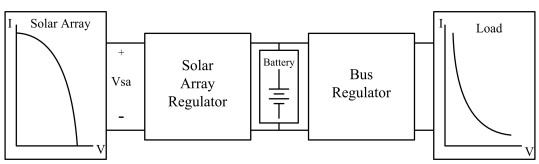


Fig. 1. Series Structure.

II. THE PROPOSED PARALLEL STRUCTURE FOR RPPT SYSTEMS

The parallel structure scheme is shown in Fig. 3. The SAR, which uses a non inverting buck-boost type switching regulator, stabilizes the SA operating point to generate the maximum power of the SA, or regulates the battery charging during the sunlight period. The bus regulator uses a buck type switching regulator which regulates the load voltage. The input of the BR is either the SA or the battery depending on the solar array modes. The battery is connected between the SA and both of the regulators thus improving the charging time since the SA directly charges the battery. The power transfer to the load is shared between two parallel connected converters giving better efficiency when compared to the series structure. The proposed structure can be easily controlled with the implementation of an analogue controller.

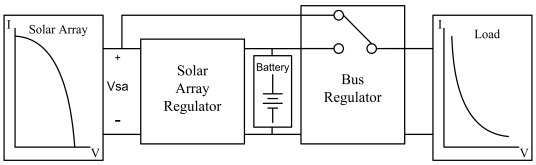


Fig. 2. Simplified Series Parallel Structure.

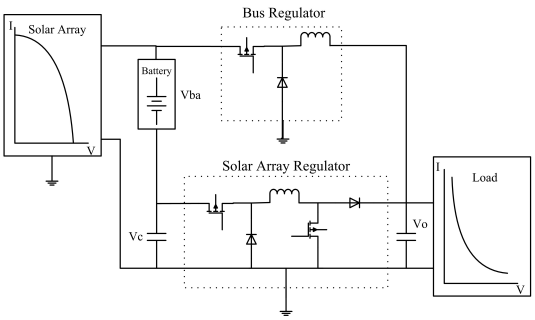


Fig. 3. Proposed Parallel Structure.

III. Operating Modes Of The Parallel Structure

During one orbit cycle, a solar array has four modes of operation.

A. PPT Charge Mode

When the solar array power exceeds the load power demand, the solar array source supplies power to the load and the remaining power is used to charge the battery. In this mode, the SAR determines the SA operating point at the maximum power point (MPP) by controlling the capacitor voltage (VC). Fig. 4 shows the SA and the load power characteristics. The load line shows the load power demand which is shared in parallel between the bus regulator and the solar array regulator. The remaining SA power is used to charge the battery.

Special Cases in PPT Charge Mode

In the PPT charge mode there is a special case where the system enters into the TC mode from the PPT charge mode. Two different cases that exist in the PPT charge mode have been discussed. Case (a) describes the conditions for proper circuit operation in the PPT charge mode.

Case (a)

$$\begin{aligned} &P_{ba} + P_{buck} < P_{SA} \\ &P_{buck} < P_{SApeak} - P_{SA} \\ &P_{buck} < P_L \end{aligned} \tag{A}$$

Derivation shows the case where the system achieves the maximum power point during the PPT charge mode. From Fig. 3 it can be seen that the load power from the SA source is the addition of the buck converter power and the battery power. Similarly, the load power which is shared by the non-inverting buck boost converter flows through the battery from the solar array source. From equation (A) it can be determined that the load power is greater than the individual buck handling load power. Since the load power is shared between the buck power and the non-inverting buck boost power, this condition can also be satisfied by equation (A).

Case (b)

$$\begin{aligned} &P_{bat} + P_{buck} > P_{SApeak} \\ &\Rightarrow P_{SA} = P_{bat} + P_{buck} \\ &\Rightarrow P_{buck} \geq P_L \end{aligned} \tag{B}$$

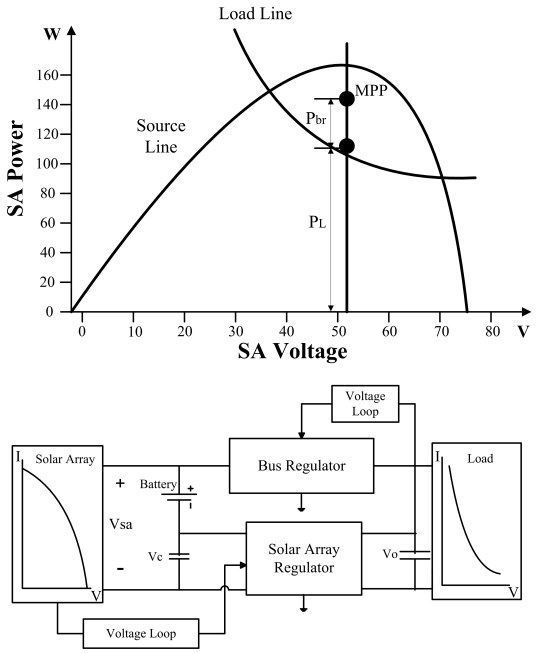


Fig. 4. PPT Charge Mode.

Case (b) shows the conditions when a system enters into the trickle charge mode from the PPT charge mode. This situation occurs when the load power demand is very low. In this case a large amount of power will flow through the battery thus charging the battery more rapidly. When the battery is fully charged, the system operational mode changes to the TC mode. The SA operating point moves toward the voltage source region, which supplies power to the load and trickle charges the battery leakage current.

Case (a) and case (b) are evident in the graphical analysis shown in Fig. 5. During the PPT charge the load power (PL) is set to some preset value. $P_{B(MPP)}$ explains the buck converter load power handling in the PPT mode. As discussed in case (a), when the system achieves MPP, the load power is sum of the buck converter and the non-inverting buck boost converter. Point A in Fig. 5 shows case (a). Similarly, when the load power is less than or equal to the buck power, the system enters into the trickle charge mode as discussed in case (b). $P_{B(TC)}$ shows the buck converter load power handling during the trickle charge mode. Point B shows case (b) in the graphical analysis.

B. Battery Discharge Mode

When the load power demand exceeds the SA maximum power, the SA and the battery supply power to the load simultaneously. During this mode, the SA power is added to the battery power (since the battery supplies insufficient power) to supply the load power. From the system block diagram shown in Fig. 6, it can be seen that current path of the SA power and the battery supply power to the load through the buck converter only. Also, D1 (diode 1), shown the in figure, is activated thus forcing the capacitor voltage (Vc) to clamp at zero potential by completing the current path. No power will flow through the non inverting buck-boost converter which means that the SAR is disabled in this mode. The purpose of

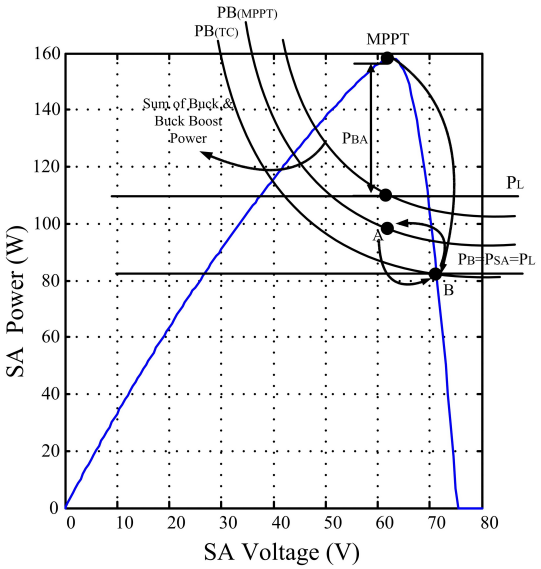


Fig. 5. Graphical analysis of special cases (a) & (b).

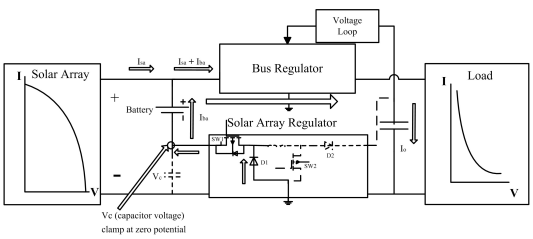


Fig. 6. System block diagram in battery discharge mode. Arrows shows the current path.

the SAR is to operate the SA power at the MPP by controlling the capacitor voltage (Vc). Due to this fact, the MPP is not achieved in the battery discharge mode. The battery clamps the capacitor voltage at zero potential which means that the SA source is now parallel with the battery source and the SA operating point is now determined by the battery only. The battery discharges more current to compensate the load power demand which is a problem of this scheme. However, this situation rarely occurs during one orbital cycle of a LEO space satellite system. Therefore, it can be said that the situation is still affordable in this case. Also only one converter (BR) is operating so power losses occur less.

Fig. 7 shows the SA power and the load power characteristics during the battery discharge mode. When the load line curve exceeds the maximum limit of the solar array curve then the battery will supply the remaining power to the load.

C. Eclipse Mode

When a satellite goes into the shadow of the earth, the solar array source is disabled. During this mode only the battery will supply power to the load which will flow through bus regulator. In this mode, the system structure is almost same as it is for the battery discharge mode with the exception that there is no SA source. Since, the system is working on the battery source, the load power cannot exceed the source power capability. The battery has a limited source and there is no other source to charge the battery. Therefore the load power is normally reduced in this particular mode so that the battery will supply

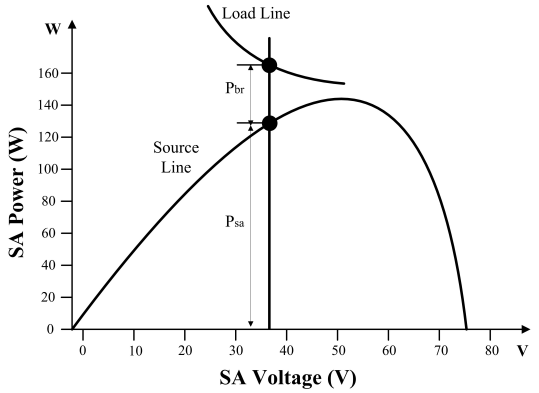


Fig. 7. SA source and load power characteristics in battery discharge mode.

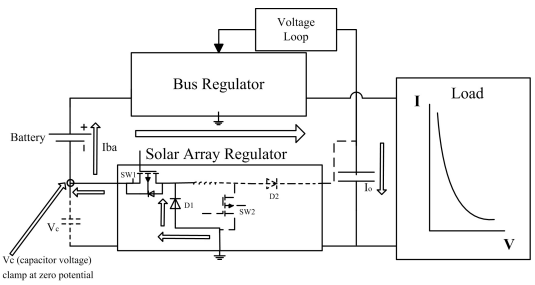


Fig. 8. System block diagram in eclipse mode. Arrows shows the current path.

enough power to the load during the entire period of the eclipse mode. The arrows in fig. 8 show the battery current discharging path. The diode (D1) is turned on and the capacitor voltage is again clamped at zero potential. Since no power is flowing through the non-inverting buck boost converter, the SAR is disabled in this mode. This is an advantage. Since the system is working only on the battery source, if both of the converters are activated simultaneously there will be an increase in the power losses and battery will discharge more rapidly.

Fig. 9 shows the source and the load power characteristics during the eclipse mode. The vertical line shows the battery power source which changes according to the battery power condition. This power also fulfills the load power demand.

D. Trickle Charge Mode

When the battery is fully charged and the solar array power exceeds the load demand, the system switches to the trickle charge (TC) mode. In this mode the SAR does not need to track the SA at the maximum power point since the battery is fully charged. A heavy load will sink a large amount of solar array current and bring the SA operating power near to the peak power point, whereas a low load will bring the solar array voltage towards the open circuit voltage. In this mode, the SA power is slightly higher than the load power which supplies power to the load and also trickle charges the battery voltage. As a result, a small amount of current is flowing through the non-inverting buck boost converter to compensate the battery leakage current and most of the load power sharing is handled by the buck converter (BR). Fig. 10 shows the structure of the scheme in the trickle charge mode.

The system operation has been analyzed graphically in the trickle charge mode, as shown in Fig. 11. During the TC mode, most of the load power is shared by the BR and a very small

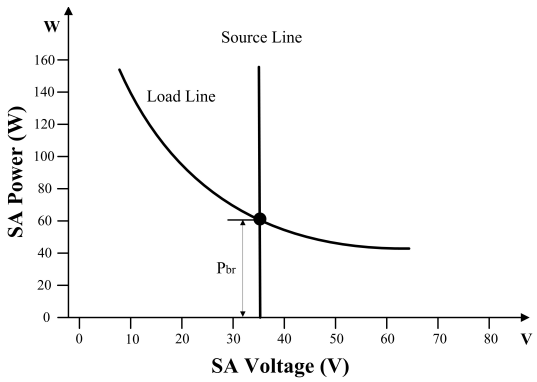


Fig. 9. Source and load power characteristics.

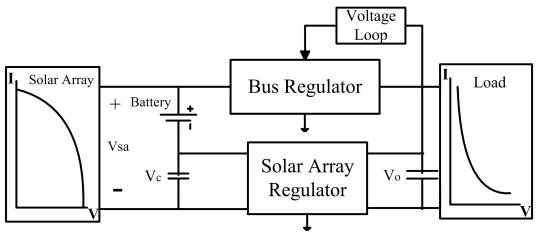


Fig. 10. System block diagram in trickle charge mode.

amount of power flows through the SAR which is used to compensate for the battery leakage current. In other words the load line is the sum of the buck power and the non-inverting buck boost power.

E. Transition from Eclipse Mode to PPT Charge Mode

When the satellite leaves the eclipse mode and enters into PPT charge mode it is ensured that for achieving the SA maximum power point, the starting point of the solar array power must be greater than the load power i.e. PL < PSA. Otherwise, a battery lock-up problem occurs. To avoid this problem it is ensured that before the mode transition, the initial solar array power should be higher than the load power. During this transition mode, the initial operating point of the solar array power is determined by the battery voltage. In the eclipse mode, the capacitor voltage (Vc) is clamped at the zero potential by the battery. Therefore if the initial SA operating point set by the battery is not higher than the load power, the solar array power source sees a higher load power demand. In this case, the solar array starts at the same operating power which is determined by the battery and the remaining load power will be supplied by the battery. This situation can be avoided by reducing the load power during the eclipse mode. Since the system works only on the battery source, when the system enters into the PPT mode it can be assumed that the initial SA operating power is higher than the load power. Once the SAR starts tracking the MPP properly the load power can be increased according to the load requirement. From the analysis it can also be said that there is a minimum load condition in the eclipse mode. Fig. 12 shows a graphical analysis of the eclipse mode to the PPT charge mode transition case. Figure point (a) represents the condition when solar array power is lower than the load power. Similarly, point (b) shows the condition when the initial SA operating power is higher than the load power.

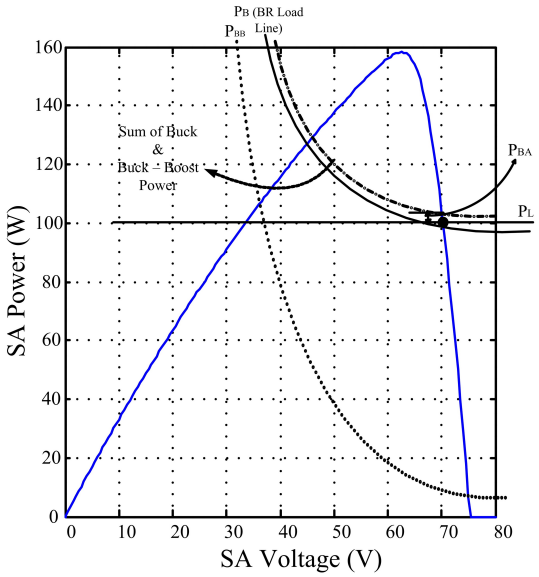


Fig. 11. Graphical analysis of the system in trickle charge mode.

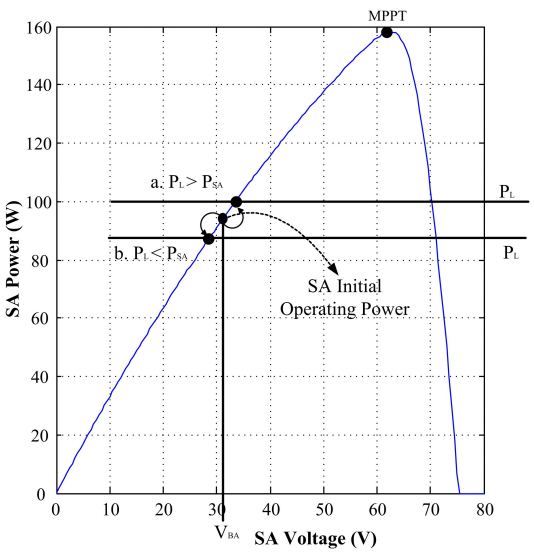


Fig. 12. Graphical analysis of modes transition case.

IV. Control Scheme Of Proposed Parallel Structure

A. Bus Regulator (BR) Controller Design

The closed loop transfer function for the bus regulator has been designed to make sure that the system remains stable under any transients or step load changes. The open loop control to the output transfer function of the buck converter is given by the expression:

$$G_{vd} = \frac{\hat{V_o}}{\hat{d}} = V_{sa} \cdot \frac{1 + sR_cC}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o}} \tag{1}$$

where

$$\omega_o = \frac{1}{\sqrt{LC}}, Q = \frac{1}{\omega_o(\frac{L}{R_o} + R_cC)}$$

G_{vd} represents the open loop transfer function of the buck converter and R_c represents the parasitic resistance of the

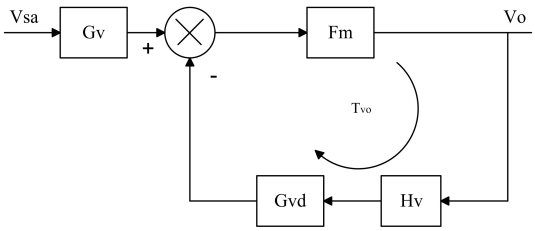


Fig. 13. Small signal model.

capacitor. The second order function shown in the denominator of eq. (1) contains positive parameters, which implies that the system open-loop poles can be real or complex and they are always located in the left half plane (LHP). The poles of the system residing in LHP ensure the stability of the system.

The open loop transfer function is closed by using a poles zeros compensator for the bus regulator loop.

$$H_{v(s)} = \frac{\omega_I(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{s(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}. \quad (2)$$

A 3-pole, 2-zero compensator (Hv(s)) can be employed to optimize the dynamic performance and stability of the converter. An integrator (wI) is placed at the origin to provide zero steady-state error. The pole wp1 of the compensator is used to cancel the first zero of the Gvd and wp2 is used to provide additional attenuation of the switching ripples. Both of the zeros wz1 and wz2 are placed near the resonant frequency of the Gvd to achieve a maximum gain and system stability [1], [2]. Since the Gvd has a positive dc gain, an inverting amplifier configuration is required to obtain an overall negative feedback. Eq. (2) represents the compensator function Hv(s) with pole and zero variables.

Fig. 13 shows a small signal block diagram of the system with the voltage loop closed.

$$T_{vo} = F_m H_v G_{vd} \quad (3)$$

Eq. (3) shows the overall closed loop (T_{vo}) gain function. H_v represents a feedback compensator with a proper poles zeros location for ensuring the stability of the system. F_m is the sensing gain and G_{vd} is the open loop transfer function.

B. Solar Array Regulator (SAR) Controller Design

Before closing the SAR, there is an important factor which can create stability and regulation problems. For proper circuit operation, the closed loop must cross over the frequency of the BR higher than the SAR under all of the SA operation modes. In this scheme, a buck topology (BR) regulates the output voltage using the SA voltage as an input source. Then by using a non-inverting buck boost converter (SAR), the capacitor voltage (Vc) is regulated at the MPPT, considering that the output voltage is stabilized and constant. From this point of view, it is said that the band width of the BR loop is critical and must be higher that the SAR band width. The

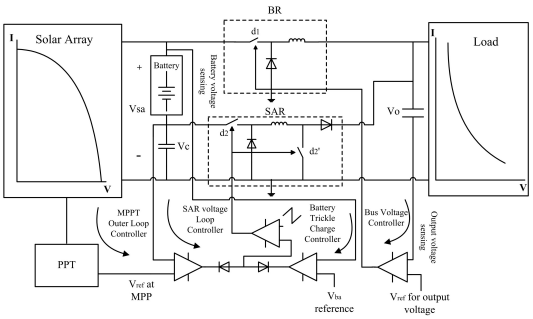


Fig. 14. Control Strategy of the Proposed Structure.

open loop control to the output transfer function of the non-inverting buck boost converter is given as:

$$G_{vd} = \frac{\hat{V}_c}{\hat{d}} = -\frac{V_o}{D^2}\frac{1+\frac{sI_L L}{V_o}}{1-s\frac{L}{D^2 r_s}+s^2\frac{LC}{D^2}} \quad (4)$$

Where

$r_s < 0$ (Incremental resistance of SA output)

The second order function shown in the denominator of eq. (4) contains negative parameters. However, r_s (the incremental resistance of the SA output) has a negative value which implies that the system open-loop poles can be real or complex and are always located in the LHP thus ensuring the stability of the system. For the closed loop operation of the SAR, the same approach is used as the BR controller design. In this case, since G_{vd} has a negative dc gain, a positive feedback gain is required to obtain an overall negative feedback. Similarly the overall SAR closed loop gain (T_{vc}) can be represented as:

$$T_{vc} = -F_m H_v G_{vd} \quad (5)$$

Equation (5) also shows that the control of duty ratio is implemented to regulate the Vc at the MPP which is set by the outer PPT loop. If the bandwidth (BW) of the buck converter (BR) is not faster than the BW of the SAR, oscillations occur in the system.

Peak power tracking is accomplished by closing two loops: the inner SAR voltage loop and the outer PPT loop. The inner voltage loop is used to regulate the solar array output voltage at V_{ref} through V_c. Several methods have been used for tracking the MPPT point like the perturbation and observation (P&O) method, the incremental method and others methods where fuzzy logic and neural networks are applied.

In this scheme, using a digital controller, the Perturbation & Observation (P&O) method [4], [5] is implemented for the outer PPT loop. The general equation used in the P&O method is:

$$V_{ref}(k+1) = V_{ref}(k) + M\frac{\Delta P}{\Delta V} \quad (6)$$

Where M is a constant parameter used to adjust the step size.

For proper circuit operation, the closed loop crosses over the frequency of the outer PPT loop much slower than the inner SAR voltage loop [1], [2].

When peak power tracking is not needed, the MPPT loop is disabled, and only a single loop is required for the trickle

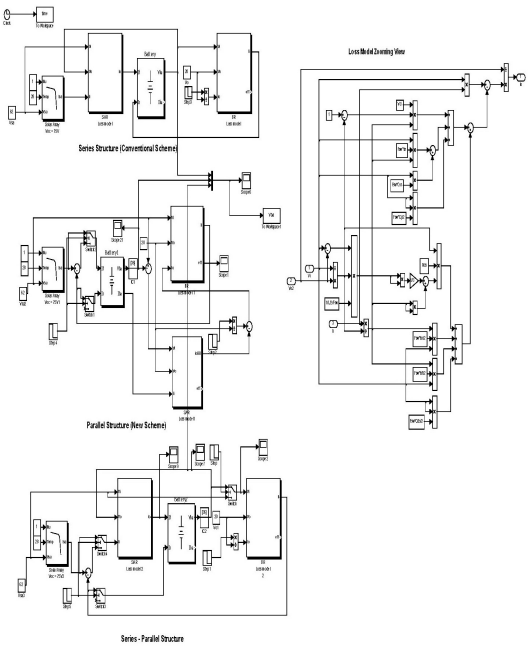


Fig. 15. Matlab Simulink loss analysis model for battery and efficiency measurement.

charge mode. An analog controller is implemented to control the battery voltage. For this purpose, the battery voltage is sensed, the battery voltage is then compared to a fixed reference voltage, and a control action on the duty cycle of the SAR converter is generated, accordingly. Fig. 14 shows a block diagram of the control strategy for the proposed structure.

V. Simulation Results

The main objective of this scheme focuses on the improvement of the battery charging time and the energy transfer efficiency of the system. So, for comparison purposes a loss analysis model has been developed for the series, the simplified series-parallel and the proposed structures. A loss analysis model has been developed in MATLAB Simulink.

A. Loss Analysis Model

Converter topologies contain components like diodes and switches which generates losses in the system. The three main losses have been considered and analyzed for the development of a loss model. These losses include switching losses, diode losses and junction capacitance losses. Descriptions of these losses with their formulas have been presented in table I.

B. Battery Voltage Measurement

To verify the improvement in the battery charging time of the proposed structure, three structures (the series, the simplified series-parallel and the proposed parallel structures) are simulated under the same loading conditions and the same SA array illumination and temperature profile.

Battery charging and discharging measurements have been simulated using the loss analysis model. Two cases have considered for the simulation. In the first case, the battery voltage has been simulated from the PPT charge mode to the

TABLE I
Loss Parameters Used in Loss Analysis Model

Converter Topologies	**Loses**	**Formula**
Buck converter	Turn on loss of the MOSFET switch	$P_{swon} = \frac{V_I I_L f_s t_{sr}}{2}$
	Turn off loss of the MOSFET switch	$P_{swoff} = \frac{V_I I_L f_s t_{sf}}{2}$
	MOSFET switch conduction loss	$P_{swcon} = R_{ds} I_{rms}^2$
	Diode reverse recovery loss	$P_{drr} = V_I I_L f_s t_{sr} + V_I f_s Q_{rr}$
	MOSFET switch junction capacitance loss	$P_{swcap} = \frac{C_{ds} V_I^2 f_s}{2}$
	Diode on loss	$P_{dcon} = V_d I_L D$
	Diode capacitance loss	$P_{dcap} = \frac{C_j V_I^2 f_s}{2}$
Non – Inverting Buck Boost Converter (SAR)	Turn off loss of the MOSFET switch	$P_{swon} = \frac{V_I I_L f_s t_{sr} + V_o I_L f_s t_{sr}}{2}$
	MOSFET switch conduction loss	$P_{swcon} = 2R_{ds} I_{rms}^2$
	MOSFET switch junction capacitance loss	$P_{swcap} = \frac{C_{ds} V_I^2 f_s + C_{ds} V_o^2 f_s}{2}$
	Diode reverse recovery loss	$P_{drr} = V_I I_L f_s t_{sr} + V_I f_s Q_{rr} + V_o I_L f_s t_{sr} + V_o f_s Q_{rr}$
	Diode on loss	$P_{dcon} = 2V_d I_L D$
	Diode capacitance loss	$P_{dcap} = \frac{C_j V_I^2 f_s + C_j V_o^2 f_s}{2}$

P_{swon} Switch on power loss

V_I Input voltage

V_o Output voltage

I_L Inductor current

f_s Switching frequency

T_{sr} Turn-on rise time

R_{ds} Drain-source on-state resistance

I_{rms} Root mean square current

Q_{rr} Reverse recovery charge

T_{sr}Turn-off fall time

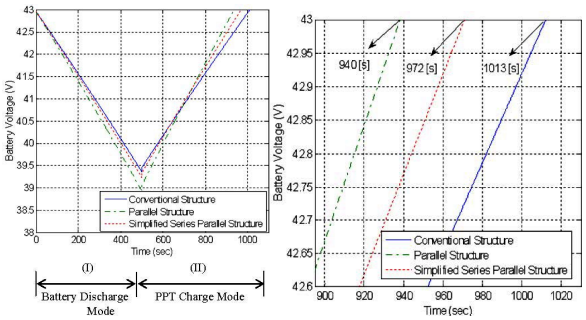
C_{ds} Drain to source capacitance

C_j Junction capacitance

P_{drr} Diode reverse recovery power loss

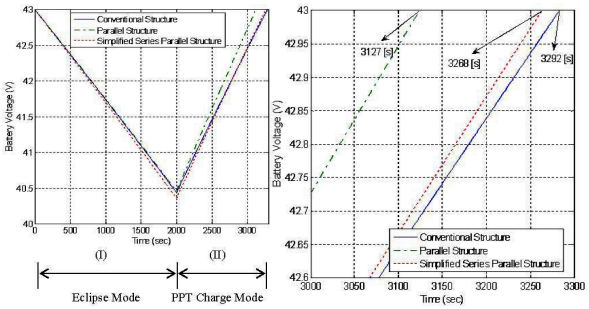
P_{swcap} Switch capacitance power loss

P_{dcon} Diode conduction power loss



(a) (b)

Fig. 16. (a) Shows the simulation of battery performance during PPT charge and battery discharge mode. (b) Shows the close view of battery charging results in PPT charge mode.



(a) (b)

Fig. 17. (a) Shows the simulation of Battery Performance during eclipse and PPT charge mode. (b) Shows the close view of battery charging results in PPT charge mode.

battery discharge mode. The battery specification used for the simulation and the hardware results have presented in table II. Initially the battery voltage is set to its maximum value with a load power of 100W. At 500 seconds, a step load of 100W to 200W has shifted the system from the PPT charge mode to the battery discharge mode. Fig. 16 (a) and (b) show the simulation result that contains the battery performance of the systems during these solar array mode transitions. The simulation results show that during the battery discharge mode, the battery of the parallel structure has a higher voltage drop when compared to the series structure and simplified series-parallel structure. As discussed in section III, the solar array regulator is disabled during this mode and hence the MPP is not achieved. For this reason the battery discharges more current and this current is added to the solar array current to supply the insufficient power to the load. During the battery discharge mode, the series structure drops a lesser amount of battery voltage when compared to the simplified series-parallel and parallel structures. In fact the behavior of the series and simplified series-parallel structures is same in the battery discharge mode except that the additional switch used in the simplified series-parallel structure is disabled in this mode. Also, an additional diode (used in the BR of the simplified series-parallel) is turned on. Due to turn on loss of the additional diode, the battery of the series structure has a slower discharge rate than the simplified series-parallel structure. However, when the system enters into the PPT charge mode, the battery performance of the proposed structure is better than other two structures i.e. the series and simplified series-parallel structures. From the fig. 16 (a) and (b) it can seen that the proposed parallel structure charges the battery voltage to its maximum value (43V) at 940 seconds, whereas the series structure and the simplified series-parallel structure achieve the maximum battery voltage in 1013 seconds and 972 seconds, respectively.

From these results it is therefore concluded that the system mode transition from the battery discharge mode to the PPT charge mode, the battery charging time of the parallel structure, has improved by 73 seconds and 32 seconds when compared to series (conventional) structure and the simplified series-parallel structure, respectively.

A second case was considered for the battery performance in which the system is simulated under the mode transition from

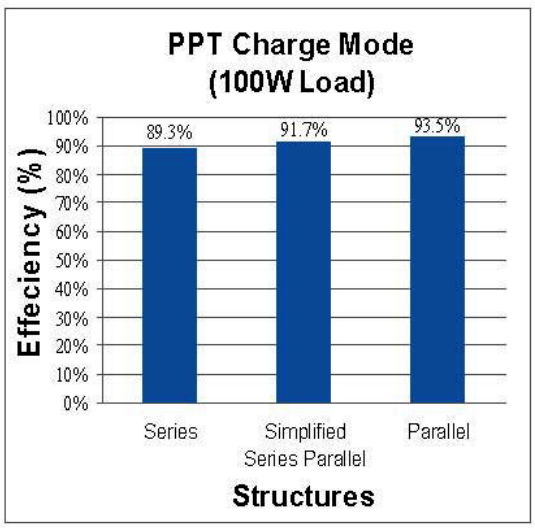


Fig. 18. Efficiency comparisons of different structures in PPT charge mode.

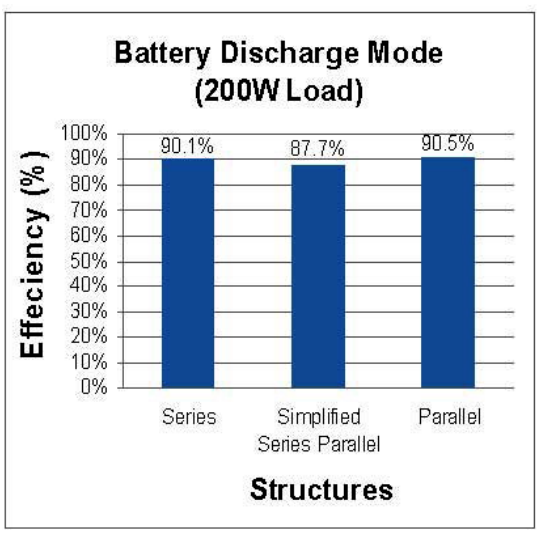


Fig. 19. Efficiency comparisons of different structures in battery discharge mode.

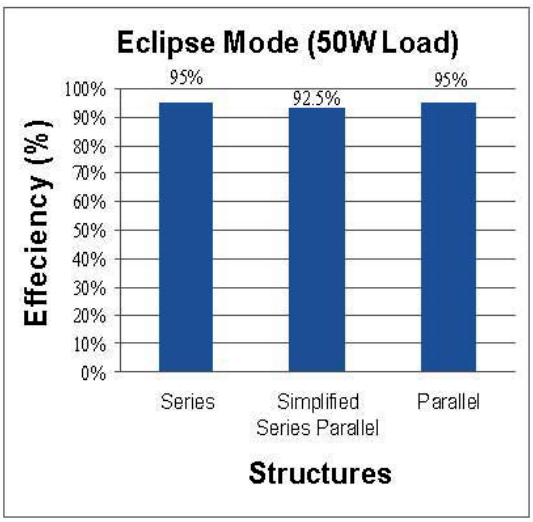


Fig. 20. Efficiency comparison of different structures in eclipse mode.

the eclipse mode to the PPT charge mode. In the eclipse mode there is no solar array source, as the only source of power for the system is the battery. An assumption has been made that before the mode transition from the PPT charge mode to the eclipse mode, the battery has already been fully charged. During the eclipse mode the load power has been set to a value of 50W and the battery supplies this power to the load. For battery charging measurement, a mode transition from the eclipse mode to the PPT charge mode has been simulated and the result are shown in fig 17. In the figure, it can be seen that, during the simulation, at 2000 seconds the system enters into the PPT charge mode from the eclipse mode. At the same time a step load of 50W to 80W has been simulated and analyzed. Simulation result show that the proposed structure charges the battery voltage to its maximum value (43V) at 3127 seconds, whereas the series structure and the simplified series-parallel structure achieve their maximum battery voltage at 3292 seconds and 3268 seconds, respectively. Therefore, from these results it can be concluded that during the mode transition, the battery charging time for the proposed parallel structure is improved by 165 seconds and 141 seconds over the series (conventional) structure and the simplified series-parallel structure, respectively.

In this case it is observed that battery discharges a lesser amount of power when compared to the previous case. This is due to the difference in the loading profile. In this case, a 50W load power is set in the eclipse mode and a step load of 80W is applied in the PPT charge mode. In the first case, a 200W load power is set in the battery discharge mode which in return discharges more battery current. During the eclipse mode, the battery of the simplified series-parallel structure discharges more when compared to the series and proposed parallel structures. However, the simplified series-parallel structure uses one extra diode in the BR for the prevention of reverse current, which increases losses and discharges more battery current.

Compared to the other structures, in this scheme the battery is placed between the converters and the solar array source, which results in an improvement of the battery charging time.

TABLE II
SUMMARY OFFPARAMETERS USED IN THE PROPOSED RPPT SYSTEM

Solar Array	(Two Panel connected in series)
Model	Symphony Energy ES-S 173×2
Operating Voltage	0 ˜ 80V
Maximum Power Point Voltage	61 ˜ 63V
Maximum Power Point	180 W
Output Voltage	20V
Maximum Load Power	200W
Illumination System	(HID Lamp)
Lamp	Phillips 150 W HID × 30
Ballast	Interpower HID ballest × 30
Battery	GS 36V of Japan
Battery Voltage Range	33V ˜ 43V
MOSFET Switch	IRF640
Inductor	100uH (PQ3535)
Capacitor	100uF
PWM Controller	UC3823
Switching Frequency	100KHz

C. Efficiency Measurement

The energy transfer efficiency of the proposed structure has been measured using the loss analysis model discussed in section V. For this purpose all three structures are simulated under the different modes of SA operation and the loading conditions using equation (7) and (8).

$$\eta = \frac{P_o}{P_{in}} \tag{7}$$

Where

$$P_{in} = P_{out} + P_{losses}$$

$$P_L = P_{SA} + P_{BA} \tag{8}$$

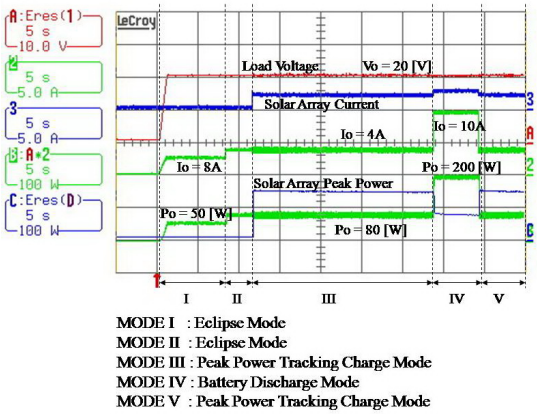
Figure 17, 18, and 19 show graphical results of the efficiency of the RPPT system under the different modes of SA operation. During the PPT charge mode, the proposed structure has a higher efficiency when compared to the series and the simplified series-parallel structures. Similarly, during the battery discharge mode and the eclipse mode, the efficiency of the proposed structure and the series structure have the same value but are better then the simplified series parallel structure. This is due to the additional diode used in the BR of the simplified series-parallel structure which effects the system efficiency.

VI. EXPERIMENTAL RESULT

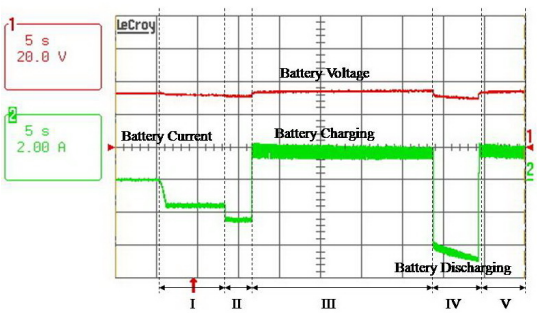
For experimental verification, a prototype RPPT system has been built and tested. It contains an in-house made solar array which consists of two solar array panels in series, whose maximum power is 180W in the emulated illumination system and a 36V battery made by GS of Japan.

The lighting system is implemented using 30 high-intensity-discharge lamps and ballasts for emulating sunlight. The photovoltaic power system consists of buck and non-inverting buck boost converters in parallel. The detailed system parameters used in the experiment are summarized in Table II. For the hardware results, the RPPT system is tested under different modes of solar array operation using the same analysis mentioned in section 3.

Fig. 21 (a) shows the hardware experimental results during one orbit cycle. It has confirmed that the proposed structure, with its control scheme, can achieve its function as a regulated

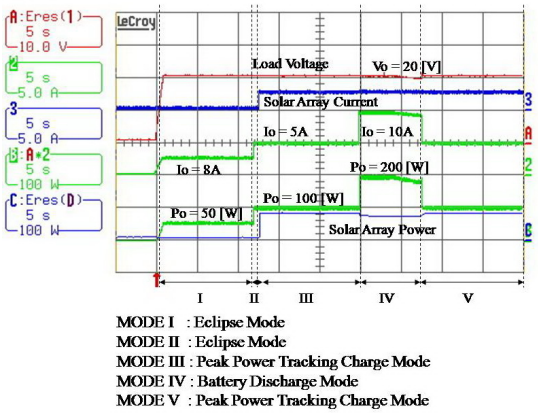


(a)

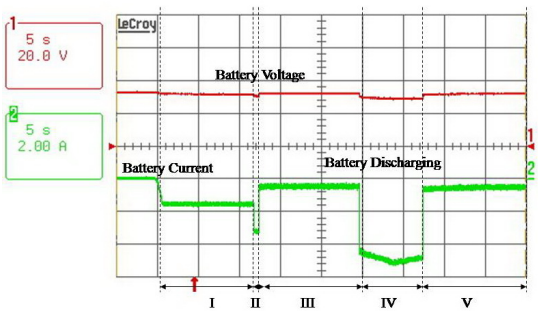


(b)

Fig. 21. (a) Experimental results during solar array one orbital cycle. (b) Battery voltage and current characteristics under SA orbital modes.



(a)



(b)

Fig. 22. (a) Experimental results during SA orbital cycle considering eclipse to PPT charge mode transition case. (b) Battery voltage and current characteristics under SA orbital modes.

peakpower tracking system in the presence of environmental and load variations. Figure 21 (b) shows the battery performance during solar modes transitions.

Another result is shown in Fig. 22 (a) and (b). The main purpose of these results is to verify the special cases discussed in section III. For the purpose of verification, a 100W load has been set before the mode transition from the eclipse mode to the PPT charge mode. From the results it can be seen that the output voltage (20V) is properly regulated. However, the SAR can not achieve the MPP during the PPT charge mode. The result demonstrate that the necessary conditions mentioned in section III must be fulfill for proper SAR operation in the PPT charge mode.

Fig. 22 (b) shows the battery current characteristics during one orbital cycle for the case mentioned above.

VII. Conclusion

In this paper, a parallel structure and a control method for a regulated peak power tracking system are proposed to improve the battery charging time and efficiency of the system. Simulation results show that under the different modes of solar array operation the battery charging time of the proposed structure is faster than the conventional structure and the simplified series-parallel structure. Simulation results also shown that the proposed structure gives better efficiency when compared to the series structure and the simplified series-parallel structure under the different modes of solar array operation. In the PPT charge mode the proposed structure improved the efficiency by 2% and 4% when compared to the simplified series-parallel structure and the series structure, respectively. Similarly, in the eclipse mode and battery discharge mode, the efficiency of the proposed structure is improved by 2.5% and 3% when compared to the simplified series-parallel structure.

In fact, the proposed structure, the simplified series-parallel structure and the series structure are simulated under the same load, illumination and temperature profile. In this way the SA generates identical electrical power and the load demands the same electrical power. Therefore, the system which saves more energy in the battery is the most efficient. The analysis is also verified by efficiency measurement simulation results.

Experimental results for the proposed structure are carried out under the different modes of SA operation which satisfies the system stability under all of the modes of solar array operation and load transitions. Also, the necessary conditions for achieving the solar array MPP before the mode transition from the eclipse mode to the PPT charge mode are verified by experimental results.

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