JPE 11-6-13

Novel Active Voltage Quality Regulator with Adaptive DC-Link Voltage Control

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Abstract

In this paper, a novel Active Voltage Quality Regulator (AVQR) topology with a thyristor rectifier and an adaptive dc-link voltage control strategy are proposed. The proposed AVQR can efficiently mitigate the long duration variations (e.g. undervoltages/overvoltages), voltage imbalances and voltage harmonics. Compared with conventional AVQRs, it can regulate the load voltage very well with a much lower dc-link voltage. This is accomplished by replacing the diode rectifier with a thyristor rectifier. Moreover, its dc-link voltage can vary with the deviations of the supply voltage through the proposed adaptive dc-link voltage control strategy. All of these contribute to its significantly higher efficiency for online operating, which is very important and attractive for many applications. The proposed topology and control strategy are theoretically analyzed in detail. Simulation results are also provided in the paper. Finally, the feasibility and effectiveness of the proposed method are verified by means of experimental results from a 2kVA prototype. Both of the simulation and experimental results show that the proposed AVQR can achieve a much higher efficiency and similar regulation performance when compared with the conventional ones.

Key Words: Adaptive dc-link voltage, Active Voltage Quality Regulator (AVQR), Efficiency, Power quality, Transformerless

I. INTRODUCTION

With the development of modern science and technology, various sophisticated types of equipment and sensitive loads that require a higher power quality are widely used. Meanwhile, the factors that degrade the power quality of the grid, such as the comprehensive application of nonlinear loads, are increasing rapidly. The contradiction between the above two aspects is becoming more and more serious [1].

Voltage quality problems, especially the voltage quality problems of the Point of Common Coupling (PCC), are considered to be the most significant and critical parts of power quality problems [2]. IEEE Std 1159-2009 classifies voltage quality problems into several groups, such as transients, short duration root-mean-square (rms) variations, long duration rms variations, voltage imbalances, waveform distortions, etc [3]. It should be noted that the most typical voltage problems of short duration rms variations are voltage sags (sag to 0.1-0.9pu and lasting for 0.5 cycles to 1min) and swells (swell to 1.1-1.8pu and lasting for 0.5 cycles to 1min). Meanwhile the long duration variations usually last for more than 1min and have smaller magnitude fluctuations (0.8-0.9pu for undervoltages and 1.1-1.2pu for overvoltages). It is obvious that, the short duration variations and the long duration variations different from each other greatly in terms of magnitude and duration.

There are several approaches to mitigating voltage quality problems. Conventional Ac Voltage Regulators (AVR) with electronic tap-changed transformers, which have been applied to many fields, can deal with long duration voltage variations, but generally they have only a limited discrete voltage regulation capability and no ability to suppress voltage harmonics. Dynamic Voltage Restorers (DVR) can compensation short duration rms variations such as sags/swells efficiently with a fast dynamic response [4], [5]. Usually, DVRs operate in off-line mode with a short running time to compensate for deep voltage sags/swells. Therefore, they can achieve both a high efficiency and a low cost. In order to increase the function and the utilization of the devices, DVRs have also been proposed to deal with undervoltages/overvoltages and voltage harmonics [6]. In this way, DVRs can be regarded as an Improved series connected Ac Voltage Regulator (IAVR) or as a Multifunction Ac Voltage Regulator (MAVR), which can deal with both short duration rms variations and long duration rms variations as well as voltage harmonics [7], [8].

Nevertheless, as mentioned above, the short duration rms variations (sags/swells) and the long duration rms variations (undervoltages/overvoltages) differ from each other greatly in terms of magnitude and duration. It is uneconomic and unreasonable to employ only one voltage conditioning device to solve both of them. To mitigate these voltage quality problems, a high dc-link voltage of the inverter is required for the former, while a much lower dc-link voltage is sufficient for the later. Moreover, the online operation of devices is

Manuscript received May 29, 2010; revised Aug. 1, 2011
Recommended for publication by Associate Editor Nam-Sup Choi.
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required for the later but unnecessary for the former, which is determined by considering the different characteristics of the magnitude and the duration. Hence, it may be more cost-effective and reasonable to deal with them separately.

Active voltage quality regulators (AVQR) are good candidates for compensating slowly varying and steady-state voltage quality problems in low power distribution systems, such as long duration variations (undervoltages/overvoltages), voltage imbalances, voltage harmonics, etc. They can regulate the load voltage continuously by injecting an appropriate voltage in series with the supply voltage. AVQRs are similar to the conventional voltage regulators, but are superior to the later in terms of functions and performance.

However, there are some deficiencies in the existing AVQRs which need to be improved. Firstly, the existing AVQRs often contain transformers, which provide electrical isolation or coupling. In addition to the transformer's bulkiness and costliness, it also contributes to the regulator's losses and causes other problems, such as saturation and nonlinear characteristics [9], [10]. Secondly, the dc-link voltages of the existing AVQRs, either uncontrolled or controlled to a constant value [8], [11], are generally designed according to the worst possible condition of the supply voltage (i.e. the maximum missing load voltage) so that they are always maintained at a high level. Since voltage quality events occur randomly, the probability of encountering the worst supply condition is relatively small and, generally, the duration of this condition is short. Therefore, such high dc-link voltages are obviously unnecessary for online operation when the missing load voltage is low, especially, when the supply voltage is almost normal (i.e. the missing load voltage is approaching zero). In addition to the decrease in system efficiency due to the unreasonable switching losses, the dead-time effect and the EMI become more serious as a consequence of an inappropriate dc-link voltage. Research has not fully taken the advantage of this topology since the dc-link voltages of the AVQRs cannot adaptively vary with the missing load voltage. This is one of the main reasons why the traditional AVQRs cannot achieve satisfying efficiency in online mode.

Based on the schemes proposed in [12], [13], a novel transformerless AVQR topology and its adaptive dc-link voltage control strategy are proposed in this paper. Compared with conventional AVQRs, the proposed topology is improved only by replacing the diode rectifier with a thyristor rectifier. This small change makes the proposed adaptive dc-link voltage control possible, which contributes to higher efficiency. The principle and realization of the proposed adaptive dc-link voltage control strategy are analyzed in detail. Then the losses and efficiencies with the diode rectifier and the thyristor rectifier are compared, respectively. Finally, the validation and the effectiveness of both the proposed topology and the control strategy are verified by laboratory experimental tests on a 2kVA prototype. The experimental results show that the proposed topology and control strategy can enhance the efficiency remarkably when compared with the conventional ones.

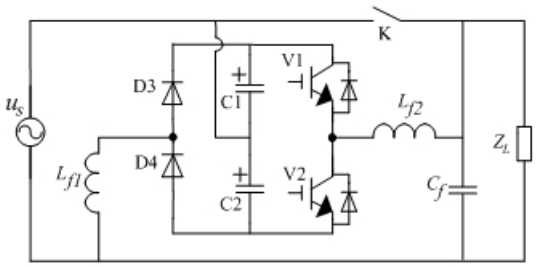


Fig. 1. Topology of DySC [12].

II. Proposed Topology

In 2001, D. M. Divan et al. proposed a transformerless Dynamic Sag Corrector (DySC) [12]. The basic topology of this DySC is shown in Fig. 1. The DySC was initially used to deal with voltage sags down to 40%-50%. In 2004, it was utilized to effectively reduce voltage sags/swells, voltage undervoltages/overvoltages as well as voltage harmonics in sensitive loads in cite7,8. Therefore, this topology can be regarded as an Improved Ac Voltage Regulator (IAVR), which can continuously regulate the load voltage by injecting a voltage in series with the supply voltage. With the increase in functions, the total efficiency of the regulator inevitably decreases because of the high dc-link voltage, which is related to the switching losses and the losses of the dc-link capacitor.

In [11], the diodes D3 and D4, as shown in Fig. 1, were replaced by two IGBTs. Nevertheless, there was a similar problem in the circuit structure, namely that the dc-link voltage was maintained at a high and constant value and could not vary with deviations of the supply voltage. Hence, the method proposed in [11] also did not fully take advantage of the topology, since the series circuit configuration is only used to compensate the missing parts between the supply voltage and the desired output voltage.

From the analysis above, the main limitation of the DySC, used as an IAVR or as a MAVR, is that the dc-link voltage cannot adapt to supply voltage deviations (i.e. the missing load voltage). To avoid this drawback in the existing topology, a novel single-phase transformerless AVQR topology with an adaptive dc-link voltage control is proposed in this paper [14]. As shown in Fig. 2, the diode rectifier is replaced with a thyristor rectifier so that the dc-link voltage can be controlled to vary with supply voltage deviations adaptively. It provides several benefits including a larger duty ratio of the inverter, a lower dead-time effect, fewer EMI problems, good compensation performance and a higher system efficiency. Therefore, the proposed topology can deal with the long duration variations, voltage imbalances, and voltage harmonics with an extremely high efficiency, while short duration voltage variations, such as voltage sags/swells, can be efficiently solved by DVRs [4], [5]. As for three-phase applications, the three single-phase configurations can be combined as a three-phase four-wire system to compensate the three-phase system and to increase the capacity of the regulator. Moreover, the proposed AVQR can include all of the functions of traditional AVQRs by controlling the thyristor rectifier to maintain the same high dc-link voltage as the conventional ones.

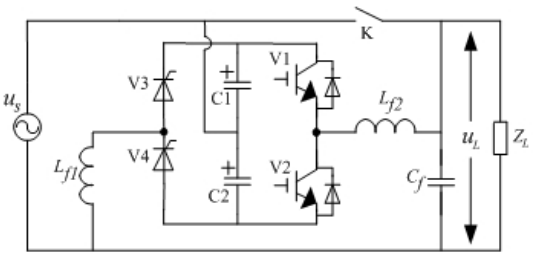


Fig. 2. Proposed topology of AVQR with controlled dc-link voltage.

III. Control Principle

Generally, the desired output voltage is a sinusoidal waveform with a constant magnitude and frequency for low power distribution systems. However, the supply voltage varies with a small range of deviations most of the time. That is, the required compensation voltage and the related dc-link voltage also vary in most cases. To obtain high efficiency of the AVQR for online operation, the dc-link voltage should adapt to supply voltage variations automatically. The principle of the proposed adaptive dc-link voltage control strategy is to reduce the dc-link voltage as low as possible on the premise of guaranteeing the regulator's compensation performance. By doing this, the system efficiency will be enhanced and the EMI problems of the inverter in the AVQR will also be greatly mitigated. A detailed analysis is demonstrated as follows.

Under the condition of undervoltages, an appropriate dc-link voltages can be obtained by properly triggering the thyristors V3 and V4, according to the supply voltage deviations. Energy is taken from the incoming supply through the thyristor rectifier and is delivered to the output side through the inverter to maintain full load power at the rated voltage.

When the supply voltage is an overvoltage, the energy will be injected into the dc-link capactiors C1 and C2 through the inverter, and the dc-link voltage will pump up, since the rectifier cannot directly feed the energy back to the distribution line. Then the thyristors V3 and V4 will be turned off. The equivalent circuit is shown in Fig. 3. In this situation, adaptive dc-link voltage control can be obtained by controlling the inverter with a phase shift control algorithm [15]–[17].

The adaptive dc-link voltage control block with the phase shift scheme is shown in Fig. 4, where u_S is the instantaneous value of the supply voltage, U_L is the rated output voltage magnitude (e.g. 220V, rms), u_{ref} is the instantaneous reference value of the desired output voltage, U_{dc1} and $U_{dc2}$are the dc-link voltages across C1 and C2, respectively, and u_L is the load voltage. The whole control block is mainly composed of two closed-loops. One is the output voltage control loop, and the other is the dc-link voltage control loop. Here, u_{ref} is generated according to u_S, U_L and the phase shift angle signal. The desired dc-link voltages can be obtained by the dc-link voltage setting block according to the errors between u_S and u_{ref}. Then the blocks of the dc-link voltage regulating and charging controls will regulate U_{dc1} and U_{dc2} by V3 and V4 to track the desired dc-link voltage. The block of the output voltage closed-loops control (e.g. a dual-closed-loop control with an inner current loop and an outer voltage loop) will control the inverter to regulate the output voltage with good steady-state and dynamic response characteristics [18].

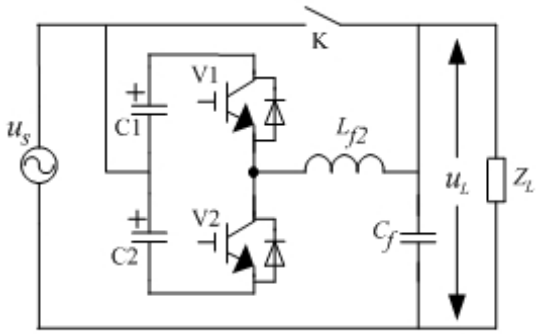


Fig. 3. Configuration when the charge circuit is turned off.

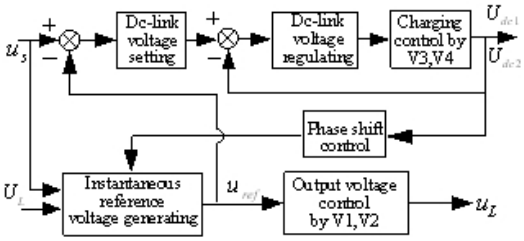


Fig. 4. Dc-link voltage control block with phase shift scheme.

When the supply voltage is an undervoltage, the in-phase compensation method is adopted. Then, the dc-link voltage regulating block will control the charging circuit by triggering the thyristors V3 and V4. When the supply voltage is an overvoltage, V3 and V4 are turned off and the dc-link voltage provides a reference for the phase shift compensation. If the dc-link voltage is below the threshold voltage for the shift phase scheme, the in-phase compensation method is applied, otherwise the shift phase compensation method is used [15]–[17]. Therefore, the regulation of the dc-link voltage is automatically realized by the control IGBTs V1 and V2, which can suppress the pumping-up of the dc-link voltage and ensure the safe operation of the AVQR.

IV. Realization of the Proposed Strategy

A. Realization of the Thyristor Controlled DC-link Voltage

As shown in Fig. 2, the supply voltage u_S is an ac voltage source with a constant frequency of 50Hz. The capacitor C2 can be charged through the thyristor V4 only in the positive half cycle of u_S, and the capacitor C1 can be charged through the thyristor V3 only in the negative half cycle of u_S. Therefore, in order to get the dc-link voltage under control, triggering thyristor V4 in the later quarter of the positive half cycle of the supply voltage u_S and triggering the thyristor V3 in the later quarter of the negative half cycle of the supply voltage u_S is a proper method. This is illustrated in Fig. 5, during the instant *t1* or *t2*.

In order to achieve adaptive dc-link voltage control, the error between the actual dc-link voltage and the required dc-link voltage is used to adjust the triggering angles of V3 and V4 through a P/PI regulator. By doing this, the actual dc-link voltage will automatically track the required dc-link voltage, and the dynamic response can be adjusted by the

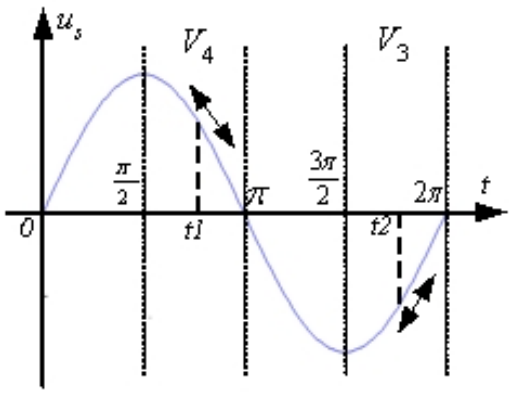


Fig. 5. Thyristor triggering pulses move range in one cycle.

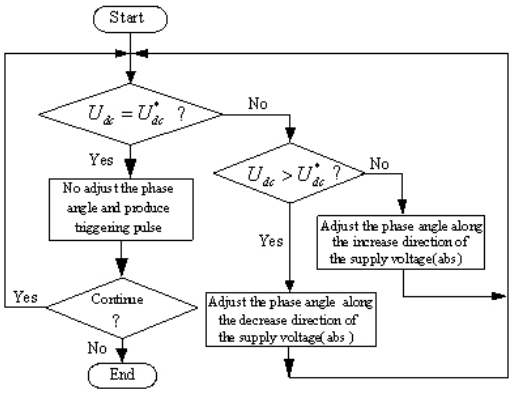


Fig. 6. Procedure flow chart of the adaptive dc-link voltage control.

P/PI regulator. Here, the required dc-link voltage, referred to as the dc-link voltage set value, is determined by the required compensation voltage.

The control process is realized by a digital signal processor (DSP), and the procedure flow chart is shown in Fig. 6, where U_{dc} is the actual dc-link voltage and U_{dc}^{*} is the dc-link voltage set value.

When $U_{dc} > U_{dc}^{*}$, the triggering angle should be increased to make U_{dc} lower. Conversely, it should be reduced to make U_{dc} rise. The purpose is to regulate U_{dc} properly to adapt to U_{dc}^{*}. The increment of the triggering angles in a cycle of the supply voltage is given by:

$$d = K_p(U_{dc}^{*} - U_{dc}) \tag{1}$$

where K_p is the proportional gain of the P regulator, which is an important parameter for adaptive dc-link voltage control and should be designed appropriately. Generally, a large K_p will contribute to both the accuracy and the fast dynamic response of the dc-link voltage. However, K_p cannot be designed to be too large. Otherwise, in case of $U_{dc} > U_{dc}^{*}$, the increase in the triggering angle may be so fast that the dc-link voltage cannot catch up with it, especially under a light load condition. As a sequence, when U_{dc} decreases to near U_{dc}^{*}, the triggering angle is larger than the expected one. Hence, a relatively low dc-link voltage appears over a period of time, which will induce a poor compensation performance to the AVQR. Conversely, if $K_p$is designed to be too small, the system's dynamic response will be slow. Thus, there is a compromise to be made in the design of K_p, which is mainly related to the load condition and the storage energy capacitors C1 and C2. How to choose a proper K_p will be discussed further in a future paper.

B. Determination of the DC-link Voltage Set Value

The design principle of the dc-link voltage set value is to set the value as low as possible on the premise of ensuring the compensation performance of the regulator.

1) DC-link Voltage Set Value for Undervoltage: When the supply voltage is an undervoltage, the in-phase compensation method is adopted. The dc-link voltage set value U_{dc}^{*} should be larger than the maximum deviation between the instantaneous values of the supply voltage and the rated output voltage. It can be given by:

$$U_{dc}^{*} = K_{dc} \times \max|u_L - u_S| \tag{2}$$

here u_L and u_S are the instantaneous values of the rated output voltage and the supply voltage, respectively, and K_{dc} is a coefficient greater than 1.0 to avoid over modulation. The typical range of K_{dc} is 1.2∼1.4. Here K_{dc} is selected to be equal to 1.3, and the minimum value of U_{dc}^{*} is designed to be 10V to ensure the compensation performance when the supply voltage is near the rated load voltage.

2) DC-link Voltage Set Value for Overvoltage: When the supply voltage is an overvoltage, the phase shift compensation scheme is adopted to regulate the dc-link voltage and to prevent the dc-link voltage from pumping-up [15]–[17]. The design of U_{dc}^{*} in this situation is different from (2), because the compensation voltage magnitude with phase shift control is much larger than that with the in-phase control. From [16], it is known that the compensation voltage achieves its maximum value in a pure resistance load. Therefore, U_{dc}^{*} should be set according to this case. Then the following equations can be obtained:

$$U_C = \sqrt{U_S^2 - U_L^2} \tag{3}$$

$$U_{dc}^{*} = K_{dc} \times \sqrt{2} U_C \tag{4}$$

here, $U_S$and U_L are the rms of the supply voltage and the rated output voltage, respectively, and U_C is the maximum compensation voltage.

According to (2)–(4), a comparison of the voltage magnitude across the capacitors (C1/C2) operating under a 1.1kW pure resistance load is shown in Fig. 7. As illustrated in Fig. 7, with different supply voltages, the blue line (◯) shows the dc-link voltages with a diode rectifier, while the green line (▽) and the red line (□) show the theoretical and experimental dc-link voltages with a thyristor rectifier, respectively. It can be seen that the dc-link voltages are reduced significantly by adopting the proposed topology and control strategy. As a result, the efficiency of the system will be improved remarkably as expected.

V. Losses Analysis and Comparison

Based on the similarities between the proposed topology and the conventional one, a detailed losses analysis and a

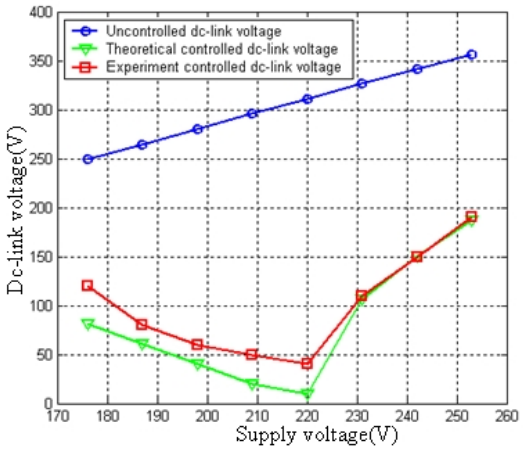


Fig. 7. Comparison of the dc-link voltage.

comparison are carried out. It is known that the losses of the two topologies include rectifier losses, inverter losses, filter capacitor and filter inductor losses, dc-link capacitor losses and some conduction wire losses. A 1.1kW purely resistive load with a rated load voltage of 220V(rms) is taken for granted in the paper, and the supply voltage is assumed to be 210V(rms). The main difference between the two topologies is the dc-link voltage control. Only the losses related to the dc-link voltage are considered, including the dc-link capacitor losses and the inverter losses. Under this condition, the dc-link voltage of the conventional topology is about 300V (nearly the natural commutation voltage), while for the proposed topology, the dc-link voltage is controlled to about 20V. The detailed calculations are as follows.

The losses of the dc-link capacitors are given by:

$$P_C = I_l U_{dc} + U_{ac}^2 \omega C tg\delta \tag{5}$$

where U_{dc} and U_{ac} are the dc and ac voltages across the capacitors, I_l is the leakage current under the dc voltage, C is the capacitor's capacity, and $tg\delta$ is the tangent of the loss angle under the rated temperature and angle frequency ω.

The losses of a single IGBT and its anti-parallel diode, including the conduction loss and the turn-on and turn-off losses, can be calculated from [19].

Using (5) and the data sheets of the components and devices, the losses of the conventional AVQR with a diode uncontrolled rectifier and those of the proposed topology can be easily obtained. The results of the loss analysis are listed in Table I. As depicted in Table I, the total losses of the proposed topology are 37.12W, while the total losses of the conventional one are 80.78W. That is, the losses are decreased by nearly 54% and the efficiency is increased by 4.5% by adopting the proposed topology under a resistance load of 1.1kW.

VI. Simulation and Experimental Results

In order to verify the effectiveness of the proposed topology and control method, detailed simulations and experiments are carried out on a single-phase 2kVA prototype. The main parameters are listed in Table II.

TABLE I
Comparison of the Losses

Losses	Topology	
	Diode rectifier	Thyristor rectifier
Dc-link capacitors losses(W)	30.1	3.61
IGBT's conduction losses(W)	3.70	5.22
Anti-parallel diode's conduction losses (W)	2.48	1.09
IGBT's turn-on and turn-off losses (W)	19.6	0.80
Rectifier unit losses (W)	3.70	5.20
Filter inductor losses (W)	12.1	12.1
Wire losses (W)	9.10	9.10
Total losses(W)	80.78	37.12

TABLE II
220V/2kVA AVQR System Parameters

Test Parameters	Nominal Values
Capacity of the AVQR	2kVA, single-phase
Rated load voltage	220V(rms), 50Hz
Switching frequency	15kHz
Dc-link capacitor C1, C2	4700 μF/450Vdc
Filter Inductor L_{f1}, L_{f2}	0.75mH
Filter capacitor C_f	20μF
Load Z_L	44Ω, resistor

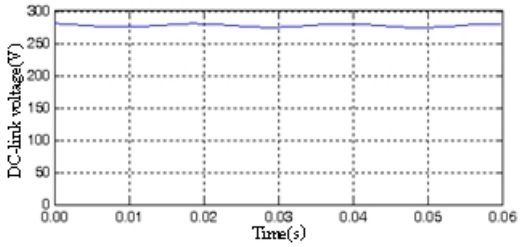
A. Simulation Results

The simulations of the proposed AVQR with adaptive dc-link voltage control in MATLAB/SIMULINK are carried out as follows. Here, the load is a resistance and the losses of the regulator are not taken into consideration.

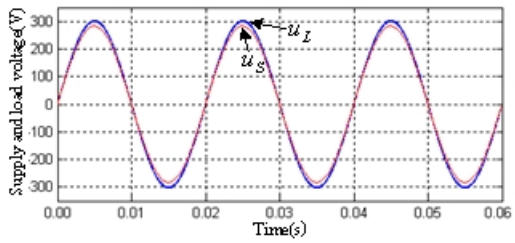
Fig. 8 and Fig. 9 show the simulation waveforms of the dc-link voltage of the capacitor C1 and the output voltage with a diode uncontrolled rectifier and with a thyristor controlled one, respectively, while the supply voltage is 200V (rms, undervoltage). Fig. 10 and Fig. 11 show the respective waveforms while the supply voltage is 240V (rms, overvoltage). The waveform of the dc-link voltage of the capacitor C2 is the same as C1 ideally. Therefore, the waveform of the dc-link voltage of the capacitor C1 is presented.

Comparing Fig. 8 and Fig. 9 in the undervoltage case, the supply voltage and output voltage are almost the same, but the dc-link voltage of the capacitor C1 makes a large difference, that is, the dc-link voltage of the capacitor C1 is about 280V in Fig. 8(a), but only about 40V in Fig. 9(a), which is controlled by the thyristors. This comparison indicates that the reduced dc-link voltage is sufficient for ensuring the compensation performance. It should still be noticed that there is a slight fluctuation in the dc-link voltage as shown in Fig. 9(a), which is caused by the thyrisitor controlled rectifier. However, this slight fluctuation has no effect on the compensation performance.

Comparing Fig. 10 and Fig. 11 in the overvoltage case, similar results can be obtained as in the undervoltage case. The reduced dc-link voltage with a thyristor controlled rectifier is sufficient for meeting the compensation performance. However, there is a difference between the overvoltage and the undervoltage cases. The dc-link voltage of the capacitor C1 with a diode uncontrolled rectifier is about 340V in Fig. 10(a). This is a little more than the peak value of the supply voltage, because, with phase shift compensation scheme, the dc-link voltage should be larger than the natural commutation

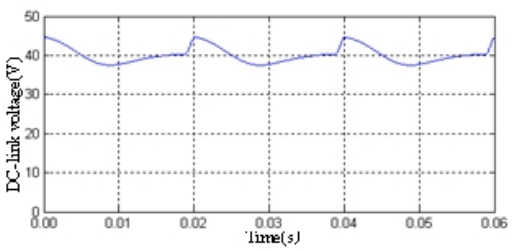


(a)

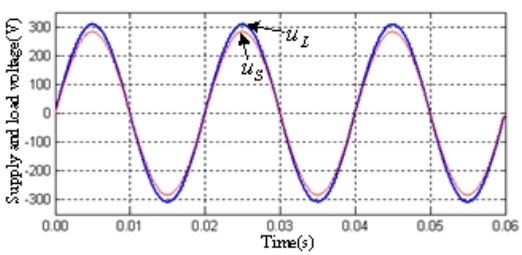


(b)

Fig. 8. Simulation result of undervoltage case with diode rectifier: (a) dc-link voltage, (b) supply voltage (u_S) and load voltage (u_L).

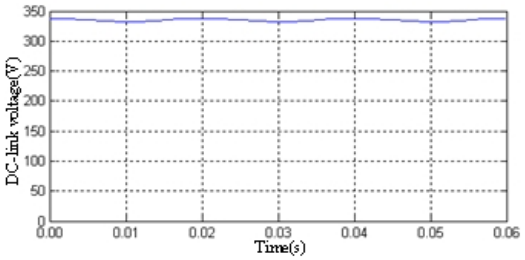


(a)

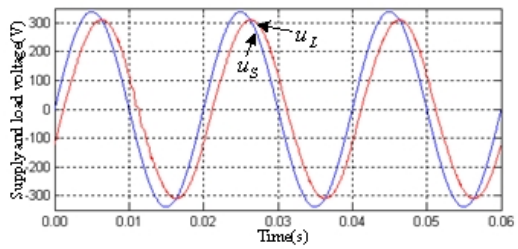


(b)

Fig. 9. Simulation result of undervoltage case with proposed scheme: (a) dc-link voltage, (b) supply voltage (u_S) and load voltage (u_L).

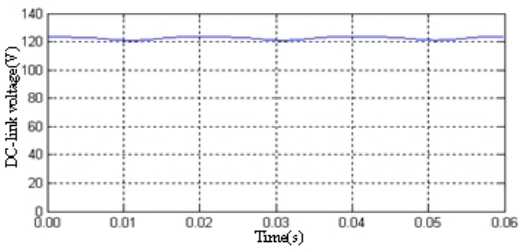


(a)

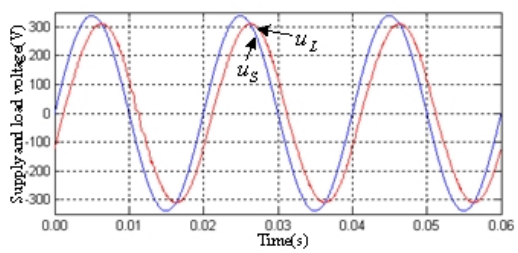


(b)

Fig. 10. Simulation result of overvoltage case with diode rectifier: (a) dc-link voltage, (b) supply voltage (u_S) and load voltage (u_L).



(a)



(b)

Fig. 11. Simulation result of overvoltage case with proposed scheme: (a) dc-link voltage, (b) supply voltage (u_S) and load voltage (u_L).

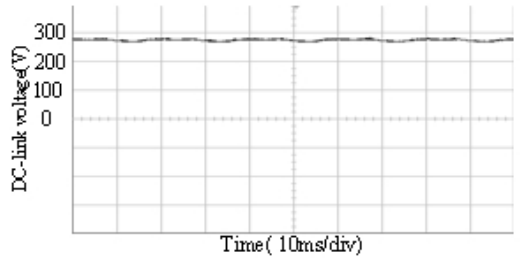
voltage to ensure the forced turning off the diodes [16]. In fact, the dc-link voltage is controlled only by the IGBTs under this condition. However, in the proposed topology, the thyristors can be controlled to turn off as shown in Fig. 3. Therefore, the dc-link voltage can be controlled by the IGBTs to be as low as possible on the premise of meeting the compensation performance of the AVQR. As shown in Fig. 11(a), the dc-link voltage is about 120V, which is enough to satisfy the compensation performance.

From Figs. 8–11, it can be seen that whether the supply is an undervoltage or an overvoltage, the dc-link voltage decreases significantly by adopting the proposed topology and the adaptive dc-link control strategy. As a result, the voltage stress and switching losses of the inverter will decrease significantly, while the duty ratio of the inverter will increase, and the compensation performance as well as the system efficiency will be improved remarkably.

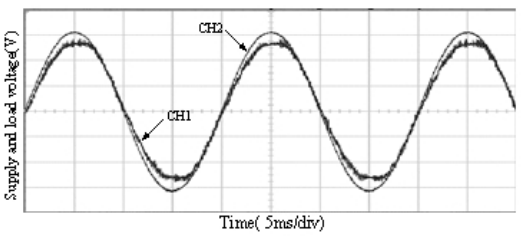
B. Experimental Results

A detailed experimental study has been carried out on a single-phase 2kVA prototype in order to verify the validity of the proposed topology and control strategy.

Fig. 12 and Fig. 13 show the experimental waveforms of the undervoltage case, where the supply voltage is 200V(rms). Fig. 12(b) and Fig. 13(b) show that the proposed system has almost the same compensation performance as the conventional one.



(a)



(b)

Fig. 12. Experimental result of undervoltage case (200V,rms) with diode rectifier: (a) dc-link voltage, (b) supply voltage (CH1, 100V/div) and output voltage (CH2, 100V/div).

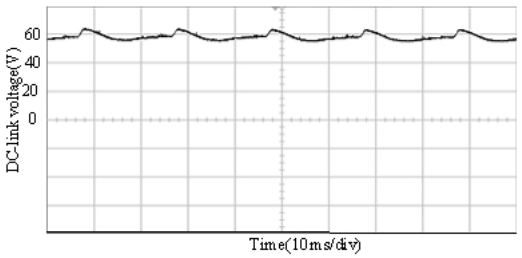
Fig. 13(a) shows that the dc-link voltage of the proposed topology (about 60V) is much lower than that of the conventional one (about 280V), which will be helpful for increasing the system efficiency.

Fig. 14 and Fig. 15 illustrate the experimental results of the overvoltage case, where the supply voltage is 240V(rms). In Fig. 14, the dc-link voltage value of the capacitor C1 is 340V. Nevertheless, in Fig. 15, the dc-link voltage of the capacitor C1 is controlled to 132V by the inverter. With the shift phase control algorithm, between the supply voltage and the output voltage, there is a phase difference angle in the steady state, as shown in Fig. 14 and Fig. 15.

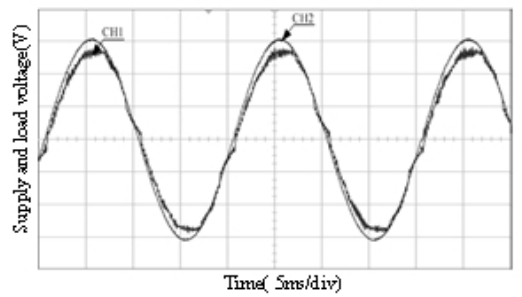
It can be seen that the experimental results shown in Figs. 12-15 are consistent with the simulations (Figs. 8-11). The same conclusion can be reached, that the dc-link voltage can be decreased without any performance degradation by employing the proposed scheme. Hence, higher efficiency can be expected.

Fig. 16 shows the case where the supply voltage contains a fundamental component of 200V(rms) and some harmonics (5th, THD = 28.8%), which can damage voltage sensitive loads. The output voltage is regulated to be an almost perfect sinusoidal waveform (220V, THD=0.4%) with the proposed system.

The output of the adaptive regulation of the dc-link voltage following supply voltage variations is shown in Fig. 17, where the supply voltage is increased from 170V to 220V(rms) and then decreased from 220V to 170V(rms) periodically. When the supply voltage is decreasing to a relatively low level (170V, i.e. the missing load voltage is 50V), the dc-link voltage is regulating to a high value (about 110V). When the supply voltage is increasing to a relatively high value (220V, i.e. the missing load voltage is 0V theoretically), the dc-link voltage is regulating to a low value (about 30V) adaptively. However, the output voltage is maintained at about 220V(rms) without



(a)



(b)

Fig. 13. Experimental result of the proposed when supply voltage is undervoltage(200Vrms): (a) dc-link voltage, (b) supply voltage (CH1, 100V/div) and output voltage (CH2, 100V/div).

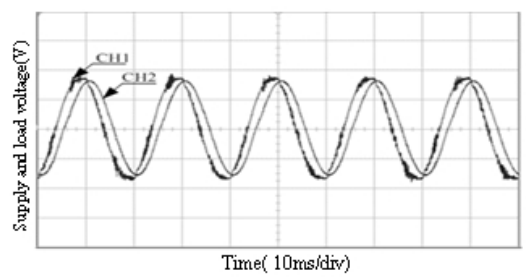


Fig. 14. Supply voltage (CH1, 200V/div) and output voltage (CH2, 200V/div) with diode rectifier when overvoltage.

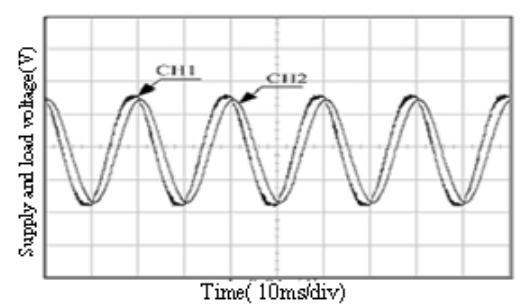


Fig. 15. Supply voltage (CH1, 200V/div) and output voltage (CH2, 200V/div) with proposed system when overvoltage.

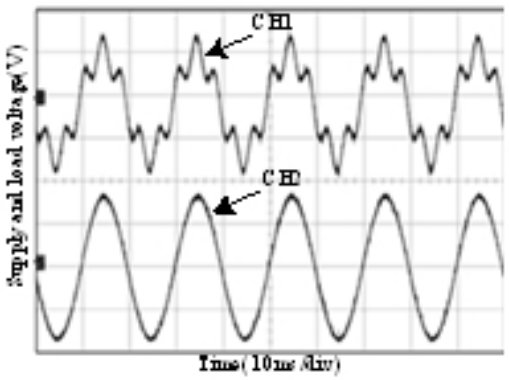


Fig. 16. Experimental result of compensating harmonics (CH1: supply voltage, CH2: output voltage, 200V/div).

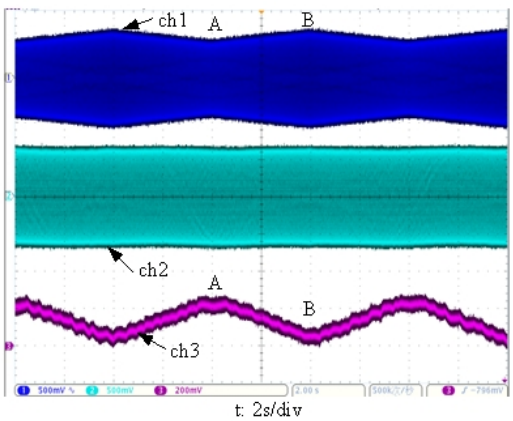


Fig. 17. Experimental result of the proposed scheme when the supply voltage is continuously varying in a range of 170 V-220 V. (CH1: supply voltage, 250V/div; CH2: output voltage, 250V/div; CH3: dc-link voltage, 100V/div).

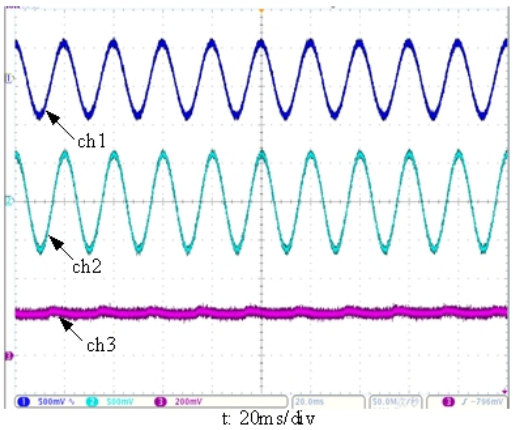


Fig. 18. Zoomed in waveforms around point A in Fig. 17. (CH1: supply voltage, 250V/div; CH2: output voltage, 250V/div; CH3: dc-link voltage, 100V/div).

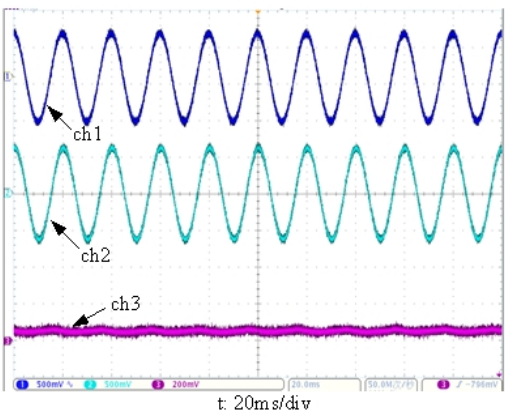


Fig. 19. Zoomed in waveforms around point B in Fig. 17. (CH1: supply voltage, 250V/div; CH2: output voltage, 250V/div; CH3: dc-link voltage, 100V/div).

any change, despite the fact that the supply voltage is varying continuously. The zoomed in views around the relatively low (point A) and high (point B) supply voltages are shown in Fig. 18 and Fig. 19, respectively. From Fig. 18 and Fig. 19, it can be easily seen that the waveforms of the output voltage are almost perfectly sinusoidal without any distortions during the adaptive regulation process of the dc-link voltage.

Furthermore, the efficiencies of the conventional topology and the proposed topology are also tested to show a contrast on the 2kVA prototype, where the rated load voltage is 220V(rms) and the load is a pure resistance of 44Ω. The related experimental results, from which the system efficiency can be easily obtained, are provided by a power quality analyzer HIOKI 3193 (made in Japan).

When the supply voltage is 170V, 190V, 210V and 240V(rms), respectively, a comparison of the efficiency with both the uncontrolled and the controlled dc-link voltages is demonstrated in Fig. 20. As can be seen in Fig. 20, the efficiency of the proposed topology with the controlled dc-link voltage is improved considerablely from the one uncontrolled, especially when the supply voltage is an overvoltage. Detailed experimental results when the supply voltage is 210V and 240V(rms) are presented in Table III–Table VI.

Table III and Table IV show the input and output power with the diode rectifier and with the thyristor rectifier in the case of an undervoltage (210V, rms), respectively. It can be seen that, the system efficiency is increased from 89.1% to 96.1% by replacing the diode rectifier with a thyristor rectifier and by adopting the proposed control strategy. That is, there is an increase of 7.0% in efficiency under the same supply voltage and load conditions, which is very important for practical applications.

Table V and Table VI list the experimental results corresponding to the case of an overvoltage (240V, rms). Similarly, the efficiency is remarkably increased from 86.2% to 95.6%. Therefore, there is an increase of 9.4% in the efficiency under the same supply voltage and load conditions by adopting the proposed topology and the adaptive dc-link voltage control strategy.

Comparing the proposed system with a conventional AVR (i.e. electronic tap-changed transformers), the proposed scheme is superior to the later in terms of compensation performance and having the capability of voltage harmonics suppression. Compared with DVR systems, the proposed system can operate in online mode to regulate the load voltage continuously for undervoltages/overvoltages, voltage imbalances and voltage harmonics, while DVRs are suitable for offline operation to mitigate deep sags/swells effectively [4], [5]. Compared with the IAVR presented in [7], [8], the structure

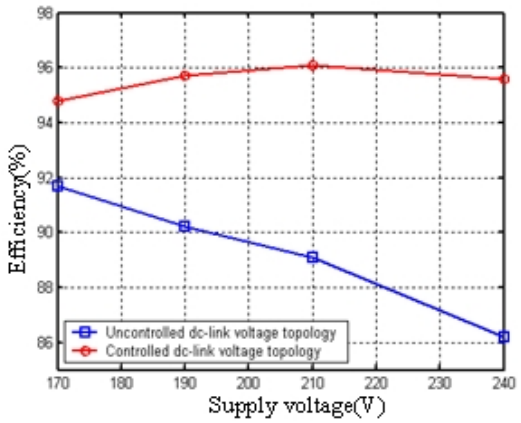


Fig. 20. Comparison of the efficiency.

TABLE III
INPUT AND OUTPUT POWER WITH DIODE RECTIFIER (UNDERVOLTAGE)

Item	Input	Output
U(V)	210.41	220.59
I(A)	7.654	5.066
P(W)	1255.3	1118.7
$\cos\varphi$	0.7794	1.0000

proposed in this paper is mainly used to solve the long duration variations and steady state voltage quality problems other than deep sags/swells. The system presented in [7], [8] has the merit of continuous regulation capability for the entire range of voltage variations. However, the system efficiency cannot be very high due to the high dc-link voltage, especially in overvoltage situations.

VII. CONCLUSIONS

It should be noted again that the short duration variations and the long duration variations of voltage differ greatly from each other both in terms of magnitude and duration. It is more reasonable and cost-effective to deal with them separately. DVRs can solve short duration variations efficiently, while AVQRs are good candidates for long duration variations. Nevertheless, the efficiency of conventional AVQRs operating in online mode is not satisfactory because of the high dc-link voltages.

Focusing on efficiency, this paper proposes a transformerless and highly efficient AVQR topology with an adaptive dc-link voltage control. The proposed topology can solve long duration variations, voltage imbalances and voltage harmonics efficiently. It is superior to the conventional topologies by providing an additional function for regulating the dc-link voltage. On the premise of ensuring good compensation performance, the dc-link voltage of the proposed topology can be controlled to adapt to the missing load voltage automatically, which is much lower than that of the conventional ones. This provides benefits including a larger duty ratio of the inverter, a lower dead-time effect, fewer EMI problems, and higher efficiency of the system. Analytical, simulation, and experimental results have been presented, all of which prove the superiority of the proposed scheme.

In conclusion, the proposed transformerless AVQR with adaptive dc-link voltage control is a better choice than the conventional ones for practical application.

TABLE IV
INPUT AND OUTPUT POWER WITH THYRISTOR RECTIFIER (UNDERVOLTAGE)

Item	Input	Output
U(V)	209.69	220.26
I(A)	7.721	5.055
P(W)	1160.0	1115.1
$\cos\varphi$	0.7165	1.0000

TABLE V
INPUT AND OUTPUT POWER WITH DIODE RECTIFIER (OVERVOLTAGE)

Item	Input	Output
U(V)	240.60	221.45
I(A)	5.904	5.145
P(W)	1323.4	1140.6
$\cos\varphi$	0.9316	1.0000

TABLE VI
INPUT AND OUTPUT POWER WITH THYRISTOR RECTIFIER (OVERVOLTAGE)

Item	Input	Output
U(V)	240.03	221.56
I(A)	5.703	5.201
P(W)	1207.6	1154.2
$\cos\varphi$	0.8822	1.0000

ACKNOWLEDGMENT

This paper and its related research work were supported by the national Natural Science Foundation of China (NSFC) (project no. 50877065)

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