JPE 11-6-19

Improved Active Power Filter Performance Based on an Indirect Current Control Technique

Mohamed Adel†, Sherif Zaid*, and Osama Mahgoub*

† Faculty of Engineering, Banha University, Qalyobia, Egypt
* Faculty of Engineering, Cairo University, Giza, Egypt

Abstract

This paper presents a method for the performance improvement of a shunt active power filter (SAPF) using the indirect current control (ICC) scheme. Compared to the conventional direct current control (DCC) scheme, the ICC gives better performance with a lower number of sensors. A simplified and efficient control algorithm using a low cost Intel 80C196KC microcontroller is implemented using only two current sensors for the source current and one voltage sensor for the DC-link voltage of the SAPF circuit. The objective is to eliminate harmonics and to compensate the reactive power produced by non-linear loads such as an uncontrolled rectifier feeding an inductive load. The APF is realized using a three phase voltage source inverter (VSI) with a dc bus capacitor. Experimental results are presented to prove the better performance of the ICC method over the DCC one.

Key Words: Active power filter, Direct current control, Indirect current control, Total harmonic distortion

I. Introduction

Harmonic pollution caused by nonlinear loads such as electric arc furnaces, electric arc welders, adjustable speed drives and switch mode power supplies has become a serious problem in electrical power systems. These loads generate a lot of harmonic currents, which are injected into the power system. The flow of these harmonic currents through the system causes a voltage distortion due to a harmonic voltage drop across the system series impedance. As a result, the harmonic producing loads and all of the other loads supplied from the point of common coupling will be affected by this harmonic voltage distortion. The concerns related to harmonic distortions are increased due to their unwanted effects such as resonance on the series and parallel circuits, additional losses in feeders, transformers and rotating electric machines, faulty operation of protection systems, errors of measuring instruments, and malfunction and low-efficiency of sensitive loads [1].

Conventionally, passive filters have been used to limit the harmonic currents in power distribution systems. However, they have several drawbacks such as the inability to compensate random frequency variations in currents, degradation of the filtering performance due to parameter variations, tuning problems, and parallel resonance [2]. In order to solve these problems, the APF has been designed to cancel the current harmonic distortion by injecting the same distortion, but with the opposite polarity, thereby improving power quality [3], [4].

Most of the time-domain control schemes used in APFs are based on the DCC method, in which the reference current of an APF is generated based on sensing both the non-linear load and the actual APF currents. The load current is used for extracting the harmonics and the reactive component, while the actual APF current is used for tracking the reference one [5], [6]. As a result, the minimum number of current sensors used in this method is four. Instead, a simple and easily implemented alternative scheme, is the ICC method, in which the desired source current is determined without sensing the load current, and the APF is controlled such that the source current tracks the desired value [7]–[11].

In this paper, a simplified control algorithm for the ICC scheme is implemented and compared with the DCC scheme. The principles of this control scheme are described and the effectiveness of the proposed method is verified via simulations and experimental work, using only two current sensors for the source current measurement and one voltage sensor for the DC-link voltage of the APF.

II. Compensation Principle of Icc Method

The basic principle of ICC for harmonics and reactive power compensation using a SAPF is shown in Fig. 1. The non-linear load current contains fundamental and harmonic components,

Manuscript received Jan. 27, 2011; revised Oct. 4, 2011
Recommended for publication by Associate Editor Kyo-Beum Lee.
† Corresponding Author: madel_ss@yahoo.com
Tel: +20-1332-31011, Fax: +20-1332-27491, Banha University
* Faculty of Engineering, Cairo University, Egypt

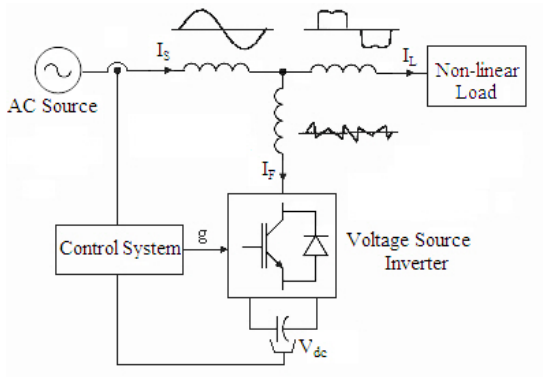

Fig. 1. Shunt Active Power Filter.

which can be written as:

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \varphi_n),$$

$$= I_1 \sin(\omega t + \varphi_1) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) \quad (1)$$

$$= I_{1a} \sin(\omega t) + I_{1r} \cos(\omega t) + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n) \quad (2)$$

where $I_{1a} = I_1 \cos(\varphi_1)$ and $I_{1r} = I_1 \sin(\varphi_1)$

In (2), there are three terms:

The terms $I_{1a} \sin(\omega t)$ and $I_{1r} \cos(\omega t)$ refer to the active and reactive components of the fundamental load current respectively, while the term $\sum_{n=2}^{\infty} I_n \sin(n\omega t + \varphi_n)$ refers to the load current harmonic component.

According to Fig. 1, the source current is given by:

$$i_S(t) = i_L(t) + i_F(t). \quad (3)$$

A perfect SAPF supplies both the harmonics and the reactive components of the load current, so that the source current supplies only the active component of that current, or $i_S(t) = I_{1a} \sin(\omega t)$. Therefore, the source current will be sinusoidal and in phase with the source voltage.

In the ICC method for a SAPF, the peak value of the source current is estimated in order to keep the energy balance between the source and the load. In practice, because of the switching losses in the PWM inverter and the leakage of the DC capacitor, the active filter draws a fundamental active component to maintain the DC capacitor voltage at its desired value. Then, the total current supplied by the AC source will be:

$$i_S(t) = I_{1a} \sin(\omega t) + I_{Floss} \sin(\omega t) = I_S \sin(\omega t) \quad (4)$$

where I_{Floss} is the fundamental active component of the SAPF current. The amplitude of the source current is obtained over the control of the DC-link voltage.

III. The Proposed Icc Scheme

A simplified block diagram of the ICC scheme for a SAPF is shown in Fig. 2, in which a PI controller is used to keep the DC-link voltage at a predetermined value such that [12];

$$V_{dc}^* \geq \frac{2\sqrt{2}}{\sqrt{3}} V_{LL} \quad (5)$$

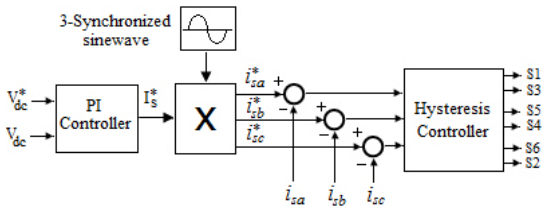

Fig. 2. Block diagram of the ICC scheme.

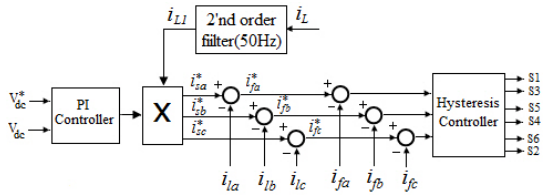

Fig. 3. Block diagram of the DCC scheme.

where V^*_{dc} is the reference DC-link voltage and V_{LL} is the line to line source voltage.

The output of the PI controller is considered as the reference peak value (I_S^*) of the source current.

A phase-locked-loop (PLL) circuit is used to generate three sinusoidal signals synchronized with the three phase source voltages. Then the instantaneous reference source currents are generated by multiplying these signals by the estimated I_S^*. The switching pattern of the SAPF circuit is generated by a hysteresis controller through which the instantaneous three phase source currents track their estimated reference values.

The advantage of this scheme is its independence from the instantaneous values of the source voltages. As a result of this, the estimated reference currents are kept sinusoidal and balanced even if the source voltages are distorted or unbalanced.

IV. The Conventional Dcc Scheme

A block diagram of the conventional DCC scheme is shown in Fig.3. The load current is measured and its fundamental component (i_{L1}) is extracted using a second order band bass filter [13].

This fundamental component is multiplied by the output of the PI controller to generate a reference waveform of the source current ($i_s{}^*$). The reference currents of the APF are estimated by subtracting the measured load currents from the instantaneous reference source currents. In this method, the extraction of the harmonic contents from the load current is strongly dependent on the type and order of the filter used. Therefore, the resultant current is not purely sinusoidal and its harmonic content is added to the harmonics resulting from the switching ripples of the source current. In ICC, the generated reference current is sinusoidal. As a result, the harmonic content may only be due to the switching ripples of the source current.

Form the practical implementation point of view, these additional tasks are overhead on the software algorithm. This is especially true for low speed microcontrollers, in which the analog to digital (A/D) conversion time is high and takes most of the sampling period. Therefore, reducing the number of analog signals to be read is a very effective method for

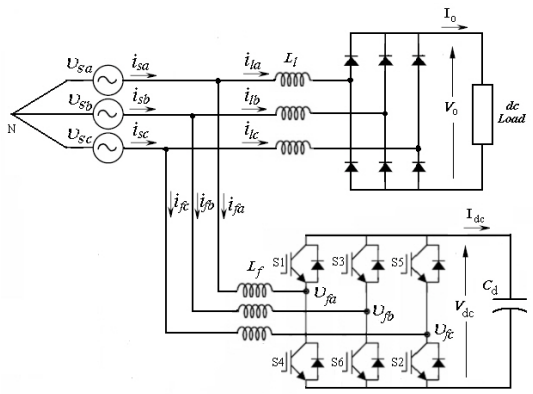

Fig. 4. The three phase SAPF circuit.

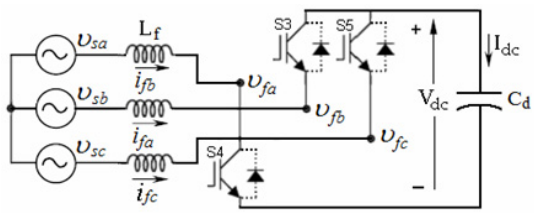

Fig. 5. Representation of a particular switching state for VSI.

increasing the sampling frequency and thereby improving the APF performance. This concept is the key for this study, where the ICC scheme uses three A/D channels; one for the DC link voltage and the others for the two phases of the source currents.

V. Operation And Model of a SAPF

A three phase SAPF system is shown in Fig.4. The APF circuit consists of a three phase VSI using six IGBT switches with a line inductor L_f to limit the magnitude of the input ripple current into the filter circuit, and the DC bus of the VSI is connected to an energy storage capacitor C_d. A three phase diode bridge rectifier, which acts as a non-linear load, is connected to the point of common coupling (PCC) through an inductor $L_l$to limit the large *di/dt* of the load current.

The six IGBT-diode combination switches of the VSI can be classified into high-side and low-side switches, forming a conjugate pair per phase. The simultaneous operation of a conjugate pair is not allowed to prevent short circuit faults. At any instant, only three of the six switches participate in current conduction. Assuming negligible conduction drops across the switches, an equivalent diagram of the VSI according to the switching states (S1 S3 S5) = (0 1 1) is presented in Fig. 5.

The equations representing the switching state in Fig. 5 are developed due to the filter voltage v_{fa} which takes the values of $(\pm\frac{2}{3}V_{dc})$ or $(\pm\frac{1}{3}V_{dc})$depending on the switching state. As a result:

$$\frac{di_{fa}}{dt} = \frac{1}{L}(V_{sa} + \frac{2}{3}V_{dc}) \tag{6}$$

$$\frac{di_{fb}}{dt} = \frac{1}{L}(V_{sb} - \frac{1}{3}V_{dc}) \tag{7}$$

$$\frac{di_{fc}}{dt} = \frac{1}{L}(V_{sc} - \frac{1}{3}V_{dc}) \tag{8}$$

Similarly, equations can be generated for the remaining valid switching states according to Table I.

TABLE I
Possible Switching States with Filter Voltages and DC Currents

	S_1 S_3 S_5	V_{fa} V_{fc} V_{fc}	I_{dc}
1	1 0 0	(2/3)V_{dc} (-1/3)V_{dc} (-1/3)V_{dc}	i_{fa}
2	1 1 0	(1/3)V_{dc} (1/3)V_{dc} (-2/3)V_{dc}	$-i_{fc}$
3	0 1 0	(-1/3)V_{dc} (2/3)V_{dc} (-1/3)V_{dc}	i_{fb}
4	0 1 1	(-2/3)V_{dc} (1/3)V_{dc} (1/3)V_{dc}	$-i_{fa}$
5	0 0 1	(-1/3)V_{dc} (-1/3)V_{dc} (2/3)V_{dc}	i_{fc}
6	1 0 1	(1/3)V_{dc} (-2/3)V_{dc} (1/3)V_{dc}	$-i_{fb}$

TABLE II
System Parameters

AC line voltage	100V, 50Hz
Ref. DC-bus voltage	220V
Line inductances	5mH
DC-link capacitor	1000μF
PI Controller: Kp, Ki	0.2, 10
Hysteresis band	10%
Sampling time	20us

The filter voltages can be represented as function of the switching states as follows:

$$\upsilon_{fa} = \frac{V_{dc}}{3}(2S1 - S3 - S5) \tag{9}$$

$$\upsilon_{fb} = \frac{V_{dc}}{3}(-S1 + 2S3 - S5) \tag{10}$$

$$\upsilon_{fc} = \frac{V_{dc}}{3}(-S1 - S3 + 2S5) \tag{11}$$

where, S1, S3, and S5 are the high-side switching functions of the inverter. If a switch is open S is digitally equal to "zero" whereas if a switch is closed S equals "one".

The dc-bus voltage can be expressed as:

$$\frac{dV_{dc}}{dt} = \frac{I_{dc}}{C_d} \tag{12}$$

where, I_{dc} is the dc capacitor current, which expressed as:

$$I_{dc} = i_{fa}S1 + i_{fb}S3 + i_{fc}S5. \tag{13}$$

Equations (6)-(13) are used to develop the APF model under any switching techniques.

A simulation platform using MATLAB is built to evaluate the performance of the APF under different operating conditions. The system parameters, shown in Table II, are estimated according to the design procedures proposed in [14].

Fig. 6 shows the SAPF performance with ICC in comparison with DCC according to a step change in the load.

From these results, it can be seen that the load current has a distorted waveform (6.b) with a THD value of 22%. It can also be seen that the source current settles to its steady state value within two cycles for both ICC (6.c) and DCC (6.d). Furthermore, it can be seen that the dc link voltage due to ICC dips to 205V and settles at its reference value within three cycles (6.e), while in DCC this voltage oscillates between 205V and 228V with a settling time of about four cycles (6.f).

Figs 7 and 8 show the harmonic spectrum of the source current after compensation according to ICC and DCC, respectively. The THD value of the source current is 1.3% for ICC while it is 2.5% for DCC. This is due to the lower values of the low order harmonics due to ICC when compared to DCC.

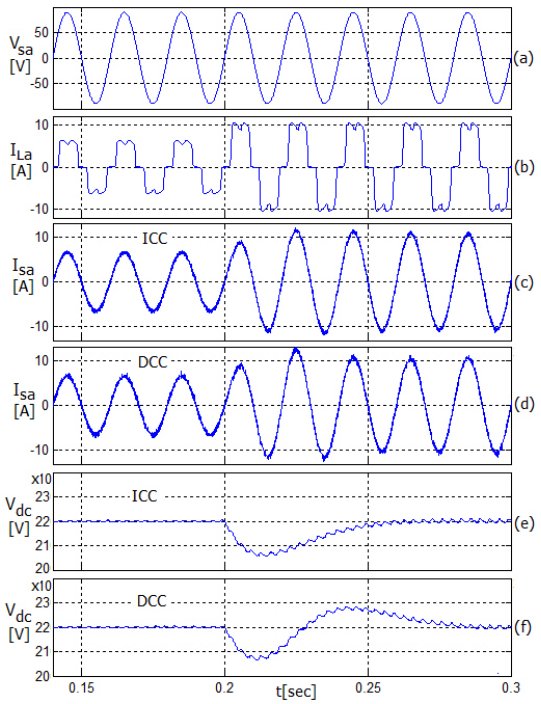

Fig. 6. SAPF performance due to step change in load current.

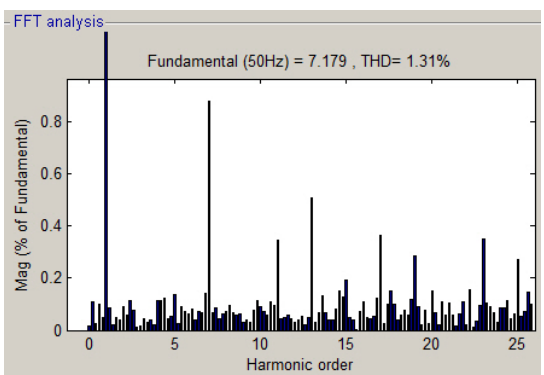

Fig. 7. Harmonic spectrum of the source current according to ICC.

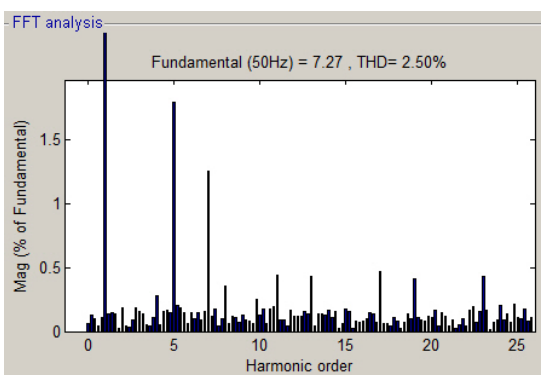

Fig. 8. Harmonic spectrum of the source current according to DCC.

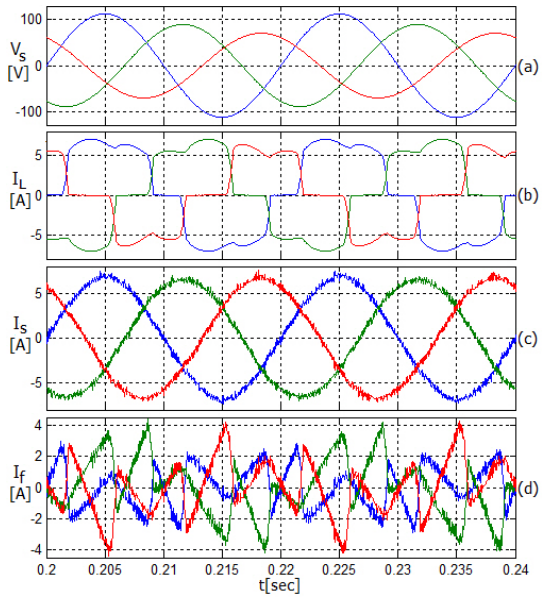

Fig. 9. SAPF response under unbalanced source voltages.

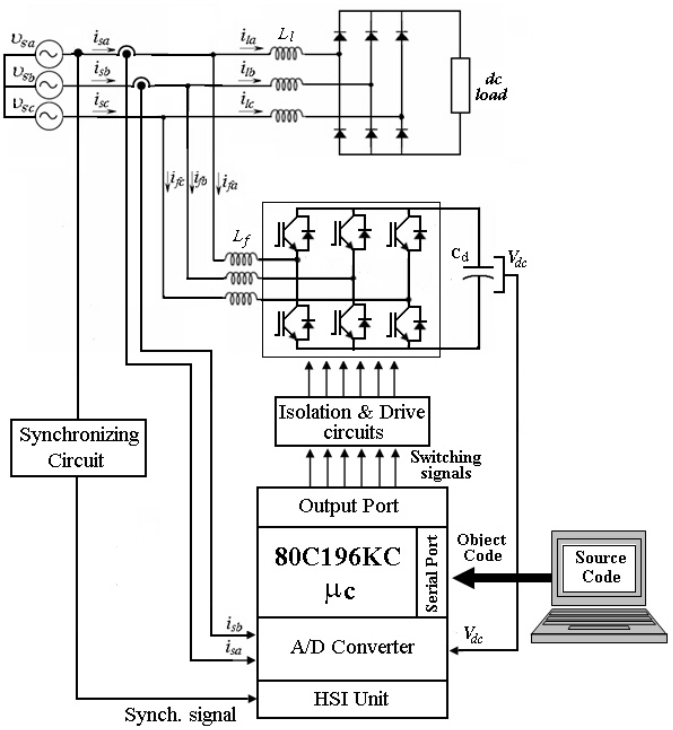

Fig. 10. Block diagram of the experimental setup.

Fig. 9 shows the SAPF response according to ICC under unbalanced source voltages. Since the source voltages are unbalanced (9.a), the load currents are also unbalanced (9.b). However, the source currents are still balanced and sinusoidal (9.c).

VI. Experimental Setup and Results

A block diagram of the proposed experimental setup is shown in Fig.10. The principle connections between the different elements in the complete system are indicated.

The software algorithm is implemented using an Intel 80C196KC 16-bit microcontroller, which provides an A/D

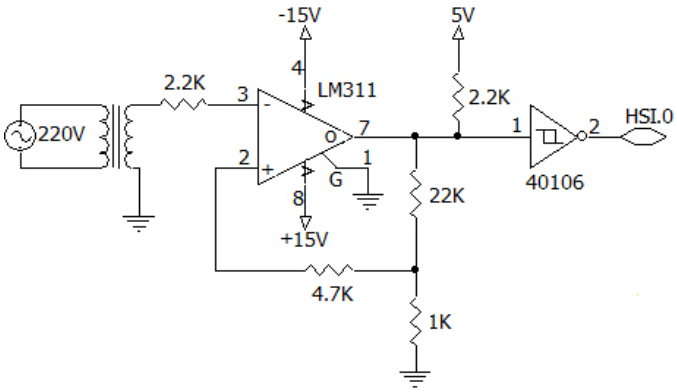

Fig. 11. Schematic diagram of the synchronizing circuit.

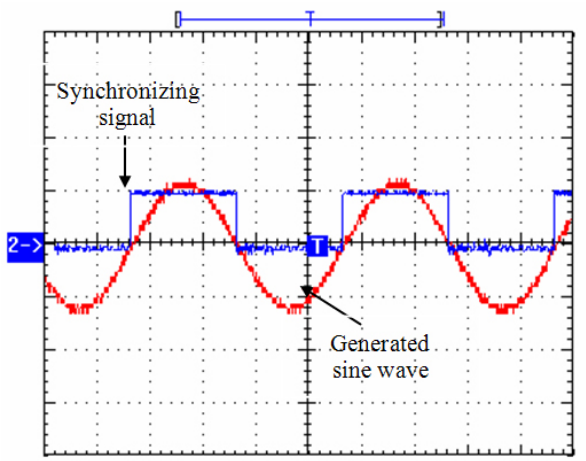

Fig. 12. Synchronizing signal and generated sine wave.

converter with multiplexed eight-input channels used for the various A/D operations required by the control algorithm. The output ports provided by this controller are used to output the switching signals required for the IGBT drive circuit. A synchronizing circuit, shown in Fig.11, generates a square wave at the power frequency every zero-crossing transition of the source voltage waveform. A high-speed input unit (HSI) is used to capture the positive rising edge of the synchronizing signal.

A unity sine wave is stored in a lookup table (LUT) in the microcontroller memory. The pointer of the LUT starts with a zero count every positive transition and is then incremented every sampling period. This enables the formation of the PLL by which a unity sine wave is generated at the power frequency and synchronized with the source voltage, as shown in Fig.12.

The 80196 controller has a 16MHz clock and a 19.75μs A/D time, which is a relatively large conversion time when compared to that of a DSP. Thus, the A/D conversion time plays an important role in selecting a suitable sampling period. Therefore, reducing the number of analog signals to be read by the A/D channels, significantly reduces the sampling time and hence increases the switching frequency which in turn improves the SAPF performance. From the experimental results, the average switching frequency for the ICC method is 4KHz, while it is 2.5KHz for the DCC method.

Fig. 13 shows the SAPF performance according to the ICC scheme.

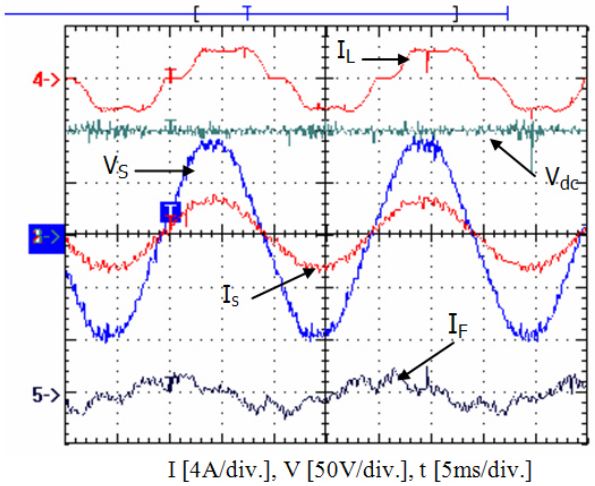

Fig. 13. SAPF performance according to ICC scheme.

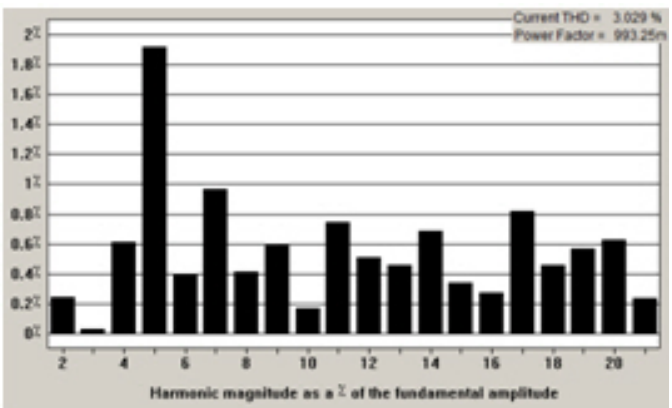

Fig. 14. Source current harmonic spectrum according to ICC scheme.

Before compensation, the source current has a low quality waveform with a THD value of 17.48%. After compensation, the source current appears to be sinusoidal and in phase with the source voltage and it has a low THD value of 3.03%, as shown in Fig. 14.

Fig. 15 shows the SAPF performance according to the DCC scheme in which the THD value of the source current is 5.05%, as shown in Fig. 16.

Table III presents an analytical comparison between the ICC and the DCC schemes applied to the SAPF.

It can be observed, from the current harmonic spectrum, that there are some even harmonics due to the asymmetry in the ripple components of the current waveform. However, these even harmonics have a lower amplitude in the ICC method. In addition, the source current peak to peak ripple values is low in the ICC method when compared to that of the DCC.

Fig. 17 shows the dynamic performance of the SAPF system according to a step change in the load current. The increase in the load current disturbs the power balance between the source and the load. Therefore the real power difference is

TABLE III
COMPARISON BETWEEN ICC AND DCC

	Low Order Harmonics(%Fundamental)						
	3^{rd}	5^{th}	7^{th}	9^{th}	11^{th}	13^{th}	THD
ICC	0.03	1.91	0.96	0.6	0.74	0.46	3.03%
DCC	0.45	1.79	1.18	1.23	0.95	1.75	5.05%

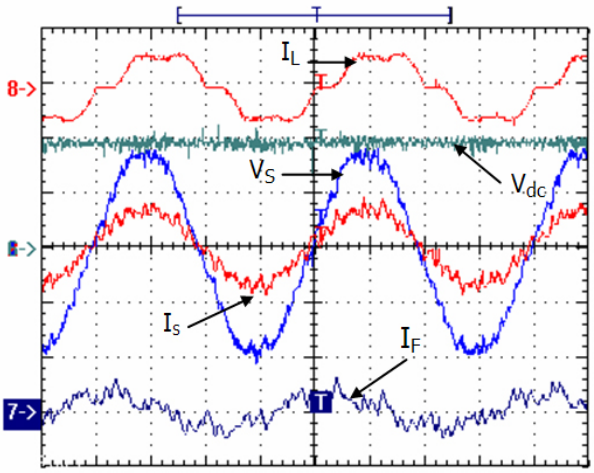

Fig. 15. SAPF performance according to DCC scheme.

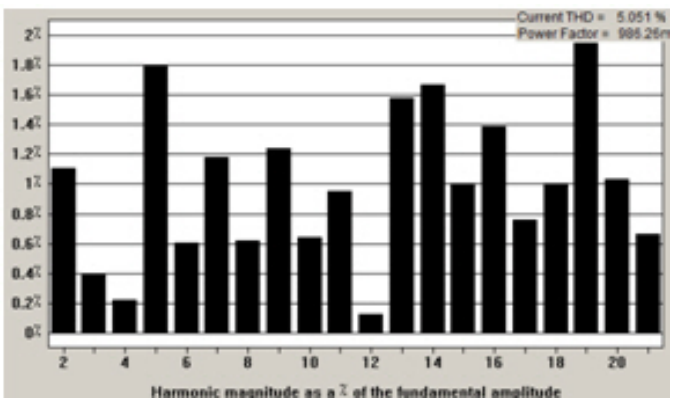

Fig. 16. Source current harmonic spectrum according to DCC scheme.

compensated by the dc-bus capacitor and the capacitor voltage is decreased from its reference level. In order to keep the dc-bus voltage constant, the mains current must increase to match the real power consumed by the load.

VII. CONCLUSION

This paper presents an improvement in the performance of a Shunt Active Power Filter based on a simplified control algorithm for the indirect current control technique.

According to the proposed scheme, sensing the source current only, instead of the load current and filter current, simplifies the computation and the circuit implementation when compared to conventional load current detection.

Experimental results using an 80C196KC microcontroller are presented to demonstrate the effectiveness and the improved performance of the proposed method in comparison to the conventional direct current control technique. The results obtained show that the THD and the low order harmonics values of the source current are significantly reduced using the ICC method over the DCC method. Furthermore, this is accomplished with greater simplification in the software and hardware implementation.

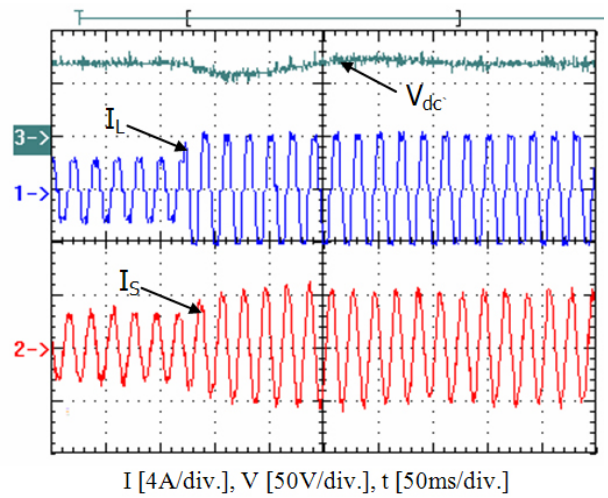

Fig. 17. Dynamic performance due to step change in the load current.

REFERENCES

[1] K. W. Louie, P. Wilson, R. A. Rivas, A. Wang, and P. Buchanan, "Discussion on power system harmonic analysis in the frequency domain," *IEEE PES Transmission and Distribution Conference and Exposition,* pp. 1-6, 2006.

[2] H. Fujita, T. amasaki, and W. Akagi, "A hybrid active filter for damping of harmonic resonance in industrial power systems," *IEEE Trans. Power Electron.*, Vol. 15, No. 2, pp. 215-222, Mar. 2000.

[3] H. Akagi, "New trends in active filters for power conditioning," *IEEE Trans. Ind. Appl.*, Vol. 32, No. 6, pp. 1312-1322, Nov./Dec. 1996.

[4] B. S. Rajpurohit and S. N. Singh, "Performance evaluation of current control algorithms used for active power filters," *EUROCON, The International Conference on 'Computer as a Tool'*, pp. 2570-2575, Sep. 2007.

[5] D. Chen and S. Xie, "Review of the control strategies applied to active power filters," *IEEE International Conference on Electric Utility Deregulation, Restructuring and Power Technologies (DRPT2004)*, pp. 666-670, 2004.

[6] W. Dai and Y. Wang, "A novel three-phase active power filter based on instantaneous reactive power theory," *IEEE Workshop on Power Electronics and Intelligent Transportation System*, pp. 375-379, 2008.

[7] A. Chandra, B. Singh, B.N. Singh, and K. Al-Haddad, "An improved control algorithm of shunt active filter for voltage regulation, harmonic elimination, power-factor correction, and balancing of nonlinear loads," IEEE Trans. *Power Electron.*, Vol. 15, No. 3, pp. 495-507, May 2000.

[8] A. Hamadi, K. Al-Haddad, P.J. Lagact, and A. Chandra, "Indirect current control techniques of Three Phase APF Using Fuzzy Logic and Proportional Integral Controller: Comparative analysis," *11th IEEE International Conference on Harmonics and Quality of Power*, pp. 362-367, 2004.

[9] Salem Rahmani, Kamal Al-Haddad, and Hadi Y. Kanaan, "Experimental design and simulation of a modified pwm with an indirect current control technique applied to a single-phase shunt active power filter," *IEEE* International Symposium on Industrial Electronics, Vol. 2, pp. 519-524, 2005.

[10] B. Singh and V. Verma, "An indirect current control of hybrid power filter for varying loads," IEEE Trans. *Power Del.*, Vol. 21, No. 1, pp. 178-184, Jan. 2006.

[11] V. Verma, B. Singh, A. Chandra, and K. Al-Haddad, "Power conditioner for variable-frequency drives in offshore oil fields," *IEEE Trans. Ind. Appl.*, Vol. 46, No. 2, Mar./Apr. 2010.

[12] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*, John Wiley & Sons, pp. 425-426, 1989.

[13] L. A. Moran, J. W. Dixon, and R. R. Wallace, "A three-phase active power filter operating with fixed switching frequency for reactive power and current harmonic compensation," *IEEE Trans. Ind. Appl.*, Vol. 42, No. 4, pp. 402-408, Aug. 1995.

[14] S. K. Jain, P. Agarwal, and H. O. Gupta, "Design simulation and experimental investigations on a shunt active power filter for harmonics and reactive power compensation," *Electric Power Components and Systems*, Vol. 31, pp.671–692, Jul. 2003.

Mohamed Adel was born in Cairo, Egypt in 1978. He received his B.S. and M.S. in Electrical Engineering from Banha University, Egypt, in 2000 and 2006, respectively, and his Ph.D. in Electrical Engineering from Cairo University, Egypt, in 2010. Since 2002, he has been with the Department of Electrical Engineering and Technology, Faculty of Engineering, Banha University, where he is currently a Lecturer. His current research interests include power quality, electrical machine drives, and power electronics.

Sherif Zaid received his B.S., M.S., and Ph.D. in Electrical Engineering from Cairo University, Egypt, in 1992, 1996, and 2001, respectively. He is currently an Instructor of power electronics in the Department of Electrical Power, Faculty of Engineering, Cairo University, Egypt. His current research interests include power electronics and drives.

Osama Mahgoub received his B.S., M.S., and Ph.D. in Electrical Engineering from Cairo University, Egypt, in 1982, 1987, and 1991, respectively. He is currently a Professor of power electronics in the Department of Electrical Power, Faculty of Engineering, Cairo University, Egypt. His current research interests include power electronics converters, motor drives, renewable energy systems, and APFs.