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Dual-Coupled Inductor High Gain DC/DC Converter with Ripple Absorption Circuit

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Abstract

High-gain DC/DC converters have become one of the key technologies for the grid-connected operation of new energy power generation, and its research provides a significant impetus for the rapid development of new energy power generation. Inspired by the transformer effect and the ripple-suppressed ability of a coupled inductor, a double-coupled inductor high gain DC/DC converter with a ripple absorption circuit is proposed in this paper. By integrating the diode-capacitor voltage multiplying unit into the quadratic Boost converter and assembling the independent inductor into the magnetic core of structure coupled inductors, the adjustable range of the voltage gain can be effectively extended and the limit on duty ratio can be avoided. In addition, the volume of the magnetic element can be reduced. Very small ripples of input current can be obtained by the ripple absorption circuit, which is composed of an auxiliary inductor and a capacitor. The leakage inductance loss can be recovered to the load in a switching period, and the switching-off voltage spikes caused by leakage inductance can be suppressed by absorption in the diode-capacitor voltage multiplying unit. On the basis of the theoretical analysis, the feasibility of the proposed converter is verified by test results obtained by simulations and an experimental prototype.

Key words: Dual-coupled inductor, High gain, Quadratic Boost converter, Ripple absorption circuit, Voltage multiplying unit

I. INTRODUCTION

High-gain and high-efficiency DC/DC converters, as a key energy conversion technology in photovoltaic power generation, fuel cell power generation and DC systems, have been widely studied since they greatly improve system conversion efficiency [1]-[3]. Traditional Boost converters and some uncomplicated step-up topologies can obtain a higher efficiency with fewer devices [4]. However, an extremely high duty cycle is unavoidable when it comes to achieving a higher gain for the Boost converter in some high gain requirement applications, and the energy conduction system loss increases due to the enlarged voltage stress of the switch devices [5]. In addition, the input and output current ripples increase for a duty cycle increasing close to the extreme high duty cycle, which results in more aggravated losses of the converter [6]. When compared to the traditional step-up DC/DC converters, high-gain DC/DC converters have the following advantages.

(1) A high voltage gain can be obtained by integrating a voltage-multiplying unit, a coupled inductor and a high step-up module without the requirement of an extreme high duty cycle, while reducing the switching loss.

(2) The voltage across switches and diodes can be clamped to the lower voltage of the capacitor voltage.

(3) Very small ripples, close to zero ripples, in the input current can be achieved by the parallel interleaving structure and the design of the coupled inductor in the converter.

(4) The voltage spike of the switch can be effectively

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reduced by designing a voltage spike absorbing circuit.

(5) Soft switching of the switching devices can be obtained with a freewheeling circuit, which improves the efficiency of the converter.

Transformer based electrical isolated converters have been widely investigated [7]-[15]. The input and output voltage of isolated high-gain DC/DC converters have no common-ground [7], [8]. A very high voltage gain can be achieved in isolated high-gain DC/DC converters by adjusting the turn ratio of the high-frequency transformer and the duty ratio [9]-[11]. However, an excessive turns ratio decreases the linearity of the high-frequency transformer, and increase the leakage inductance loss. Furthermore, the leakage inductance that causes weak coupling also triggers voltage spikes of the switch during the turn-on and turn-off periods, and increase the voltage stress on the active switch [12]. The isolated high gain DC/DC converter that introduces the structure of a lossless absorption circuit can achieve higher voltage gain and realize the soft switching of the switch during the period of load mutation [13], [14]. However, the increased leakage inductance caused by high turns ratio of the transformer is not be alleviated. It still results in added leakage inductance loss.

An isolated converter integrated with the switching capacitor unit can achieve a higher gain with a smaller turn ratio and duty ratio [15]. The leakage inductance energy can be recovered to the primary side of the converter by adding an energy recovery circuit consisting of a clamp diode and an energy storage capacitor [16]. However, the energy transfer between the two sides of the high frequency transformer is accompanied by increased ferromagnetic losses for the electromagnetic conversion process, which reduces the efficiency and power density of the converter.

In order to obtain a higher voltage gain and conversion efficiency, non-isolated high gain DC/DC converters have been studied [17]-[28]. Energy conduction and voltage lifting can be achieved through the dynamic charging and discharging period among energy storage inductors and capacitors. The non-isolated DC/DC converter by means of a coupled inductor can realize a higher voltage gain [17]-[19]. However, leakage inductance of the coupled inductor is inevitable [20], [21]. A clamping circuit consisting of energy storage capacitors and diodes is designed to suppress the voltage spikes of active switches caused by leakage inductance, and an added energy recovery circuit is integrated to reduce the leakage inductance loss [22]-[24]. A coupled inductor non-isolated high gain converter integrating the diode-capacitor voltage multiplying unit can effectively widen the adjustable range of the gain, and it naturally forms a passive clamp circuit and a leakage inductance energy recovery circuit [25]-[27]. The voltage spike in a switch caused by the leakage inductance can be effectively suppressed and the leakage inductance loss can be recovered to the load side, which improves the efficiency of the converter [28].

The Input Current Ripple (ICR) in high frequency switching converters is one of the reasons for the high current peak of a switching device and the low efficiency of converters. There has been a lot of effort to solve the above-mentioned problems in power electronics converters [29]-[36]. One common method of ripple-suppression is to adopt a dual or multi-phase converter operated with interleaving control [29]. However, the interleaving control can lead to high cost and control complexities since multi-phase converters are necessary and operated in synchronization [30,31]. A Boost-based high gain converter can reduce the ICR by adjusting the value of the input inductor [32]. However, the dynamic response speed decreases when the filter inductor increases. In addition, this method increases the hardware size of converters. The converter proposed in [33] can decrease the ICR by properly configuring the duty cycle. However, the voltage gain and ICR are simultaneously controlled by the duty cycle, which limits the adjustable range of the gain. The method of ripple-suppression in [34] is the design of a resonant ripple absorption circuit. However, an additional absorption circuit is necessary to alleviate voltage spikes in the switch. The Boost-Sepic converter in [35] can obtain small input current ripples by integrating the input inductor and the intermediate inductor into a magnetic core and properly configuring the coupling coefficient. Nevertheless, the coupling strength of the coupled inductors can be adjusted with high precision [25].

Inspired by the transformer effect and the ripple-suppressed capability of coupled inductors, a double-coupled inductor high gain DC/DC converter with a ripple absorption circuit is proposed in this paper. The proposed converter has a diode-capacitor voltage multiplying unit integrated into a Quadratic Boost Converter (QBC) and independent inductors assembled into one magnetic core to structure the coupled inductors, which can reduce the size of the magnetic components. This converter can effectively expand the adjustable range of the voltage gain without an extreme duty cycle. Very small ripples, close to zero input current ripple, can be obtained by the ripple absorption circuit composed of an auxiliary inductor and a capacitor. In addition, the current of the absorption branch is low, the loss can be negligible, and the volume of the absorption branch is tiny. The leakage inductance loss in one switching period can be recovered to the load through the diode-capacitor voltage multiplying unit, and the voltage spikes of switches due to leakage inductance can be suppressed by an absorption circuit composed of a clamping diode and a storage capacitor. Based on the PSIM simulation platform and a hardware platform, an experimental prototype with an input voltage/output voltage of 18V/400V and a rated power of 200W is constructed to verify feasibility of the proposed converter through simulation and experimental results.

II. Working Principle of the Converter

A diode-capacitor voltage multiplying unit and an input

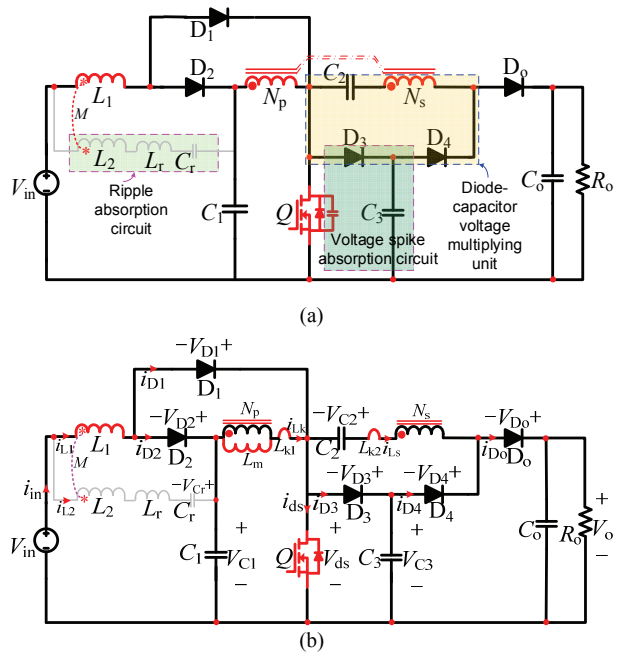

Fig. 1. High gain DC/DC converter with a ripple absorption circuit. (a) Circuit topology. (b) Topological equivalent circuit.

current ripple absorption circuit are integrated into a QBC to obtain the circuit topology of a converter shown in Fig. 1(a). The main working circuit includes a DC input power supply V_{in}, an active power switch tube Q, five diodes D_1-D_5, three storage capacitors C_1-C_3, one output filter capacitor, two pairs of coupled inductors T_1-T_2, and one weak voltage and current ripple absorption circuit. The voltage multiplying unit (composed of diodes D_3 and D_4), the storage capacitor C_2 and the secondary side of the coupled inductor T_2 can be used to increase the voltage gain of the converter. The ripple absorption circuit is composed of the auxiliary inductor L_r, the auxiliary capacitor C_r and the secondary side of the coupled inductor T_1. The input inductor L_1 and the inductor L_2 are assembled into one magnetic core to structure a coupled inductor that can reduce the amplitude of the input current ripple to a low level. The peak absorption circuit is composed of the parasitic capacitance of the switch Q, the clamping diode D_3 and the capacitor C_3. The maximum voltage across the switch Q is clamped to the voltage of the capacitor C_3. Fig. 1(b) shows a topology equivalent circuit of the converter. The coupled inductor T_1 is a fully coupled inductor, where the turns ratio can be expressed as $N_1(N_1=(L_1/L_2)^{1/2})$. The mutual inductance of T_1 can be expressed as M. The coupled inductor T_2 can be equivalent to a high-frequency transformer with a turns ratio of $N_2(N_2=N_s/N_p)$. In addition, the magnetizing inductance is L_m, and the leakage inductance of the primary and secondary sides are L_{k1} and L_{k2}, respectively. In order to simplify the circuit analysis and ignore the interference on the converter characteristics caused by the device parameters, the following assumptions should be made.

1) All of the capacitors in the circuit are large enough so that the voltage ripples across both terminals can be ignored, and the voltage across all of the capacitors is constant in a switching period.

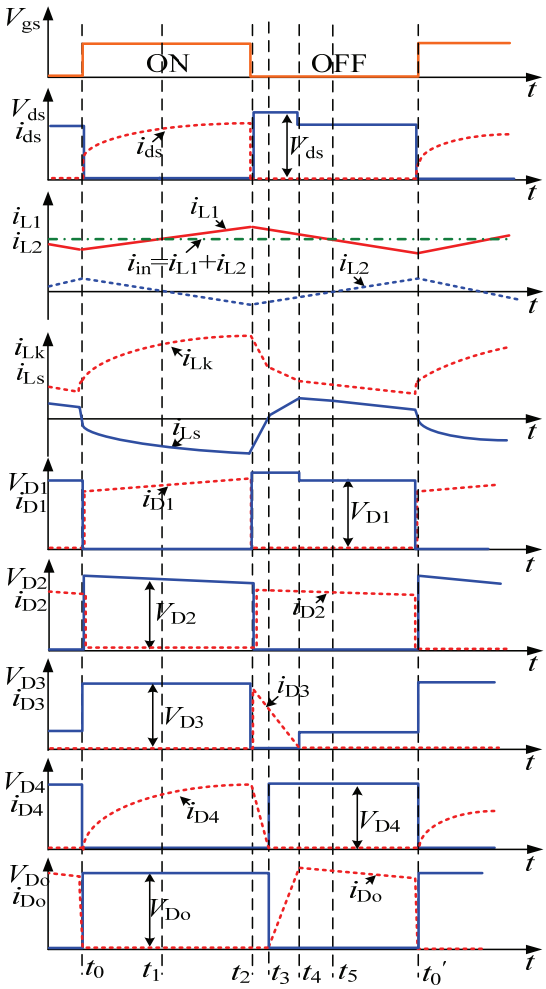

Fig. 2. Working principle waveforms of the converter in a switching period.

2) Except for containing the anti-parallel diode and capacitors, the switch tube and diodes are ideal devices without switching losses.

3) The coupled inductor T_2 is a high-frequency transformer considering the magnetizing inductance and leakage inductance, and its coupling coefficient is $k_2=L_m/(L_{k1}+L_m)$.

According to the above assumptions and the on-off states of the switch, the diode and the energy storage device, a converter operating in the continuous conduction mode (CCM) of the inductor current can be divided into six operating modes in a switching period. Modal equivalent circuits of the converter are shown in Fig. 3. Fig. 2 shows waveforms of the inductor current, the voltage and the current of the switching devices during a switching period. The modal switching process is as follows.

1) Mode 1[$t_0<t<t_1$, as shown in Fig. 3(a)]: At time t_0, the switch Q and the diodes D_1 and D_4 are turned on, and the diodes D_2, D_3 and D_o are turned off and supported by the

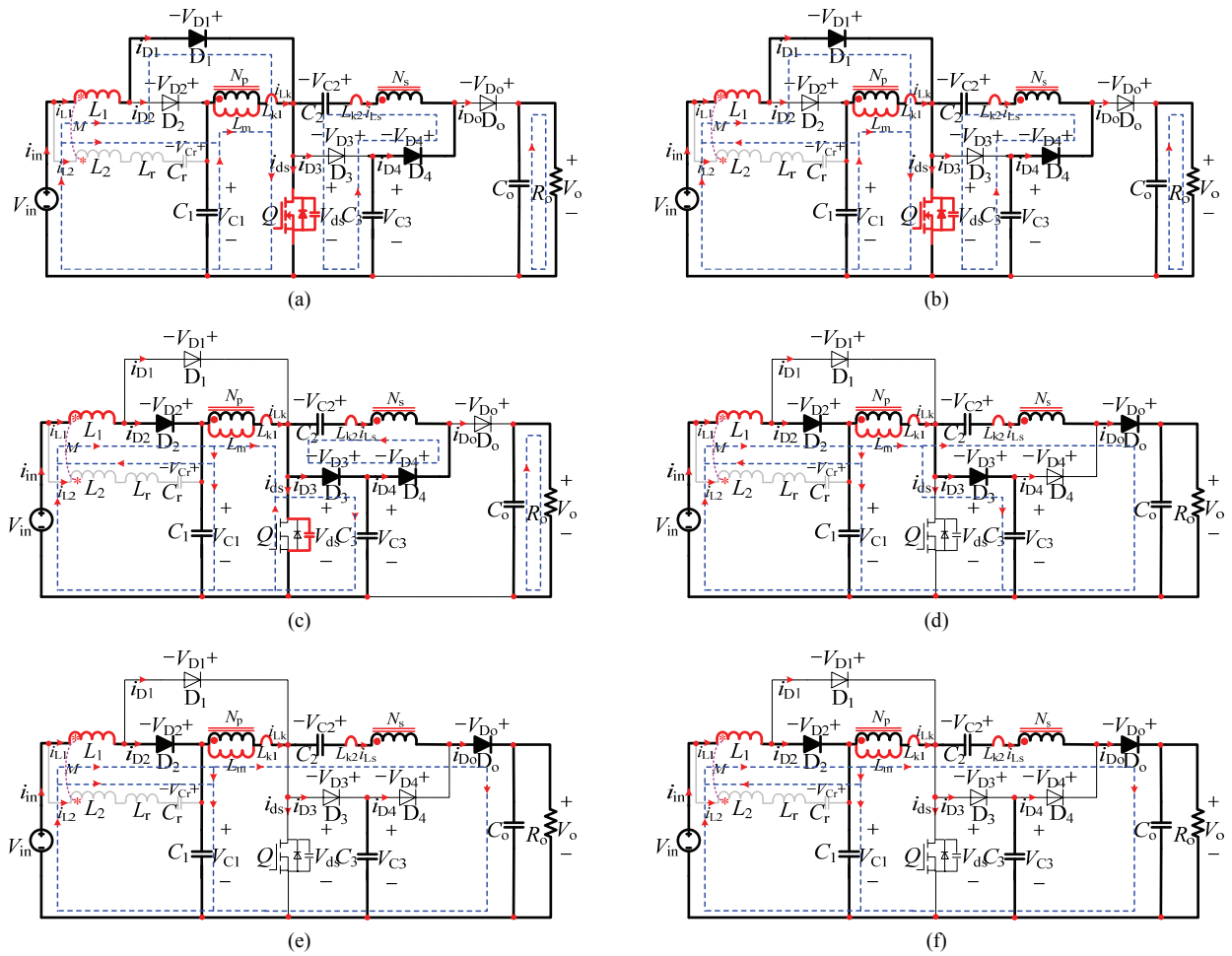

Fig. 3. Equivalent circuits of the proposed converter. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

reverse voltages V_{C1}, V_{C3} and V_o, respectively. The energy from the DC source V_{in} is delivered to the primary side winding L_1 through D_1 and Q, and the current i_{L1} is linearly enlarged. In this mode, i_{L1} is smaller than the effective value of the input current, and the secondary side of T_1 and the auxiliary inductor L_r are charged by the auxiliary capacitor. Meanwhile, the secondary side current i_{L2} of T_1, which is greater than zero, is opposite to the variation tendency of i_{L1}. As a result, the input current ripple is reduced. The energy storage in the capacitor C_1 is released to the primary side of T_2 through Q, and the current i_{Lk} rises linearly. The energy stored in the secondary side of T_2 is transferred to the capacitor C_2 by using the transformer effect, and the current i_{Ls} rises in the opposite direction.

$$i_{in} = i_{L1} + i_{L2} \tag{1}$$

$$L_1 \frac{di_{L1}}{dt} + M \frac{di_{L2}}{dt} = V_{in} \tag{2}$$

$$M \frac{di_{L1}}{dt} + (L_2 + L_r) \frac{di_{L2}}{dt} = V_{in} + V_{Cr} - V_{C1} \tag{3}$$

$$V_{Lm} = k_2 V_{C1} \tag{4}$$

$$V_{Ns} = V_{C2} - V_{C3} \tag{5}$$

2) Mode 2[t_1<t<t_2, as shown in Fig. 3(b)]: In this mode, the switch Q and the diodes D_1 and D_4 continue to conduct, and the diodes D_2, D_3 and D_o are turned off. The energy from the DC source Vin is released to the primary side of T_1 via D_1 and Q, C_1 is discharged to the primary side of T_1 through Q, and i_{L1} and i_{Lk} continue to rise. The secondary side of T_2 and the capacitor C_3 are discharged to C_2, and the current -i_{Ls} rises. i_{L1} is greater than the effective value of the input current. In addition, the current i_{L2} is opposite to i_{L1} and its amplitude is less than zero. Therefore, the input current ripple is reduced by the sum of the ripples of the currents i_{L1} and i_{L1}.

3) Mode 3[t_2<t<t_3, as shown in Fig. 3(c)]: In this mode, the switch Q and the diode D_1 are turned off, and the diode D_2 is continuously turned on. At t_2, D_3 with support from the forward voltage is conducted and forms a discharge circuit with the parasitic capacitors of Q and C_3. The voltage across Q is clamped to the voltage of C_3. The current path of i_{Lk} is rapidly switched from the switch Q to C_3. In addition, i_{Lk} declines rapidly. The leakage energy in both sides of T_2 is stored in C_2 via D_4, and the current -i_{Ls} decreases linearly.

$$V_{ds} = V_{C3} \tag{6}$$

$$\frac{di_{Lm}}{dt} = \frac{k_2(V_{C1} - V_{C3})}{L_m} \tag{7}$$

4) Mode 4[t_3<t<t_4, as shown in Fig. 3(d)]: In this mode, the switch Q and the diode D_1 remain turned off, and the diode D_2 is conducted. At t_3, the leakage inductance energy in both sides of T_2 is completely discharged. In addition, the diode D_4 is turned off, and output diode D_o is conducted. The energy from the primary side of T_1 and V_{in} is transferred to C_1 via D_2. In addition, i_{L1} decreases linearly. The energy stored in the primary side of T_2 is released to C_3 through D_3, and discharged to the output side through D_o with the secondary side of T_2 and C_2. In addition, i_{Lk} decreases linearly, and the current i_{Ls} rises linearly. The current i_{L1} is greater than the effective value of the input current, and C_r is charged by the secondary side of T_1 and the auxiliary inductor L_r. In addition, i_{L2} rises linearly and its amplitude is less than zero.

$$L_1 \frac{di_{L1}}{dt} + M \frac{di_{L2}}{dt} = V_{in} - V_{C1} \tag{8}$$

$$M \frac{di_{L1}}{dt} + (L_2 + L_r) \frac{di_{L2}}{dt} = V_{C1} - V_{in} - V_{Cr} \tag{9}$$

$$V_{Lm} = k_2(V_{C1} - V_{C3}) \tag{10}$$

$$V_{Ns} = V_{C2} + V_{C3} - V_o \tag{11}$$

5) Mode 5[t_4<t<t_5, as shown in Fig. 3(e)]: At t_4, the storage capacitor C_3 is completely charged and the diode D_3 is turned off. In this period, Q and D_1 are turned off, and D_2 and D_o are conducted. The energy in the primary side of T_1 is discharged to C_1 through D_2, and i_{L1} maintains a downward trend. C_r is charged by the secondary side of T_1 and L_r, and the current -i_{L2} continues to decrease. The energy stored in the secondary side winding of T_2 and C_2 is released to the output load via D_o. In addition, the current i_{Lk} starts to rise, and the current i_{Ls} begins to decline.

6) Mode 6[t_5<t<t_0′, as shown in Fig. 3(f)]: At t_5, the current i_{L1} is equal to the effective value of the input current and -i_{L2} drops to zero. In this mode, the primary side of T_1 continues to discharge, and i_{L1} declines lower than i_{in}. Meanwhile, the capacitance energy stored in C_r is discharged to the secondary side of T_1 and L_r, and i_{L2} begins to increase. The energy stored in the secondary side winding of T_2 and C_2 is sequentially released to the output load via D_o, and the current i_{Lk} continues to increase. Until time t_0′, when switch is turned back on, the converter starts the next switching period.

III. Steady State Analysis

A. Voltage Gain

In order to reduce the volume of the magnetic component, the coupling inductor T_1, the auxiliary inductor L_r and the auxiliary capacitor C_r are combined to form a ripple absorption circuit, which can reduce the ICR with the ripple suppression capability of the coupled inductor. T_1 can be configured as a fully coupled inductor, and its coupling coefficient can be expressed as:

$$k_1 = \frac{M}{\sqrt{L_1 L_2}} \tag{12}$$

During the two periods of the switch turn-on and turn-off, the voltage across the inductor can be approximately constant. In order to simplify the analysis process with the above mode analysis, the inductor voltage in modes 1 and 4 are used to represent the inductor voltage during the two periods of the switch turn-on and turn-off, respectively.

In a switching period T_s, by using the volt-second balance law in two sides of T_1 and the magnetizing inductance L_m of T_2, the voltage of C_1, C_2, C_3 and C_r can be obtained by arranging equations (2) - (5) and (8) - (11):

$$V_{C1} = \frac{V_{in}}{1 - D} \tag{13}$$

$$V_{Cr} = \frac{DV_{in}}{1 - D} \tag{14}$$

$$V_{C2} = (1 - D)V_o - (1 - 2D)V_{C3} \tag{15}$$

$$V_{C3} = \frac{V_{C1}}{1 - D} \tag{16}$$

Based on (10) - (11), the output voltage of the proposed converter can be expressed by:

$$\begin{aligned} V_o &= V_{C2} + (1 + k_2 N_2)V_{C3} - k_2 N_2 V_{C1} \\ &= \frac{2 + k_2 N_2}{(1 - D)} V_{in} \end{aligned} \tag{17}$$

Therefore, the steady-state voltage gain of the converter can be obtained when the converter operates in the CCM:

$$G(D, N_2, k_2)_{CCM} = \frac{V_o}{V_{in}} = \frac{2 + k_2 N_2}{(1 - D)^2} \tag{18}$$

Fig. 4 shows gain contrast curves of the converter under different coupling coefficients. It is shown that the leakage inductance and the coupling inductance T_1 have no effect on the voltage gain of the converter. However, the gain loss of the converter due to the leakage inductance of T_2 cannot be ignored. Therefore, the design of coupling inductor T_2 should ensure that the winding is compact and minimize the air gap between magnetic cores for to reduce the gain loss caused by the leakage inductance. When the gain loss caused by the leakage inductance in T_2 is ignored (k_2=1), the voltage gain of the converter can be expressed as:

$$G(D, N_2)_{CCM} = \frac{2 + N_2}{(1 - D)^2} \tag{19}$$

It can be obtained from equation (19) that the voltage gain of the converter is simultaneously controlled by the duty ratio D and the turns ratio N_2 of T_2 without considering the influence of the leakage inductance T_2 on the gain. In other words, increases of the duty cycle D and the turns ratio N_2 can enlarge the voltage gain of the converter. In high gain requirement applications, the gain of the converter can be

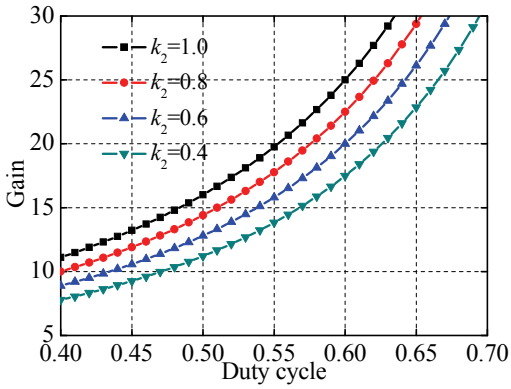

Fig. 4. Gain comparison curve under different coupling coefficients k_2.

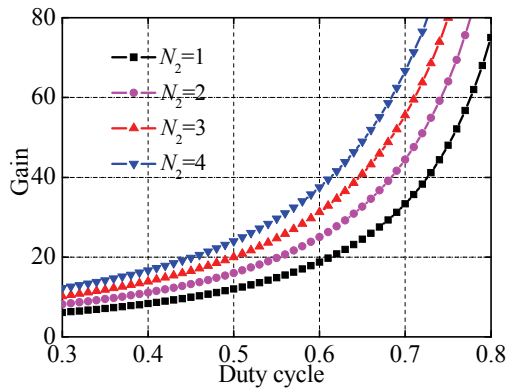

Fig. 5. Gain comparison curves with different turns ratios N2 and duty cycles.

further improved by increasing the turn ratio N_2 without an extremely high duty cycle.

B. Voltage Stress Analysis

According to the above analysis of the operation mode and steady-state gain, the voltage stress of the switching devices including the switch Q and the diodes D_1-D_o can be derived from (13)-(16). Ignoring the influence of the voltage ripple on the capacitor C_3 and the leakage inductance of the coupled inductors, the voltage stress of the switch Q can be obtained from modes 3 and 4. The parameter measurement for the armature inductance L_1 is also executed in a wide frequency range from 40Hz to 100Hz under various V/f ratios. The armature inductance is calculated by using the center of the P-Q circle diagram depicted for each driving frequency.

$$V_{ds} = V_{C3} = \frac{V_{in}}{(1-D)^2} = \frac{V_o}{2+N_2} \tag{20}$$

According to mode 1 and mode 3, the voltage stresses of diodes D_1, D_2 and D_3 are (V_{C3}-V_{C1}), V_{C1} and V_{C3}, respectively. From mode 2 and mode 4, the voltage stresses of the diode D_4 and the output diode D_o are equal to (V_o-V_{C3}). Therefore, the voltage stress expressions of D_1 and D_o can be expressed as:

$$V_{D1} = V_{C3} - V_{C1} = \frac{DV_{in}}{(1-D)^2} = \frac{DV_o}{2+N_2} \tag{21}$$

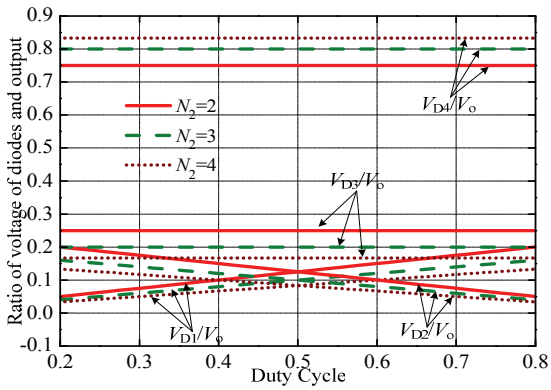

Fig. 6. Ratio of the diode voltage to the output voltage under different turns ratios and duty cycles.

$$V_{D2} = V_{C1} = \frac{V_{in}}{1-D} = \frac{(1-D)V_o}{2+N_2} \tag{22}$$

$$V_{D3} = V_{C3} = \frac{V_{in}}{(1-D)^2} = \frac{V_o}{2+N_2} \tag{23}$$

$$V_{D4} = V_{Do} = V_o - V_{C3} = \frac{(1+N_2)V_o}{2+N_2} \tag{24}$$

Fig. 6 shows variation curves of the ratio of the voltage on the diode and the output under different turn ratios and duty cycles. It is noticeable that the voltage stress of the diode D_1 is proportional to the duty cycle D and inversely proportional to the turn ratio N_2. The voltage across the diode D_2 is inversely proportional to D and N_2. When the voltage spikes of the switching tube are ignored, the voltage stress of the diode D_3 is equal to the voltage across the switching tube, and the ratio V_{D3}/V_o is independent of D and proportional to N_2. The voltages across the diodes D_4 and D_o are equal, and the ratio V_{D4}/V_o is independent from D and rises with an increase of N_2. Therefore, when the input voltage and output voltage are constant, the duty cycle and the turn ratio N_2 should be reasonably allocated to effectively reduce the voltage stress of the switching devices and to improve the efficiency of the converter.

C. Current Stress Analysis

In order to simplify the current stress analysis of switching devices, the simplified current stress diagram shown in Fig. 7 can be obtained by neglecting the leakage inductance influence. According to equations (2) and (3), the current ripple of the inductors L_1 and L_2 can be expressed as:

$$\Delta i_{L1} = \frac{(L_2+L_r)V_{in} - M(V_{in}+V_{Cr}-V_{C1})}{L_1(L_2+L_r)-M^2} DT_s \tag{25}$$

$$\Delta i_{L2} = \left| \frac{L_1(V_{in}+V_{Cr}-V_{C1}) - MV_{in}}{L_1(L_2+L_r)-M^2} DT_s \right| \tag{26}$$

According to operating modes 1 and 2, the input current is equal to the sum of the current flowing through L_1 and L_2. In order to make the ICR as small as possible, it is necessary to properly configure the current ripple of L_2. When the absolute

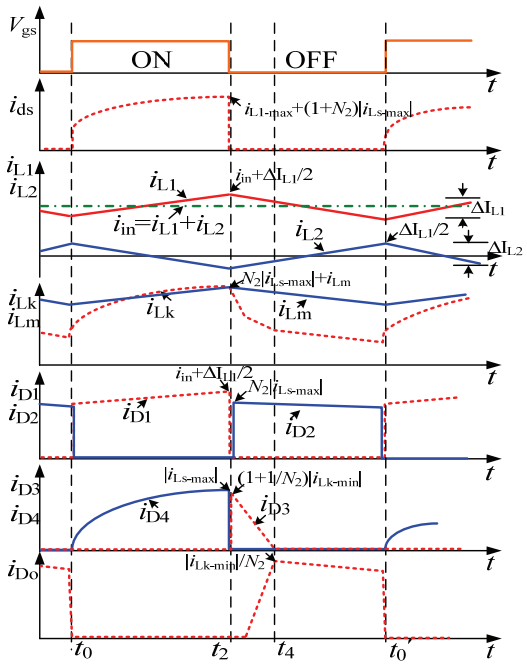

Fig. 7. Device current stress simplified diagram.

value of the current ripple Δi_{L2} is equal to the current ripple Δi_{L1} in same time and the variation tendency is opposite, very small input current ripples that are close to zero can be achieved. Therefore, the current stress of L_1 and L_2 are obtained as:

$$i_{\text{L1-max}} = i_{in} + \frac{\Delta i_{\text{L1}}}{2} = \frac{2+N_2}{(1-D)^2} I_{\text{o}} + \frac{\Delta i_{\text{L1}}}{2} \tag{27}$$

$$i_{\text{L2-max}} = \frac{\Delta i_{\text{L1}}}{2} \tag{28}$$

By using the ampere-second balance law in the capacitor C_1, the average current flowing through the primary winding of T_2 is zero in a switching period. The current i_{Lk} is equal to the superposition of the current flowing through the secondary winding and the magnetizing inductor current of T_2. Thus, the following can be obtained:

$$i_{\text{Lm-max}} = i_{\text{Lk-max}} = \frac{(2+N_2)I_{\text{o}}}{(1-D)^2} + \frac{V_{\text{C1}}D}{2L_{\text{m}}f_{\text{s}}} \tag{29}$$

$$i_{\text{Lm-min}} = \frac{(2+N_2)I_{\text{o}}}{(1-D)^2} - \frac{V_{\text{C1}}D}{2L_{\text{m}}f_{\text{s}}} \tag{30}$$

From the current flowing path of the diodes and the current stress of all the inductors, the current stress of D_1 and D_2 can be expressed as follows:

$$i_{\text{D1-stress}} = i_{\text{L1-max}} = \frac{2+N_2}{(1-D)^2} I_{\text{o}} + \frac{\Delta i_{\text{L1}}}{2} \tag{31}$$

$$i_{\text{D2-stress}} = i_{\text{L1-max}} = \frac{2+N_2}{(1-D)^2} I_{\text{o}} + \frac{\Delta i_{\text{L1}}}{2} \tag{32}$$

According to mode 2 and mode 4, the current flowing through the diodes D_3, D_4 and D_{o} varies with the change of the current flowing through the secondary winding of T_2. Therefore, the current stresses of D_3, D_4 and D_{o} are obtained as follows:

$$\begin{aligned} i_{\text{D3-stress}} &= i_{\text{Lk}} + \frac{1}{N_2}(i_{\text{Lk}} - i_{\text{Lm}}) \\ &= \frac{(N_2+1)(2+N_2)I_{\text{o}}}{N_2(1-D)^2} - \frac{V_{\text{C1}}D}{2N_2L_{\text{m}}f_{\text{s}}} \end{aligned} \tag{33}$$

$$i_{\text{D4-stress}} = |\, i_{\text{Ls-max}} \,| = \frac{(2+N_2)I_{\text{o}}}{N_2(1-D)^2} - \frac{V_{\text{C1}}D}{2N_2L_{\text{m}}f_{\text{s}}} \tag{34}$$

$$i_{\text{Do-stress}} = |\, i_{\text{Ls-max}} \,| = \frac{(2+N_2)I_{\text{o}}}{N_2(1-D)^2} - \frac{V_{\text{C1}}D}{2N_2L_{\text{m}}f_{\text{s}}} \tag{35}$$

As shown in Fig. 7, the current stress of the switch is equal to the current of the switch at time t_2. At this time, the charging process of L_1 and the magnetizing inductance of T_2 is completed. Therefore, the current stress of the switch can be written as follows:

$$\begin{aligned} i_{\text{ds-stress}} &= i_{\text{L1-max}} + (1+\frac{1}{N_2}) i_{\text{Lk-max}} \\ &= (2+\frac{1}{N_2})\frac{(2+N_2)I_{\text{o}}}{(1-D)^2} + \frac{\Delta i_{\text{L1}} + \Delta i_{\text{Lm}}}{2} \end{aligned} \tag{36}$$

D. Realization Conditions for Zero Ripple of the Input Current

Very small ripples of the input current can be achieved due to the ripple-suppressed capabilities of the coupled inductor. According to the above current stress analysis of L_1 and L_2, very small input current ripples that are close to zero can be obtained when the absolute value of the current ripple Δi_{L2} is equal to the current ripple Δi_{L1} in same time and the variation tendency is opposite. Hence, the detailed derivation process of the realization condition for zero ripple of the input current is expressed as follows.

As can be seen from Fig. 7 and from equations (25)-(26), the following can be obtained:

$$\begin{aligned} &\Delta I_{\text{L1}} = \Delta I_{\text{L2}} \\ &\Rightarrow \frac{(L_2+L_{\text{r}})V_{\text{in}} - M(V_{\text{in}} + V_{\text{Cr}} - V_{\text{C1}})}{L_1(L_2+L_{\text{r}}) - M^2} DT_{\text{s}} \\ &= |\, \frac{L_1(V_{\text{in}} + V_{\text{Cr}} - V_{\text{C1}}) - MV_{\text{in}}}{L_1(L_2+L_{\text{r}}) - M^2} DT_{\text{s}} \,| \\ &\Rightarrow (L_2+L_{\text{r}})V_{\text{in}} - M(V_{\text{in}} + V_{\text{Cr}} - V_{\text{C1}}) \\ &= |L_1(V_{\text{in}} + V_{\text{Cr}} - V_{\text{C1}}) - MV_{\text{in}}| \end{aligned} \tag{37}$$

Without considering the influence of capacitor voltage ripples, substituting equations (13) - (14) into equation (37) yields:

$$M = L_2 + L_{\text{r}} \tag{38}$$

Assume the coupling coefficient k_1 of the coupled inductor T_1 is 1, that is $M=(L_1L_2)^{1/2}$, the condition can be obtained by equation (38) as follows:

$$N_1 = \sqrt{L_1 / L_2} = \sqrt{L_1 L_2 / L_2^2} = \frac{L_2 + L_{\text{r}}}{L_2} > 1 \tag{39}$$

Therefore, by using a ripple absorption circuit composed of a coupled inductor T_1, an auxiliary inductor L_{r} and an auxiliary

TABLE I
COMPARATIVE ANALYSIS OF CHARACTERISTICS

Converters	[2]	[3]	[4]	[5]	[6]	Proposed converter
Number of switch	1	2	2	1	2	1
Number of diode	5	4	4	6	4	5
Number of capacitor	4	5	5	5	3	5
Voltage gain in CCM	$\frac{(2+D)N+3}{1-D}$	$\frac{1+2N}{1-D}$	$\frac{2(1+N)}{1-D}$	$\frac{N(2+3D)+2-D}{2(1-D)^2}$	$\frac{2+N_2}{1-D}$	$\frac{2+N_2}{(1-D)^2}$
Voltage stress on switch	$\frac{V_o}{N(2+D)+3}$	$\frac{V_o}{1+2N}$	$\frac{V_o}{2(1+N)}$	$\frac{2+D(N-1)}{N(3D+2)+2-D}V_o$	$\frac{V_o}{2+N_2}$	$\frac{V_o}{2+N_2}$
Maximum voltage stress on diodes	$\frac{(N+1)V_o}{N(2+D)+3}$	$\frac{NV_o}{1+2N}$	$\frac{V_o}{2}$	$\frac{2N}{N(3D+2)+2-D}V_o$	V_o	$\frac{(1+N_2)V_o}{2+N_2}$
Leakage inductance loss	Small	Small	Small	Small	Medium	Small
Input current ripples	Large	Large	Large	Medium	Small	Very small
Maximum efficiency	95.38%	96.46%	96.15%	93.14%	97.32%	94.83%

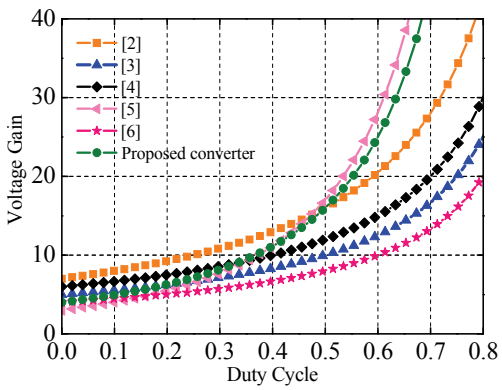

Fig. 8. Voltage gain comparison with N_2=2.

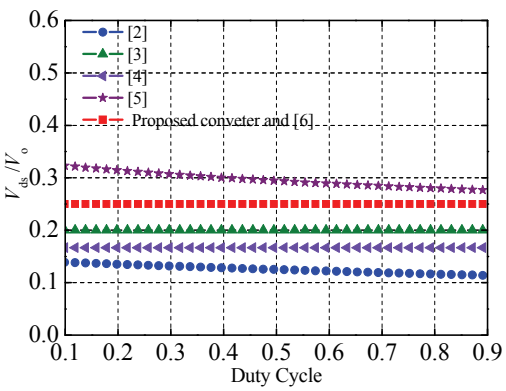

Fig. 9. Ratios between the diode voltage and the output voltage.

capacitor C_r, very small ripples of the input current can be achieved by reasonably configuring the turn ratio of the primary and secondary inductors T_1 and the value of auxiliary inductor L_r to satisfy equations (37)-(38).

IV. CONVERTER CHARACTERISTICS COMPARISON

In this paper, a number of DC/DC converters with high gains and low switching voltage stresses are selected for a comparative analysis with the proposed converter. Table I gives a comparative analysis of the main performances and experimental results among the converters, including the number of devices, voltage gain, voltage stress of switch, maximum voltage stress of diode, leakage loss, input current ripple and maximum efficiency. Fig. 8 shows a gain comparison among some homothetic converters. Fig. 9 shows a voltage stress comparison of the switching tube when the turns ratios are equal. In addition to a high voltage gain and a low voltage stress, the converter proposed in this paper can achieve zero ripple of the input current.

V. PARAMETER DESIGN

In order to verify the steady-state characteristics of the converter and the feasibility of the theoretical analysis, an experimental prototype is designed in this paper. The parameters of the experimental prototype are designed as follows.

1) Input voltage range V_{in}= 18V-36V.
2) Output voltage V_o= 400V.
3) Rated output power P_o= 200W.
4) Switching frequency f_s= 40kHz.

A. Selection of the Duty Cycle and Turn Ratio N_2

According to equation (18) and considering the gain loss due to the leakage inductance of the coupled inductor, the voltage gain can step up in order meet the requirement of the experimental prototype when the input voltage is 18V, the value of N_2 is 3, and the duty ratio is 0.54.

B. Selection of the Inductors L_1, L_2, L_r and Turn Ratio N_2

According to the above analysis of the input current ripples, the inductor L_1 should be large enough to ensure that its minimum current is greater than zero. The primary side equivalent inductance of the coupled inductor T_1 is larger than the value of L_1 when an independent inductance is used. In order to obtain a continuous inductor current, L_1 should be

selected as follows:

$$L_1 > \frac{V_{in}D}{2i_{in}f_s} = \frac{18\times 0.54}{2\times\frac{100}{18}\times 40\times 10^3} = 21.87\mu H \quad (40)$$

Therefore, the primary inductance value of T_1 is 240μH. According to equation (39), it is necessary to satisfy N_1>1 to achieve zero ripple of the input current. Therefore, N_1 can be set to 2. Assuming the coupled inductor is a fully coupled inductor, the value of the secondary side L_2 of T_1 can be obtained as follows:

$$L_2 = \frac{L_1}{N_1^2} = \frac{240}{4} = 60\mu H \quad (41)$$

Since the leakage inductance of the coupled inductor cannot be ignored, it can be obtained according to equation (38) as follows:

$$L_r < \sqrt{L_1 L_2} - L_2 = 60\mu H \quad (42)$$

Therefore, the auxiliary inductance L_r is selected to be 58μH.

C. Selection of the Magnetizing Inductance L_m

To operate the converter in the CCM mode of the inductor current, the minimum value of the magnetizing inductor current i_{Lm} needs to be greater than zero. According to formula (30), L_m needs to satisfy the following relational expression:

$$L_m > \frac{V_{C1}D}{2\times\frac{(2+N_2)I_o}{(1-D)^2}\times f_s} = \frac{39.13\times 0.54}{2\times 5.9\times 40\times 10^3} = 44.76\mu H \quad (43)$$

Therefore, L_m can selected to be 200μH, which can ensure that the inductance current operates in the CCM without increasing the number of turns of T_2 and reducing the volume of the magnetic components.

D. Selection of the Switch and the Diode

The rated voltage of the switching devices can be obtained based on (20)-(24) and (31)-(36). In practice, voltage spikes can be triggered during the switching transition process. Hence, FQP34N20 (200V, 31A, 0.075Ω) can be used for the switch, Schottky diodes MBR20200 (200V, 20A) can be used for the diodes D_1 and D_2, and fast recovery diodes SFF1606G (400V) can be used for the diodes D_3, D_4 and D_o.

E. Selection of the Capacitor

The rated voltage of the capacitors can be obtained from (13)-(16). The selected capacitor capacity needs to be greater than 1.5 times the theoretical value to reduce voltage ripples. In addition, the values of the capacitors are supposed to satisfy the following condition:

$$C > \frac{P_o}{V_o \Delta V_C f_s} \quad (44)$$

Therefore:

$$C_1 > \frac{200}{400\times 0.5\%\times V_{C1}\times 40\times 10^3} = 63.88\mu F \quad (45)$$

$$C_r > \frac{200}{400\times 2\%\times V_{Cr}\times 40\times 10^3} = 29.58\mu F \quad (46)$$

$$C_2 > \frac{200}{400\times 0.5\%\times V_{C2}\times 40\times 10^3} = 12.76\mu F \quad (47)$$

$$C_3 > \frac{200}{400\times 0.5\%\times V_{C3}\times 40\times 10^3} = 29.38\mu F \quad (48)$$

$$C_o > \frac{200}{400\times 0.05\%\times V_o\times 40\times 10^3} = 62.50\mu F \quad (49)$$

The capacitor C_1, as the equivalent excitation power of T_1 should maintain stability. Therefore, its parameters can be selected as 100μF and 100V. In order to reduce the output voltage ripple, the output capacitor C_o is selected to be an electrolytic capacitor with parameters of 470μF/450V, the auxiliary capacitor is selected with parameters of 22μF/ 50V, and C_2 and C_3 are selected with parameters of 47μF/ 250V.

VI. Simulation Results

Fig. 10 shows waveforms of simulation results under the same parameters as the experimental prototype, including the voltage and current waveforms of the switch, and the current waveform of the diodes and inductors. It can be observed from the results that the input current ripple is approximately zero. When the input voltage and output voltage are 18V/400V, the turns ratio N_2 is 3 and the duty ratio is 0.54, the switching tube voltage stress is about 80V. The simulation results are basically consistent with the principle analysis.

VII. Experimental Results

An experimental prototype has been constructed to verify the feasibilities of the proposed converter by using the design parameters in this paper. Sampled waveforms are presented in Fig. 11(a) including waveforms of the driving pulse, and current waveforms of the input and the two sides of T_1. The ripple absorption circuit, composed of a coupled inductor T_1, an auxiliary inductor L_r and an auxiliary capacitor, can reduce the input current ripple. This can be seen from the fact that the current variation tendency of the two sides of T_1 is opposite. By adjusting the auxiliary inductance, the peak-to-peak value of the input current ripples can be reduced to lower than 5%.

Fig. 11(b) illustrates the gate signal of Q and the current waveform of T_2. Figs. 11(c) and 11(d) show current waveforms of all the diodes and the switch tube. Obviously, when the switch is turned off, the primary current of T_2 decreases, and the diodes D_3 and D_4 are conducted. In

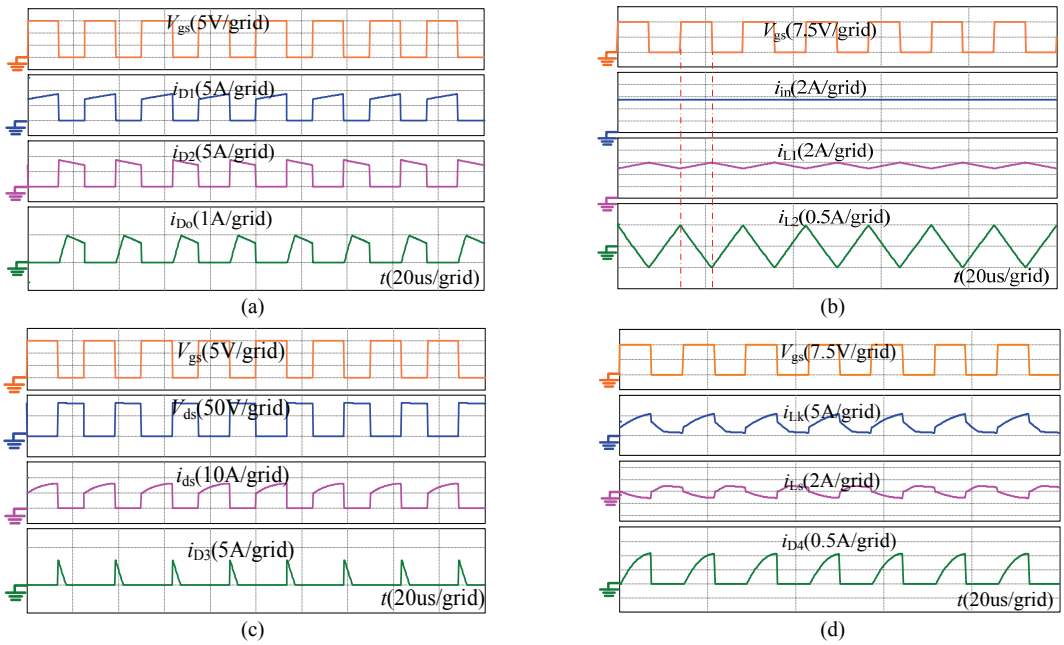

Fig. 10. Simulation test waveforms. (a) V_{gs}, i_{D1}, i_{D2} and i_{Do}. (b) V_{gs}, i_{in}, i_{L1} and i_{L2}. (c) V_{gs}, V_{ds}, i_{ds} and i_{D3}. (d) V_{gs}, i_{Lk}, i_{Ls} and i_{D4}.

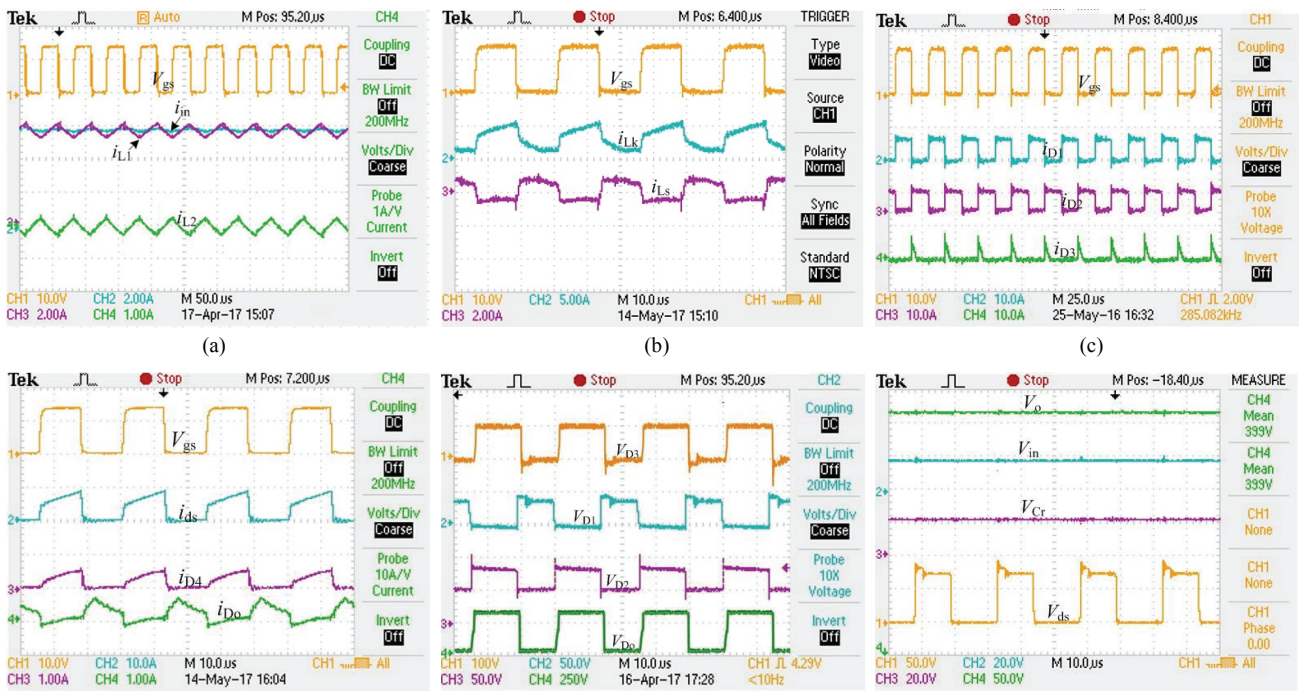

Fig. 11. Experimental prototype test waveforms. (a) V_{gs}, i_{in}, i_{L1} and i_{L2}. (b) V_{gs}, i_{Lk} and i_{Ls}. (c) V_{gs}, i_{D1}, i_{D2} and i_{D3}. (d) V_{gs}, i_{ds}, i_{D4} and i_{Do}. (e) V_{gs}, V_{D1}, V_{D2} and V_{Do}. (f) V_{ds}, V_{in}, V_o and V_{Cr} with V_{in}=18V.

addition, the energy stored in the primary and secondary side leakage inductances of T_2 is recovered into the capacitors C_3 and C_2 and eventually to the load. The diodes D_1 and D_2 are conducted in the complementary mode. Hence, they can provide loops for the charge and discharge processes of the coupled inductor T_1, which can improve the voltage gain of the converter.

As can be seen from Fig. 11(d), the output voltage can be step up to 400V when the input voltage is 18V, and the current stress of the switch is about 10A, which is consistent with the theoretical analysis and simulation test results.

Fig. 11(e) gives the gate signal of Q and voltage waveform of the diodes D_1, D_2 and D_o. It is easy to observe that the output diode can achieve approximately zero voltage switching

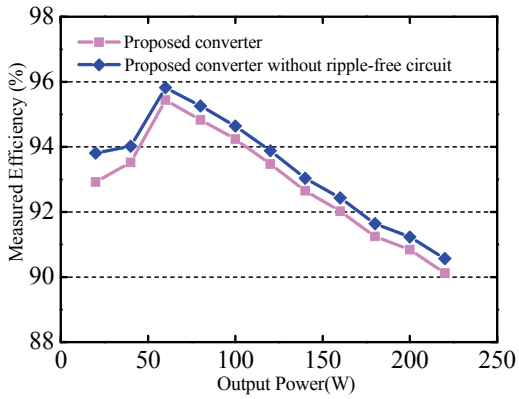

Fig. 12. Converter efficiency comparison.

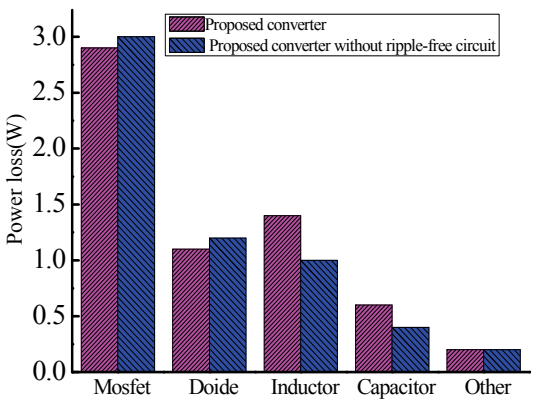

Fig. 13. Loss distribution of devices.

(ZVS). When the diode D_3 is turned off, the voltage across the diode D_3 is clamped at a low voltage (V_{Ns}+V_{C2}-V_{D4}). In addition, the voltage across the diode D_1 has a voltage drop at the same time.

Fig. 11(f) illustrates waveforms of the output voltage, the switching voltage and the voltage across the auxiliary capacitor C_r when the input voltage is 18V. The voltage stress of the switch is about 80V and the voltage across the auxiliary capacitor is only about 20V. Voltage spikes of the switch can be suppressed by a passive lossless absorption circuit composed of a diode D_3 and a capacitor C_3 at the moment of switching turn off. The current flowing through the ripple absorption circuit current is very small. Therefore, this auxiliary branch can be constructed by a capacitor and litz wire with a low tolerance parameter to reduce the place of the converter.

Fig. 12 shows an efficiency comparison of the proposed converter and a converter without a ripple absorption circuit under different loads. As can be seen from Fig. 13, the proposed converter with a ripple absorption circuit contains additional conduction loss due to the auxiliary capacitance and inductance. In addition, the switching device loss and the energy storage device loss of the proposed converter are lower than the converter without a ripple absorption circuit. Therefore, the conversion efficiency of the converter proposed in this paper is slightly lower than the high gain converter without a ripple absorption circuit. The maximum efficiency of the high gain converter without a ripple absorption circuit is 95.82%, and proposed high gain converter proposed achieves a maximum efficiency of 94.83% when the power is P_o=60W. Nevertheless, a very small input ripple that is close to zero can be obtained from the high gain converter proposed in this paper, which can provide a good alternative option with attractive performance for some occasions such as PV generation systems.

VIII. CONCLUSION

In this paper, a double-coupled inductor high gain DC/DC converter with a ripple absorption circuit is proposed. When compared with a traditional quadratic high gain converter and a coupled inductor high gain converter, the proposed converter has the following advantages. 1) A voltage multiplier module composed of a diode-capacitor unit and a coupled inductor is integrated into a conventional converter, and a higher voltage gain can be obtained by configuring the turns ratio of the coupled inductor and the duty ratio, which can effectively avoid an extremely high duty cycle and reduce the leakage inductance loss caused by the weak coupling of a high frequency transformer. 2) Very small input current ripples can be achieved by using a ripple absorption circuit composed of an auxiliary inductor and a capacitor, which effectively reduces the switching devices loss. Additionally, the current through the ripple absorption circuit is small and the volume of the absorption branch is tiny. 3) The voltage stress of the switch tube can be clamped at a value much lower than the output voltage since the voltage across the switch and the output voltage are isolated by the voltage multiplying unit. 4) The leakage inductance loss of the coupled inductor can be recovered and fed back to the load in a switching period, which can improve the efficiency of the converter.

APPENDIX

This appendix provides the approximate derivation used to estimate the loss breakdown in the proposed converter [14]. The loss in the active switch is mainly conduction losses [32]. The conduction losses are estimated using the RMS current through the switch and its on-state resistance. Thus, the losses in the active switch Q are given by:

$$P_Q = I_{\text{rms}}^2 R_{\text{ds-on}} \tag{50}$$

where I_{rms} is the RMS current through the switch Q, and $R_{\text{ds-on}}$ is its on-state resistance.

The diode losses can be obtained by:

$$P_{\text{diode}} = I_{\text{rms-d}}^2 R_{\text{T}} + I_{\text{avg-d}} V_{\text{T}} \tag{51}$$

where $I_{\text{rms-d}}$ is the RMS current through the diode, R_{T} is its on-state resistance, $I_{\text{avg-d}}$ is its average current, and V_{T} is its on-state voltage drop.

The capacitor losses are estimated by using the following equation:

$$P_{\text{capacitor}} = I_{\text{rms-c}}^2 R_{\text{ESR}} \tag{52}$$

where $I_{\text{rms-c}}$ is the RMS current through the capacitor and R_{ESR} is its equivalent series resistance.

The losses in the magnetic components are comprised of the core losses and the winding losses [10]. The core losses are estimated as:

$$P_{\text{core}} = (k f_{\text{s}}^{1.23} B_{\text{ac}}^{2.12})(W_{\text{tfe}})(10^{-13}) \tag{53}$$

where k is the eddy current loss coefficient, B_{ac} is the magnetic flux variation, and W_{tfe} is the core weight in grams.

The winding losses in T_1, T_2 and L_{r} are estimated by using the following equation:

$$P_{\text{cu-wire}} = I_{\text{rms-cu}}^2 R_{\text{cu}} \tag{54}$$

where $I_{\text{rms-cu}}$ is the RMS current through the wire, and R_{cu} is the resistance of the wire.

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