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Zero-Voltage and Zero-Current Switching Interleaved Two-Switch Forward Converter

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Abstract

In this paper, a novel zero-voltage and zero-current switching (ZVZCS) interleaved two switch forward converter is proposed. By using a coupled-inductor-type smoothing filter, a snubber capacitor, the parallel capacitance of the leading switches and the transformer parasitic inductance, the proposed converter can realize soft-switching for the main power switches. This converter can effectively reduce the primary circulating current loss by using the coupled inductor and the snubber capacitor. Furthermore, this converter can reduce the reverse recovery loss, parasitic ringing and transient voltage stress in the secondary rectifier diodes caused by the leakage inductors of the transformer and the coupled inductance. The operation principle and steady state characteristics of the converter are analyzed according to the equivalent circuits in different operation modes. The practical effectiveness of the proposed converter was is illustrated by simulation and experimental results via a 500W, 100 kHz prototype using the power MOSFET.

Key words: Interleaved, Passive auxiliary resonant circuit, Two switch forward converter, Zero-current-switching (ZCS), Zero-voltage-switching (ZVS)

I. INTRODUCTION

With the development of power electronics technology, soft switching technology plays an important role in high frequency processes of PWM converters. Under the same condition, the soft switching converters can work at higher switching frequency compared to the hard switching converters. Meanwhile, soft switching technology can improve the operating reliability of switches, reduce the sizes of converters, suppress excessive *di/dt* and *dv/dt*, reduce power losses and enhance efficiency. Moreover, it can effectively cut down electromagnetic interference (EMI) and system noise [1], [2].

The forward converter is a widely used isolated DC/DC converter, especially in low and medium power applications [3]-[10]. Since the requirements of topological standardization in system integration are higher and higher, a series of forward converters has been presented. Two-switch forward converters [11]-[19] reduce the voltage stress on switches and creates development conditions for high-input-voltage forward converters. The active clamp forward converters [14]-[18] solve the problem of high turn-off voltage spikes at the switches of forward converters. However, these two types of converters both increase the number of switches without increasing the transmission power. Although the active clamp circuit can create the ZVS turn-on condition for the main and auxiliary switches, the efficiency of the converter is restricted as a result of increasing the resonant circuit losses and circulating losses. Interleaved two-switch forward converters [20]-[24] reduce the output filter current ripple and the filter elements size. Moreover, they improve the power density and the fault tolerance of the converter. However, the interleaved structure cannot solve the problem of high turn-off voltage spikes at the switches.

Paper [25] proposed an interleaved two-switch forward converter with a coupled inductance. By employing a coupled output inductor, parallel capacitor of the switch and transformer leakage inductors, the converter in [25] can realize soft switching for all of the switches, reduce the circulating current, and achieve high efficiency. However, in order to rapidly decrease the primary current to zero, it has to increase the turn-ratio of the coupled inductor. In this case, the voltage stress and parasitic ringing in the freewheeling and rectification diodes are increased. For the purpose of

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suppressing the parasitic ringing, the saturable reactors connected in series with the secondary windings are essential [26]. However, the use of the saturable reactors produces an additional loss and heat in the saturable core.

Accordingly, based on the converter proposed in [25], aiming at the DC converters used in aviation secondary power supplies, this paper proposed a novel interleaved two-switch forward converter that employs a coupled inductor and a snubber capacitance. The proposed converter has the following advantages. ① By using a simple auxiliary circuit, the proposed converter can realize soft-switching for all of the power switches. In addition, this topology improves the reset speed of the primary current. Therefore, the circulating current loss is further reduced. ② By increasing the ratio of the coupled inductor, the ZCS control of the lagging switches can be more easily realized. In addition, the proposed converter can effectively reduce the reverse recovery loss, the parasitic ringing and voltage stress in the secondary rectification diodes. ③ The circulating current of the auxiliary circuit can be self-adjusted according to the load, which is helpful for improving efficiency under a light load. Consequently, the converter can maintain a high efficiency over a wide load range.

II. Circuit Topology and Operation Principle

A. Circuit Topology

Fig. 1 shows the topology structure of the proposed ZVZCS ITSF converter with a coupled inductance and a snubber capacitor. E is the input dc voltage source. The switches S_1 and S_4, the transformer T_2, the diodes D_2 and D_4 and the rectifier diode D_6 constitute one of the forward converters. The switches S_2 and S_3, the transformer T_1, the diodes D_1 and D_3 and the rectifier diode D_5 constitute the other forward converter. The passive snubber capacitors C_1 (C_2) parallel with S_1 (S_2). L_{s1} (L_{s2}) is the secondary equivalent leakage inductance of the transformer T_1 (T_2). L_{m1} (L_{m2}) is the magnetizing inductance of the transformer T_1 (T_2). L_{d1} and L_{d2} compose the coupled output inductor. The secondary auxiliary circuit consists of the snubber capacitor C_s, the auxiliary diodes D_{s1} and D_{s2}, the freewheeling diode D_f and the coupled output inductor. C_o is the output filter capacitor. R_o is the load.

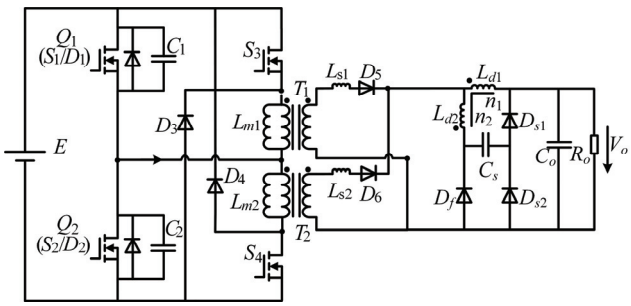


Fig. 1. Proposed ZVZCS ITSF converter.

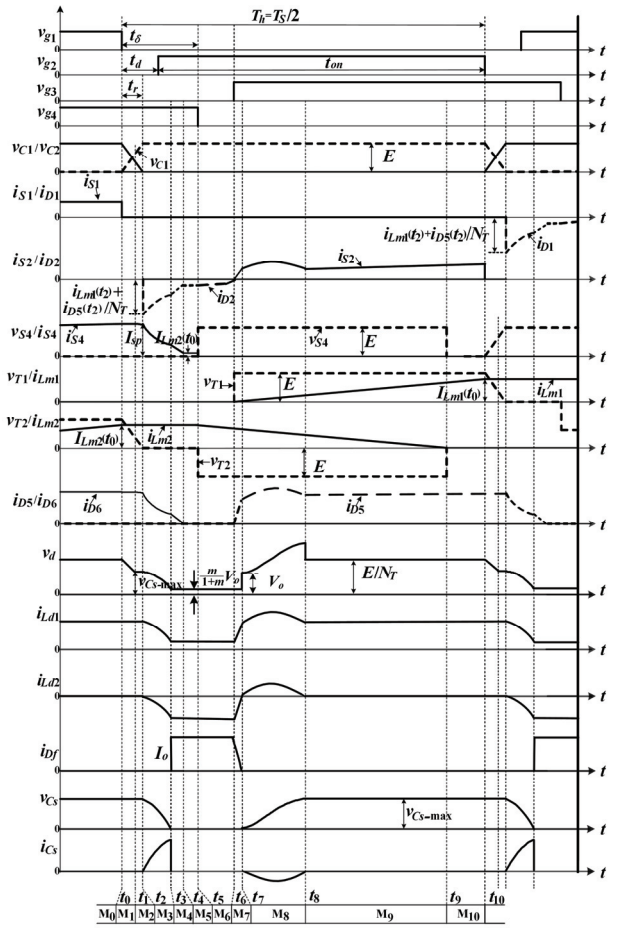


Fig. 2. Working waveforms of the proposed converter.

B. Operation Principle

Working waveforms and operation stages of the proposed converter are illustrated in Fig. 2 and Fig. 3, respectively. As shown in Fig. 2, v_{g1}~v_{g4} are driving waveforms of S_1~S_4, respectively. Moreover, S_1 (S_4) and S_2 (S_3) are driven complementary with a dead-time t_d. S_4 (S_3) turns off after S_1 (S_2) with a delay-time t_δ. T_s is one switching period. t_{on} is the conduction time of the switches. The converter output duty ratio is $D=(t_{on}-t_\delta)/T_h$, where $T_h = T_s/2$.

In order to simplify the analysis, several assumptions are made as follows.

(1) All of the switches, diodes, capacitors and inductors are ideal devices.

(2) The passive snubber capacitors in parallel with the switches are expressed as $C_1=C_2=C$.

(3) N_p and N_s are the turns of the transformer primary and secondary, respectively. In addition, the transformer turn ratio is $N_T=N_p/N_s$. The roll line resistance of the transformer is neglected.

(4) The magnetizing inductances are expressed as $L_{m1}=$

L_{m2}=L_m, which are large enough to keep the magnetizing current constant during the charging or discharging periods of C_1 or C_2.

(5) The coupled output inductors L_{d1} and L_{d2} are tightly coupled with each other. n_1 and n_2 are the turns of the coupled output inductors L_{d1} and L_{d2}, respectively. In addition, the coupled inductor turn ratio is m=n_2/n_1. Furthermore, L_{d1} is large enough and the current through L_{d1} is continuous.

(6) The output capacitor C_o is large enough to be considered as a voltage source V_o.

Before t_0, referring to Fig. 1, S_1, S_4 and D_6 are in the on state. Meanwhile, S_2 and S_3 are in the off state, and D_1~D_5, D_{s1}, D_{s2} and D_f are reverse biased. The voltages across C_1 and C_2 are zero and E, respectively. In addition, the voltage across the snubber capacitor is $V_{Cs\text{-max}}$. The dc source transfers energy to the load through the transformer and the rectifier circuit. The magnetizing current i_{Lm2} increases in a linear way. i_{Lm2} satisfies i_u=i_{Lm2}+i_{T2}, where i_{T2} is the current through the primary winding of the transformer T_2. The ten converter working stages are analyzed as follows.

Stage 1 *[t_0~t_1][see Fig.* 3(a)*]*: At t_0, S_1 ZVS turns off. In addtion, the energy stored in C_2 starts transferring to C_1. C_1 is charged while C_2 is discharged. L_{d1} and L_{m2} are large enough so that i_{D6} and i_{Lm2} are considered to be constant during this stage. The voltage across C_1 increases linearly as:

$$v_{C1}(t)=\frac{i_{Lm2}(t_0)+i_{D6}(t_0)/N_T}{2C}(t-t_0) \tag{1}$$

The voltage across C_2 decreases linearly as:

$$v_{C2}(t)=E-v_{C1}(t) \tag{2}$$

Where $i_{Lm2}(t_0)$ is the maximum current value of the magnetizing inductance L_{m2}. During this stage, both the primary voltage of the transformer T_2 and the voltage v_d rectified by D_6 decrease linearly. v_d is expressed as:

$$v_d(t)=\frac{E-v_{C1}(t)}{N_T} \tag{3}$$

The voltage of the coupled inductor L_{d2} decreases linearly with a decrease of v_d. v_{Ld2} is expressed as:

$$v_{Ld2}(t)=m\left[v_d(t)-V_o\right] \tag{4}$$

When v_d= $V_{Cs\text{-max}}$ - v_{Ld2}, D_{s2} turns on and Stage 1 ends. At t_1, the voltage across C_1 is expressed as:

$$v_{C_1}(t_1)=E-N_T\left[\frac{V_{Cs-\max}+mV_o}{1+m}\right] \tag{5}$$

Stage 2 *[t_1~t_2][see Fig.* 3(b)*]*: At t_1, D_{s2} turns on and the load current begins flowing through D_{s2}. Since C_s is large enough, i_{Lm2} and v_{Cs} remain constant during this stage. v_d is clamped at ($V_{Cs\text{-max}}$+mV_o)/(1+m). The voltage v_{C1} across C_1 and the current i_{D6} through D_6 are expressed as:

$$v_{C1}(t)=v_{C_1}(t_1)+\left[i_{D_6}(t_1)+N_T i_{L_{m2}}(t_1)\right]\sqrt{\frac{L_s}{2C}}\sin\left[\frac{t-t_1}{\sqrt{2N_T{}^2L_sC}}\right] \tag{6}$$

$$i_{D6}(t)=\left[N_T i_{L_{m2}}(t_1)+i_{D_6}(t_1)\right]\cos\left[\frac{t-t_1}{\sqrt{2N_T{}^2L_sC}}\right]-N_T i_{L_{m2}}(t_1) \tag{7}$$

Where $i_{Lm2}(t_1)$=$i_{Lm2}(t_0)$, $i_{D6}(t_1)$=$i_{D6}(t_0)$.

In order to realize the turn-on condition for D_{s2} and to provide a reliable discharge circuit for C_s, it should be ensured that ($V_{Cs\text{-max}}$+mV_o)/(1+m)<E/N_T.

At t_2, v_{C1} rises to E, v_{C2} and the transformer primary voltage drop to zero. D_2 turns on. Stage 2 ends.

Stage 3 *[t_2~t_3][see Fig.* 3(c)*]*: At t_2, D_2 turns on, and the voltage across S_2 is clamped at zero. The magnetizing current i_{Lm2} continues to be constant. C_s resonates with the transformer secondary leakage inductance L_s, v_{Cs} and i_{Cs} are expressed as:

$$v_{C_s}(t)=\left[V_{Cs-\max}+mV_o\right]\cos\left(\frac{t-t_2}{\sqrt{(1+m)^2C_sL_s}}\right)-mV_o \tag{8}$$

$$i_{C_s}(t)=\left[\frac{V_{Cs-\max}+mV_o}{1+m}\right]\sqrt{\frac{C_s}{L_s}}\sin\left(\frac{t-t_2}{\sqrt{(1+m)^2C_sL_s}}\right) \tag{9}$$

Due to the effect of the snubber capacitance C_s and the transformer secondary leakage inductance L_s, the current i_{D6} through D_6 decreases as:

$$i_{D_6}(t)=i_{D_6}(t_2)-(V_{Cs-\max}+mV_o)\sqrt{\frac{C_s}{L_s}}\sin\left(\frac{t-t_2}{\sqrt{(1+m)^2C_sL_s}}\right) \tag{10}$$

Where $i_{Lm2}(t_2)$=$i_{Lm2}(t_0)$.

At t_3, v_{Cs} decreases to zero. D_{s2} turns off, and D_f turns on, and stage 3 ends. The duration of this stage is expressed as:

$$t_{23}=\sqrt{(1+m)^2L_sC_s}\arccos\left[\frac{mV_o}{V_{Cs-\max}+mV_o}\right] \tag{11}$$

Stage 4 *[t_3~t_4][see Fig.* 3(d)*]*: At t_3, D_{s2} turns off, and D_f turns on. The load current starts flowing through D_f. The magnetizing current i_{Lm2} continues to be constant. The current i_{D6} through D_6 decrease linearly by the force of v_d, and its expression is:

$$i_{D_6}(t)=i_{D_6}(t_3)-\frac{mV_o}{1+m}\frac{1}{L_s}(t-t_3) \tag{12}$$

The primary current i_u decrease in a linear way as:

$$i_u(t)=i_{Lm2}(t_3)+\frac{i_{D6}(t)}{N_T} \tag{13}$$

Where $i_{Lm2}(t_3)$=$i_{Lm2}(t_0)$.

When i_{D6} decreases to zero at t_4, i_u decreases to the magnetizing current i_{Lm}. D_6 turns off naturally, and stage 4 ends. The duration of this stage is expressed as:

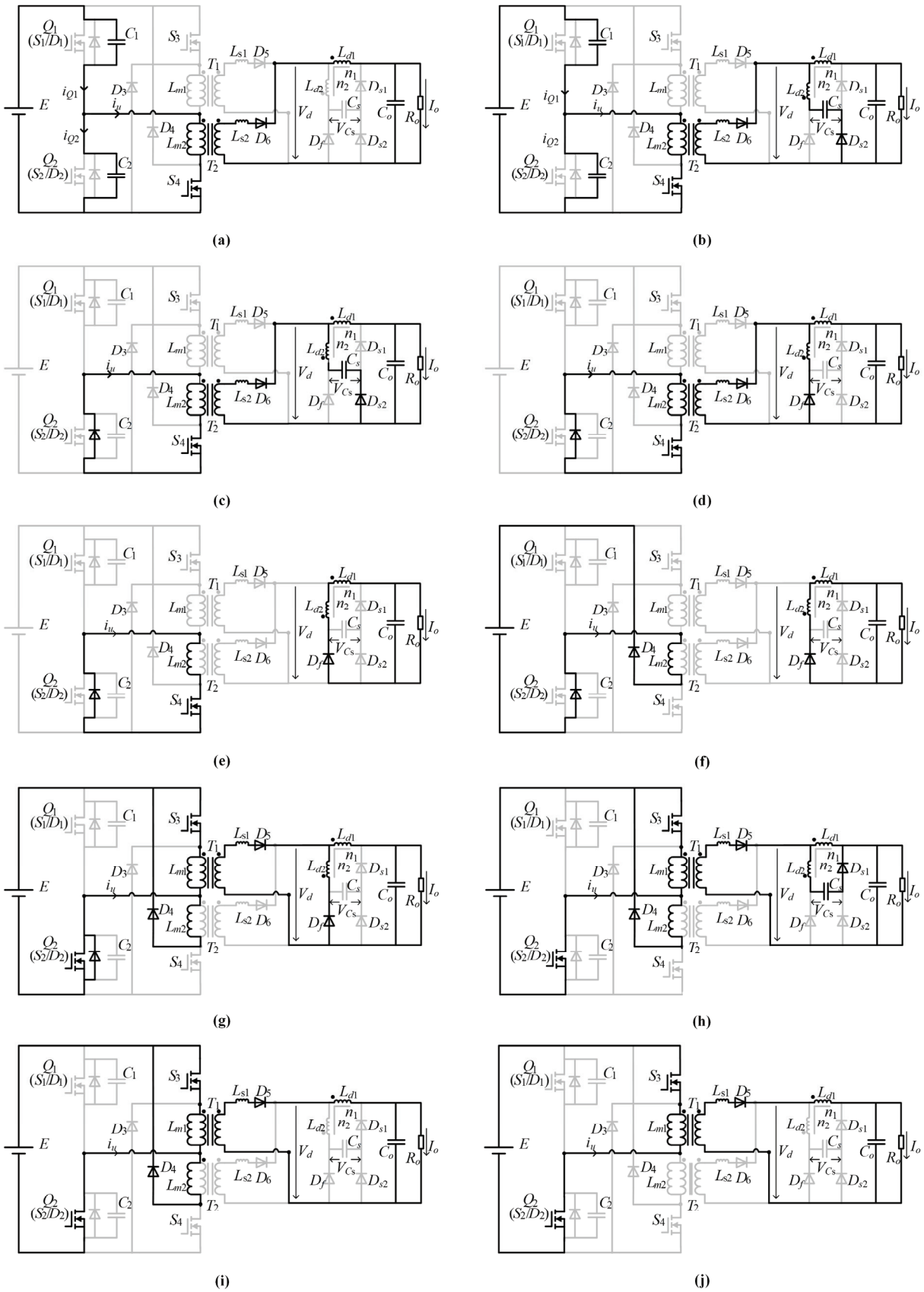


Fig. 3. Equivalent circuits of the operation stages. (a) Stage 1 [t_0-t_1]. (b) Stage 2 [t_1-t_2]. (c) Stage 3 [t_2-t_3]. (d) Stage 4 [t_3-t_4]. (e) Stage 5 [t_4-t_5]. (f) Stage 6 [t_5-t_6]. (g) Stage 7 [t_6-t_7]. (h) Stage 8 [t_7-t_8]. (i) Stage 9 [t_8-t_9]. (j) Stage 10 [t_9-t_{10}].

$$t_{34} = \frac{1+m}{mV_o} L_s i_{D6}(t_3) \tag{14}$$

Stage 5 *[t_4~t_5][see Fig.* 3(e)*]*: At t_4, D_6 turns off. The primary current i_u, which is equals to the magnetizing current i_{Lm}, flows through S_4 and D_2 for circulating. At the same time, the load current I_o flows through D_f, L_{d1} and L_{d2} for freewheeling. Because i_{Lm} is very small, only a few circulating current losses are produced. If S_4 turns off during the circulating period, near ZCS turn-off for S_4 is achieved due to the existence of the magnetizing current i_{Lm2}.

Stage 6 *[t_5~t_6][see Fig.* 3(f)*]*: At t_5, S_4 turns off, and D_4 turns on. The magnetizing current i_{Lm2} feeds back energy to the dc voltage source through D_2 and D_4. The transformer T_2 enters the magnetic reset process. i_{Lm2} decreases linearly as:

$$i_{L_{m2}}(t) = i_{L_{m2}}(t_5) - \frac{E}{L_m}(t - t_5) \tag{15}$$

Where $i_{Lm2}(t_5)$=$i_{Lm2}(t_0)$.

At t_6, S_3 turns on, and stage 6 ends. Due to the effect of L_{s1}, the current through S_3 gradually increases from zero, and S_3 can achieve ZCS turn-on.

Stage 7 *[t_6~t_7][see Fig.* 3(g)*]*: At t_6, S_3 and D_5 turn on. D_f keeps conducting to clamp v_d at $mV_o/(1+m)$. i_{Lm2} continues to decrease linearly as (15). The current i_{D5} through D_5 and the magnetizing current i_{Lm1} of the transformer T_1 increase linearly from zero as (16) and (17), respectively.

$$i_{D_5}(t) = \frac{E - N_T V_d}{N_T L_s}(t - t_6) \tag{16}$$

$$i_{Lm1}(t) = \frac{E}{L_{m1}}(t - t_6) \tag{17}$$

The current i_{S3} through S_3 increases linearly from zero as:

$$i_{S_3}(t) = [\frac{E}{L_m} + \frac{E - N_T V_d}{N_T{}^2 L_s}](t - t_6) \tag{18}$$

When $i_u(t)$=$i_{Lm2}(t)$-$i_{S3}(t)$=0, D_2 turns off. Due to the effect of D_2 and L_{m1}, S_2 achieves ZVZCS turn-on. When the current through D_5 increases to the load current I_o, D_f turns off, and stage 7 ends. The duration of this stage is expressed as:

$$t_{67} = \frac{I_o N_T L_s}{\left(E - N_T \frac{mV_o}{1+m}\right)} \tag{19}$$

Stage 8 *[t_7~t_8][see* Fig. 3(*h*)*]*: At t_7, D_f turns off. The dc source transfers energy to the load through the transformer T_1, D_5 and L_{d1}. D_{s1} turns on. The leakage inductance L_s of the transformer and the snubber capacitor C_s begin to resonate. The voltage across C_s increases from zero. v_{Cs} and i_{Cs} are expressed as:

$$v_{C_s}(t) = (1+m)(\frac{E}{N_T} - V_o)(1 - \cos\frac{t - t_7}{\sqrt{(1+m)^2 L_s C_s}}) \tag{20}$$

$$i_{C_s}(t) = (\frac{E}{N_T} - V_o)\sqrt{\frac{C_s}{L_s}} \sin[\frac{t - t_7}{\sqrt{(1+m)^2 L_s C_s}}] \tag{21}$$

At the moment of 1/2 a resonant period, v_{Cs} is charged to the maximum value $V_{Cs\text{-max}}$. The secondary transient over-voltage is clamped at V_o+$V_{Cs\text{-max}}/(1+m)$, and i_{Cs} decreases to zero. D_{s1} softly turns off, and stage 8 ends. $V_{Cs\text{-max}}$ is expressed as:

$$V_{Cs-\max} = 2(1+m)\left(\frac{E}{N_T} - V_o\right) \tag{22}$$

The duration of this stage is expressed as:

$$t_{78} = \pi\sqrt{(1+m)^2 L_s C_s} \tag{23}$$

Stage 9 *[t_8~t_9][see Fig.* 3(i)*]*: At t_8, D_{s1} turns off. i_{Lm2} continues to decrease as (15). At t_9, i_{Lm2} decreases to zero, and D_4 turns off. The transformer T_2 completes its magnetic reset, and stage 9 ends.

Stage 10 *[t_9~t_{10}][see Fig.* 3(j)*]*: At t_9, D_4 turns off. All of the energy stored in the transformer T_2 is completely delivered to the dc source. In addition, the dc source supplies energy to the load through T_1. Due to the effect of E, i_{Lm1} continues to increase linearly as (17).

At t_{10}, S_2 turns off. Half of the working stages of a switching period are completed. Due to the symmetrical configuration of the proposed converter, the analysis of the second half of the working stages is omitted.

C. Operation Principle at Light Load

At heavy load, the snubber capacitor voltage v_{Cs} is completely discharged to zero through the resonant process with the leakage inductance of the transformer during stage 3. However, at light load, the snubber capacitor has not yet been reduced to zero, while the current i_{D6} through D_6 has been decreased to zero. In this case, the duration of stage 3 is expressed as:

$$t_{23} = \sqrt{(1+m)^2 L_s C_s}\ \arcsin\left[\sqrt{\frac{L_s}{C_s}}\frac{i_{D6}(t_0)}{V_{Cs-\max} + mV_o}\right] \tag{24}$$

After the current i_{D6} through D_6 decreases to zero, the snubber capacitor supplies the load. Under the effect of the load current I_o, v_{Cs} decreases linearly as:

$$v_{Cs}(t) = v_{Cs}(t_3) - \frac{I_o}{C_s}(t - t_3) \tag{25}$$

Where $v_{Cs}(t_3)$ can be obtained by (8) and (24).

The snubber capacitor is discharged until t_7. Then C_s begins to be resonantly charged. The difference between the maximum and minimum values of the snubber capacitor voltage v_{Cs} is obtained by integrating the load current:

$$v_{Cs-\max} - v_{Cs-\min} = \frac{1}{C_s}\int_{t_1}^{t_7} i_{Cs}(t)dt \approx \frac{I_o}{C_s}(1-D)\frac{T_s}{2} \tag{26}$$

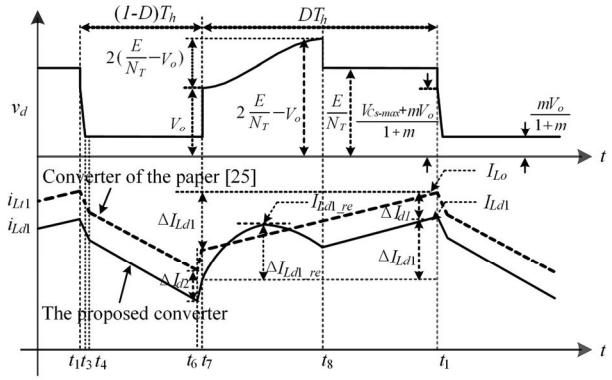


Fig. 4. Waveforms of rectified voltage and filter current.

According to (26), at light load, the resonant charging current of the snubber capacitor in (21) changes as follows:

$$\begin{aligned} i_{Cs}(t) &= \frac{(v_{Cs-\max}-v_{Cs-\min})}{1+m}\sqrt{\frac{C_s}{L_s}}\sin\frac{(t-t_7)}{\sqrt{(1+m)^2 L_s C_s}} \\ &\approx \frac{(1-D)}{(1+m)}\frac{T_s}{2}\frac{I_o}{C_s}\sqrt{\frac{C_s}{L_s}}\sin\frac{(t-t_7)}{\sqrt{(1+m)^2 L_s C_h}} \end{aligned} \tag{27}$$

According to (27), it can be observed that, under light load, the charging current of the snubber capacitor varies with the change of the load current. This means that the secondary circulating current is self-adjusted in accordance with the load condition.

III. Steady-State Characteristics of the Converter

A. The Maximum Current Stress on Switches

Fig. 4 shows waveforms of the rectified voltage v_d and output filter current i_{Ld1} of the proposed converter and the output filter current i_{Lt1} of the converter proposed in [25]. ΔI_{Ld1} and $\Delta I_{Ld1\text{-}re}$ are the linear increment and resonant increment of the output filter current i_{Ld1} in the proposed converter. I_o is the output load current. Due to the very short commutation time of the current flowing through D_5 (D_6), D_{s2} and D_f, the current i_{Ld1} of L_{d1} satisfies the following equations:

$$\begin{cases} n_1 i_{Ld1}(t_1) = (n_1+n_2) i_{Ld1}(t_4) \\ (n_1+n_2) i_{Ld1}(t_6) = n_1 i_{Ld1}(t_7) \end{cases} \tag{28}$$

Because the average value of i_{Ld1} of L_{d1} is equal to the load current I_o, the following equation is satisfied:

$$\begin{aligned} I_o &= \frac{1}{T_h}\int_0^{T_h} i_{Ld1}(t)dt \\ &= \Delta I_d + \frac{1}{2}D(2i_{Ld1}(t_1)-\Delta I_{Ld1}) + \frac{(1-D)(2i_{Ld1}(t_1)-\Delta I_{Ld1})}{2(1+m)} \end{aligned} \tag{29}$$

From (29), $i_{D6}(t_0)$ is approximately equal to:

$$i_{D6}(t_0) \approx i_{Ld1}(t_1) = \frac{I_o-\Delta I_d}{1-(1-D)\dfrac{m}{1+m}} + \frac{\Delta I_{Ld1}}{2} \tag{30}$$

The linear increment ΔI_{Ld1} is expressed as:

$$\Delta I_{Ld1} = i_{Ld1}(t_1) - i_{Ld1}(t_7) = \frac{(1-D)V_o T_h}{(1+m)L_{d1}} \tag{31}$$

$i_{Ld1}(t_7)$ is expressed as:

$$i_{Ld1}(t_7) = \frac{I_o-\Delta I_d}{1-(1-D)\dfrac{m}{1+m}} - \frac{\Delta I_{Ld1}}{2} \tag{32}$$

ΔI_d is expressed as:

$$\Delta I_d = \frac{m}{T_h}\int_{t_7}^{t_8} i_{Cs}(t)dt = \frac{2m(1+m)(\dfrac{E}{N_T}-V_o)C_s}{T_h} \tag{33}$$

The resonant increment $\Delta I_{Ld1\text{-}re}$ of the output filter current i_{Ld1} is expressed as:

$$\Delta I_{Ld1\text{-}re} = (\frac{E}{N_T}-V_o)(\frac{\pi\sqrt{L_s C_s}}{2L_{d1}} + m\sqrt{\frac{C_s}{L_s}}) \tag{34}$$

According to Fig. 4, the following equations can be satisfied:

$$\begin{cases} \Delta I_{d1} = i_{Lt1}(t_1) - i_{Ld1}(t_1) \\ \Delta I_{d2} = i_{Lt1}(t_4) - i_{Ld1}(t_4) \\ \Delta I_d = D\Delta I_{d1} + (1-D)\Delta I_{d2} \end{cases} \tag{35}$$

According to (33) and (35), ΔI_{d1} and ΔI_{d2} are expressed as:

$$\begin{cases} \Delta I_{d1} = \dfrac{\Delta I_d}{1-(1-D)\dfrac{m}{1+m}} \\ \Delta I_{d2} = \dfrac{\Delta I_d}{1+m-(1-D)m} \end{cases} \tag{36}$$

From Fig. 4, it can be observed that:

(1) When $\Delta I_{Ld1\text{-}re} \le \Delta I_{Ld1}$, the maximum current I_{SP} of the switches S_1~S_4 appears at the turn-off instant of the switches S_1 or S_2:

$$I_{SP} = i_{Lm2}(t_0) + i_{D6}(t_0)/N_T \tag{37}$$

Where $i_{Lm2}(t_0)$ can be obtained by (38).

$$i_{Lm2}(t_0) = \frac{EDT_h}{L_{m2}} \tag{38}$$

According to (30), (37) and (38), I_{SP} can be derived by:

$$I_{SP} = \frac{EDT_h}{L_{m2}} + \frac{1}{N_T}[\frac{I_o-\Delta I_d}{1-(1-D)\dfrac{m}{1+m}} + \frac{\Delta I_{Ld1}}{2}] \tag{39}$$

In this case, the current ripple ΔI_{LP} is expressed as:

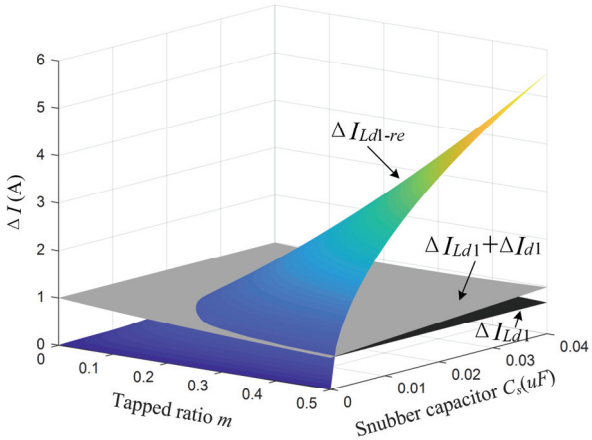


Fig. 5. Current stress on switches under different coupled inductor turn ratios m and snubber capacitors C_s (I_o=10A).

$$\Delta I_{LP}=\Delta I_{Ld1}+i_{Ld1}(t_7)-i_{Ld1}(t_6)$$
$$=\Delta I_{Ld1}+\frac{m}{1+m}\left[\frac{I_o-\Delta I_d}{1-(1-D)\frac{m}{1+m}}-\frac{\Delta I_{Ld1}}{2}\right] \quad (40)$$

(2) When $\Delta I_{Ld1\text{-}re}>\Delta I_{Ld1}$, the maximum current $I_{SP\text{-}re}$ of the switches S_1~S_4 appears at the moment of 1/2 of a resonance period during stage 8:

$$I_{SP-re}=\frac{1}{N_T}[i_{Ld1}(t_7)+\Delta I_{Ld1-re}] \quad (41)$$

Where $i_{Ld1}(t_7)$ and $\Delta I_{Ld1\text{-}re}$ can be obtained by (32) and (34), respectively.

In this case, the current ripple ΔI_{LP} is expressed as:

$$\Delta I_{LP}=\Delta I_{Ld1-re}+i_{Ld1}(t_7)-i_{Ld1}(t_6)$$
$$=\Delta I_{Ld1-re}+\frac{m}{1+m}\left[\frac{I_o-\Delta I_d}{1-(1-D)\frac{m}{1+m}}-\frac{\Delta I_{Ld1}}{2}\right] \quad (42)$$

According to the above analysis, when $\Delta I_{Ld1\text{-}re}\le\Delta I_{Ld1}+\Delta I_{d1}$, the maximum current stress on the switches of the proposed converter is less than or equal to that of the converter proposed in [25]. However, when $\Delta I_{Ld1\text{-}re}>\Delta I_{Ld1}+\Delta I_{d1}$, the maximum current stress on the switches of the proposed converter is higher than that of the converter proposed in [25].

Fig. 5 shows the effects of different coupled inductor turn ratios m and snubber capacitances C_s on $\Delta I_{Ld1\text{-}re}$, ΔI_{Ld1} and ΔI_{d1} under I_o=10A. As shown in Fig. 5, when C_s and m increase, $\Delta I_{Ld1\text{-}re}$ and ΔI_{d1} increase. ΔI_{Ld1} decreases with m increase. Selecting reasonable values of C_s and m can make the maximum current stress of the proposed converter smaller than that of the converter in [25].

B. Output Voltage Characteristics

The output voltage V_o is equal to the average value of the voltage v_d, which is rectified by the transformer secondary rectifier circuit. According to the waveform of v_d depicted in Fig. 4, V_o is given by (43).

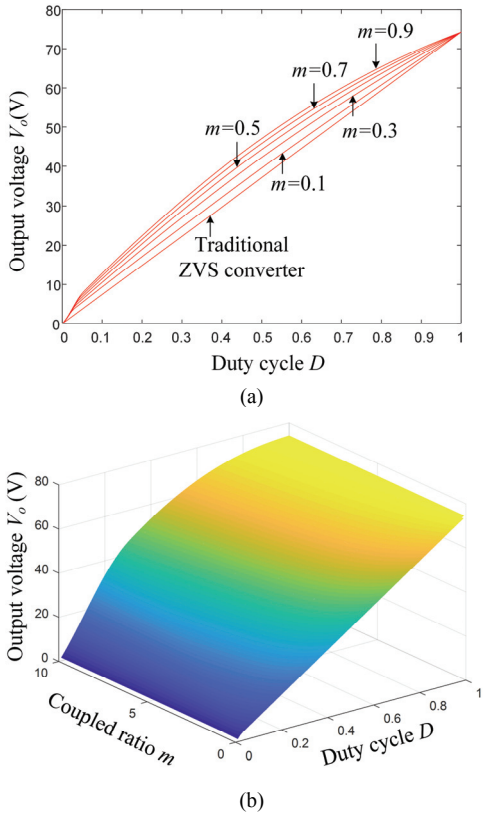


Fig. 6. Output voltage characteristics under the open-loop control strategy (E=260V, I_o=10A, C_s=6.8nF). (a) Two-dimensional plot. (b) Three-dimensional plot.

$$V_o=\frac{1}{T_h}\int_0^{T_h}v_d(t)dt$$
$$\approx\frac{E}{N_T}D+\frac{\sqrt{L_sC_s}}{T_h}\sqrt{(V_{Cs-\max}+2mV_o)V_{Cs-\max}}$$
$$+\frac{mV_o}{1+m}\left(1-D-\frac{\sqrt{(1+m)^2L_sC_s}\arccos\left[\frac{mV_o}{V_{Cs-\max}+mV_o}\right]}{T_h}\right) \quad (43)$$
$$-\frac{I_oL_s}{T_h}$$

In (43), the last part is the voltage drop caused by the transformer leakage inductance L_s. Since L_s is small enough, the last part can be neglected. Therefore, (43) can be changed as:

$$V_o\approx\frac{E}{N_T}D+\frac{\sqrt{L_sC_s}}{T_h}\sqrt{(V_{Cs-\max}+2mV_o)V_{Cs-\max}}$$
$$+\frac{mV_o}{1+m}\left(1-D-\frac{1}{T_h}\sqrt{(1+m)^2L_sC_s}\arccos\left[\frac{mV_o}{V_{Cs-\max}+mV_o}\right]\right) \quad (44)$$

Fig. 6 shows the effects of different coupled inductor turn ratios m on the output voltage characteristics under the

following conditions of the open-loop control strategy, input voltage E=260V, load current I_o=10A and snubber capacitor C_s=0.01μF. As shown in Fig. 6, when compared to the traditional ZVS ITSF converter, the linear relationship between the output voltage and the duty cycle D gets worse with the increasing of the coupled inductor turn ratio m. Therefore, the complexity of the closed-loop control strategy increases. When m<0.3, the output voltage increases almost linearly with respect to duty cycle D increases. In addition, it is beneficial for closed-loop control.

IV. Conditions to Achieve Soft-Switching

A. ZVS Condition for the Switches S_1 and S_2

t_r is the duration from S_1 turning off to the voltage of C_1 rising to E. If the dead-time t_d meets $t_r \le t_d \le T_h$, the switches S_1 and S_2 realize ZVS turn-on. According to (1), (5) and (6), t_r (see Fig. 2) is:

$$t_r = \frac{2C\left[E - N_T\left(\frac{v_{Cs-\max} + mV_o}{1+m}\right)\right]}{i_{Lm2}(t_0) + i_{D6}(t_0)/N_T} + \sqrt{2N_T{}^2 L_s C}\arcsin\sqrt{\frac{2C}{L_s}}\frac{N_T\left(\frac{v_{Cs-\max} + mV_o}{1+m}\right)}{N_T i_{Lm2}(t_0) + i_{D6}(t_0)} \tag{45}$$

From (45), to guarantee that S_1 and S_2 can achieve ZVS, the minimum load current is obtained as:

$$I_{o\text{-}\min} \ge \sqrt{\frac{2C}{L_s}} N_T\left(\frac{v_{Cs-\max} + mV_o}{1+m}\right) \tag{46}$$

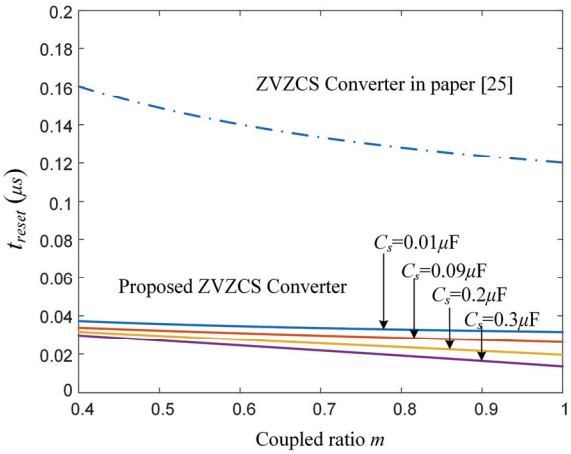
Based on the above analysis, the parallel capacitors C_1 and C_2 can limit the turn-off voltage rise rates of S_1 and S_2, respectively. The turn-off voltage rise rate and the turn-off loss decrease as the parallel capacitance increases. However, a large parallel capacitance limits the ZVS range of S_1 and S_2. Thus, it is a trade-off between the turn-off switching losses and ZVS range of the switches S_1 and S_2 in the design for parallel capacitance.

B. ZCS Condition for the Switches S_3 and S_4

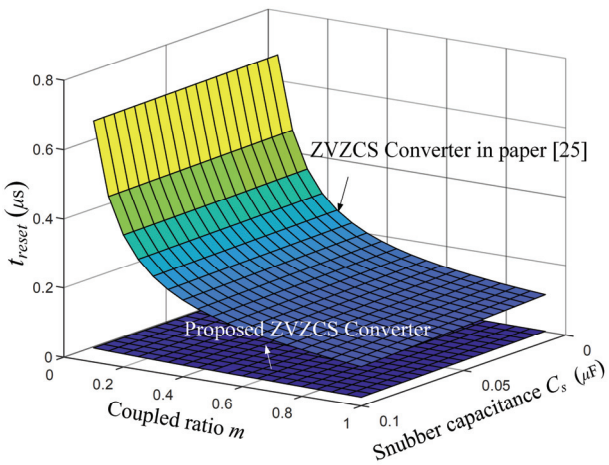
In order to achieve ZCS for the switches S_3 and S_4, the primary current must be reset to the magnetizing current before the switches S_3 or S_4 turn off. Thus, the reset time must meet the following constraint:

$$t_{reset} + t_r < t_\delta < (1-D)T_h \tag{47}$$

t_{reset} is the duration of the i_{D6} decrease to zero under the effect of the coupled inductance and the snubber capacitance C_s. According to (11) and (14), t_{reset} can be derived as:



(a)



(b)

Fig. 7. Reset times t_{reset} under different coupled inductor turn ratios and snubber capacitors. (a) Two-dimensional plot. (b) Three-dimensional plot.

$$t_{reset} = \sqrt{(1+m)^2 L_s C_s}\arccos\left[\frac{mV_o}{V_{Cs-\max} + mV_o}\right] + \frac{1+m}{mV_o}L_s\left(i_{D6}(t_2) - \sqrt{\frac{C_s}{L_s}}V_{Cs-\max}\left(V_{Cs-\max} + 2mV_o\right)\right) \tag{48}$$

Fig. 7 shows the characteristic of the reset time in the proposed converter and that of the converter in [25] under different coupled inductor turn ratios m and snubber capacitors C_s. As shown in Fig. 7, when compared with the converter in [25], the proposed converter effectively reduce the primary current reset time.

Fig. 8 illustrates the effects of the load current on the primary current reset time. Fig. 8(a) shows the variations of the primary reset times in the proposed converter and the converter in [25] with load current. In Fig. 8(a), t_A is the reset time of the converter in [25], while t_B is the reset time of the proposed converter. Their difference is $\Delta t = t_A - t_B$. When compared with t_A, the decrease ratio of t_B is $\theta = \Delta t/t_A$. Fig. 8(b) shows the relationship between the load current and the

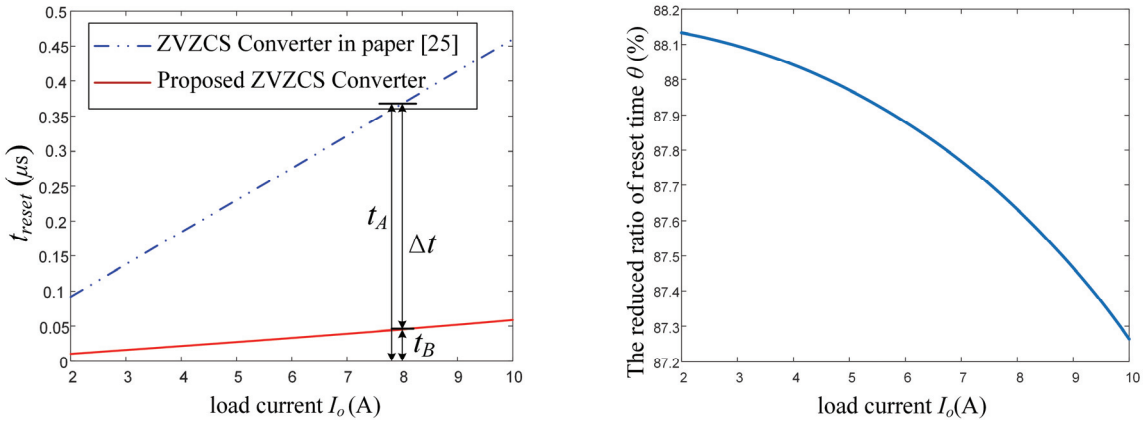


Fig. 8. Effects of different loads on the primary current reset time t_{reset}. (a) Primary current reset time. (b) Decrease ratio of the reset time.

TABLE I
VOLTAGE AND CURRENT STRESS ON THE MAIN COMPONENTS OF THREE KINDS OF ITSF CONVERTERS

	Paper [22]	Paper [25]	The proposed ZVZCS ITSF converter	
Voltage stress				
Power switches	E	E	E	
Rectifier diodes	$2E/N_T$	$2E/N_T$	$3E/N_T$-V_o	
Freewheeling diodes	E/N_T	E/N_T+V_{Lf2}	$2(1+m)(E/N_T$-$V_o)$+V_o	
Current stress			$\Delta I_{Ld1\text{-}re}\le\Delta I_{Ld1}$	$\Delta I_{Ld1\text{-}re}>\Delta I_{Ld1}$
Power switches	$\frac{EDT_h}{L_m}+\frac{1}{N_T}(I_o+\frac{\Delta I_L}{2})$	$\frac{EDT_h}{L_m}+\frac{1}{N_T}[\frac{I_o}{1-(1-D_o)N_L}+\frac{\Delta I_{Lf1}}{2}]$	$\frac{EDT_h}{L_{m2}}+\frac{1}{N_T}[\frac{I_o-\Delta I_d}{1-(1-D)\frac{m}{1+m}}+\frac{\Delta I_{Ld1}}{2}]$	$\frac{1}{N_T}[\frac{I_o-\Delta I_d}{1-(1-D)\frac{m}{1+m}}-\frac{\Delta I_{Ld1}}{2}+(\frac{E}{N_T}-V_o)(\frac{\pi\sqrt{L_sC_s}}{2L_{d1}}+m\sqrt{\frac{C_s}{L_s}})]$
Rectifier diodes	$I_o+\frac{\Delta I_L}{2}$	$\frac{I_o}{1-(1-D_o)N_L}+\frac{\Delta I_{Lf1}}{2}$	$\frac{I_o-\Delta I_d}{1-(1-D)\frac{m}{1+m}}+\frac{\Delta I_{Ld1}}{2}$	$\frac{I_o-\Delta I_d}{1-(1-D)\frac{m}{1+m}}-\frac{\Delta I_{Ld1}}{2}+(\frac{E}{N_T}-V_o)(\frac{\pi\sqrt{L_sC_s}}{2L_{d1}}+m\sqrt{\frac{C_s}{L_s}})$

decrease ratio θ. As shown in Fig. 8(b), when the load current decreases, the value of θ increases. This means that, under a light load, the decrease ratio of the primary current reset time is raised when the load current is reduced. This characteristic is beneficial to improve the efficiency of the converter under a light load.

C. Comparison of the Voltage and Current Stress on the Main Components among Different Converters

Table I shows the voltage and current stress on main components of the proposed converter, the conventional ZVS ITSF converter [22] and the ZVZCS ITSF converter using a coupled inductor [25].

The following conclusions can be drawn from Table I. (1) When $\Delta I_{Ld1\text{-}re}\le\Delta I_{Ld1}$, the current stresses on switches and rectifier diodes of the proposed converter are lower than those of the ZVZCS ITSF converter in paper [25]. (2) The voltage stresses on the power switches of the three converters are identical. The voltage stresses on the rectifier diodes and freewheeling diodes in the proposed converter are higher than those of the conventional ZVS converter in [22] and the ZVZCS ITSF converter in [25].

D. Maximum Effective Duty Cycle $D_{eff\text{-}max}$

Due to the existence of the transformer leakage inductance, at t_6, although the switches Q_2 and S_3 are both conducting, the primary current of the converter is not enough to provide the load current. During the period of [t_6, t_7], the rectifier diode and the freewheeling diodes are both conducting, and the secondary voltage of the transformer is clamped at $mV_o/(1+m)$. In this case, the voltages of [t_6, t_7] are lost in the secondary. The ratio of this duration and T_h is D_{loss}. It is expressed as:

$$D_{loss}=\frac{t_{67}}{T_h}=\frac{I_oN_TL_s}{T_h\left(E-N_T\frac{mV_o}{1+m}\right)} \tag{49}$$

Considering the ZCS realizing condition of the lagging

switches and the duty cycle loss, the expression of the maximum effective duty cycle $D_{eff\text{-max}}$ is:

$$D_{eff-\max}=1-D_{reset}-D_{loss} \tag{50}$$

Where $D_{reset}=t_{reset}/T_h$. t_{reset} can be obtained by (48).

E. Parallel Capacitance, Coupled Ratio and Snubber Capacitance Design and Coupled Inductance Values Calculation

1) Parallel Capacitance Design: The parallel capacitance should satisfy the following two rules.

① The turn-off voltage rise rate of the leading switches should be lower than the given value of q. This value is set to q=5V/ns in this paper. According to (1):

$$\frac{dv_C(t)}{dt}=\frac{I_{o-\max}}{2N_TC}<q \tag{51}$$

Where, $I_{o\text{-max}}$=10A, N_T=3.5. From (51), C should satisfy C>285pF.

② Two parallel capacitances can complete energy conversion during the dead time t_d=0.5μs, even under the condition of the lightest load. According to (45):

$$t_r\approx\frac{2CN_TE}{I_{o-\min}}<t_d \tag{52}$$

Where, $I_{o\text{-min}}$=2A, N_T=3.5, E=260V. From (52), C should satisfy C<549pF.

In summary, the range of the parallel capacitance is 285pF <C<549pF. A 300pF capacitance, which includes the parasitic capacitor in the switch, is taken to parallel with the leading switches.

2) Coupled Ratio and Snubber Capacitance Design and Coupled Inductance Values Calculation: According to the previous theoretical analysis, to effectively minimize the loss produced by the primary current during the reset period, the faster the primary current is reset, the better the effect becomes. However, the coupled ratio m and snubber capacitance C_s increase. The current stress of the power switches and rectifier diodes increase accordingly.

Under the following conditions, input voltage E=260V, output voltage V_o=50V, turn ratio of the transformer N_T=3.5 and rated load current I_o=10A, the effects of different coupled ratios m and snubber capacitances C_s on the reset time t_{reset} and the maximum current I_{SP} are shown in Fig. 9 and Fig. 10, respectively. From Fig. 9 and Fig. 10, it can be observed that with an increase in the coupled ratio and the snubber capacitor, the contribution for resetting the primary current is no more obvious than before. However, the current stress on the power switches and the rectifier diodes is increased. Moreover, the output voltage characteristic becomes worse.

Therefore, the design of the coupled ratio m and the snubber capacitance C_s should satisfy the following two rules.

① m and C_s should make the lagging switches realize ZCS turn-off even under the condition of $D_{eff\text{-max}}$.

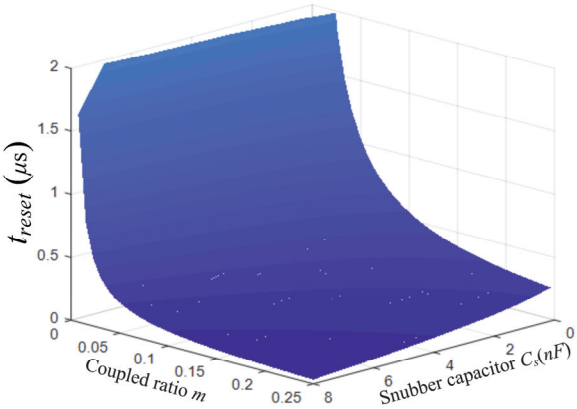


Fig. 9. Effects of different coupled inductor turn ratios m and snubber capacitors C_s on the primary current reset time t_{reset}.

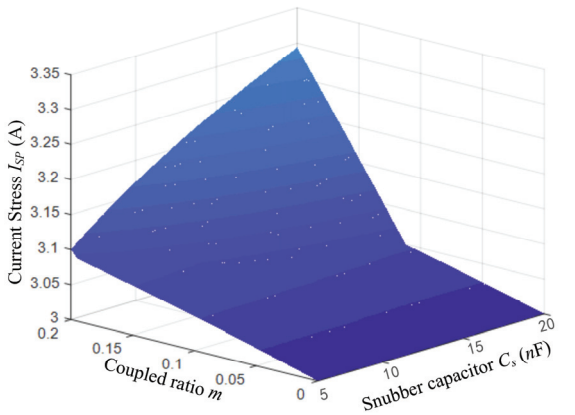


Fig. 10. Current stress of the power switches under different coupled ratios m and snubber capacitances C_s.

② In order to satisfy the requirements of the converter on the current ripple ΔI_{LP} of the output filter inductor, ΔI_{LP} should be less than a given value.

For the sake of rule ①, according to (48) and (50), the primary current reset time t_{reset} should satisfy the inequality:

$$\begin{aligned}t_{reset}=&\sqrt{(1+m)^2L_sC_s}\arccos\left[\frac{mV_o}{V_{Cs-\max}+mV_o}\right]\\&+\frac{1+m}{mV_o}L_s\left(i_{D6}(t_2)-\sqrt{\frac{C_s}{L_s}}V_{Cs-\max}\left(V_{Cs-\max}+2mV_o\right)\right)\\&\le\left(1-D_{eff-\max}-D_{loss}\right)T_h\end{aligned} \tag{53}$$

In order to correspond to rule ②, (40) should satisfy:

$$\begin{aligned}\Delta I_{LP}=&\frac{(1-D)V_oT_h}{(1+m)L_{d1}}\\&+\frac{m}{1+m}\left[\frac{I_o-\dfrac{2m(1+m)(\frac{E}{N_T}-V_o)C_s}{T_h}}{1-(1-D)\dfrac{m}{1+m}}-\frac{0.5(1-D)V_oT_h}{(1+m)L_{d1}}\right]\\\le&\,p\times I_o\end{aligned} \tag{54}$$

Where p is the ripple rate of the current through the filter inductance L_{d1}.

From (31), L_{d1} is:

$$L_{d1}=\frac{(1-D)V_oT_h}{(1+m)\Delta I_{Ld1}} \tag{55}$$

Since the coupled inductor shares a single core, the inductor L_{d2} of the coupled inductor is:

$$L_{d2}=\left(\frac{n_2}{n_1}\right)^2 L_{d1}=m^2L_{d1} \tag{56}$$

For example, assuming a rated output voltage of V_o=50V, the rated output current I_o=10A, f_s=100kHz, p=0.2, N_T=3.5, L_s=0.3μH. Taking $D_{eff\text{-}max}$=0.8, D_{loss}=0.1. From (53):

$$\begin{aligned}&\sqrt{(1+m)^2\,0.3C_s}\arccos\left[\frac{50m}{48.57+98.57m}\right]\\&+0.3\times\frac{1+m}{50m}\left(10-\sqrt{48.57(1+m)\frac{C_s}{0.3}(48.57+148.57m)}\right)\\&\le 0.5\end{aligned} \tag{57}$$

From Fig. 9 and Fig. 10, it can be observed that, when the coupled ratio m≥0.1 and the snubber capacitor C_s≥6nF, the contribution for resetting the primary current is not very obvious. Nevertheless, when m≥0.15, the current stresses of the rectifier diodes and the power switches increase a lot. Therefore, the best parameters for the coupled ratio m are between 0.1 and 0.15. In this paper, m=0.1 is chosen. Then, according to (57), the snubber capacitor should satisfy C_s≥0.7nF. In this paper, C_s=6.8nF is chosen.

According to (48) and (49), D_{reset}≈0.037 and D_{loss}≈0.009 can be calculated, respectively. In this case, D_{loss}+D_{reset}+$D_{eff\text{-}max}$≈0.846<1. As a result, C_s=6.8nF and m=0.1 can satisfy the demand.

In order to make the current stress of the switches in the proposed converter less than that of the converter in [25], the proposed converter needs to satisfy $\Delta I_{Ld1\text{-}re}\le\Delta I_{Ld1}$. According to (31) and (34), the coupled inductor L_{d1} needs to satisfy the following inequality:

$$L_{d1}\le\sqrt{\frac{L_s}{C_s}}\frac{(1-D)V_oT_h}{m(1+m)\left(\frac{E}{N_T}-V_o\right)}-\frac{\pi L_s}{2m}\approx 154\mu H \tag{58}$$

Since the linear increment ΔI_{Ld1} increases with a decrease of the coupling inductance, the current ripple also increases. Thus, ΔI_{Ld1} is set at $\Delta I_{Ld1}\le 0.1I_o$. According to (55), the following inequality is obtained:

$$L_{d1}\ge\frac{(1-D)V_oT_h}{0.1(1+m)I_o}\approx 55\mu H \tag{59}$$

According to (58) and (59), the range of the coupled inductor L_{d1} is 55μH≤L_{d1}≤154μH. In this paper, L_{d1}=120μH is chosen. From (56), L_{d2}=1.2μH. According to (40), ΔI_{LP}=1.36<pI_o. Therefore, the set values of L_{d1} and L_{d2} satisfy the demand.

TABLE II
COMPONENTS AND PARAMETERS IN THE PROTOTYPE

Components	Parameters
E (Input voltage)	260V
V_o (Output voltage)	50V
f (Switching frequency)	100kHZ
t_d(Dead time)	0.5μs
S_1~S_4 (Switches)	IPW65R065C7(650V, 33A)
D_3, D_4 (Primary diodes)	DMUR3060WT (600V, 30A)
D_5, D_6 (Rectifier diodes)	DMUR3060WT (600V, 30A)
D_f, D_{s1}, D_{s2} (Freewheeling and auxiliary diodes)	DMUR1540 (400V, 15A)
N_T (Transformer turn ratio)	3.5:1
L_m (Transformer magnetizing inductor)	3mH
L_s(Transformer secondary leakage inductance)	0.3μH
m (Coupled inductor turn ratio)	0.1
L_{d1}, L_{d2} (Coupled inductance)	120μH、1.2μH
C_1, C_2 (Parallel capacitance)	300pF
C_s (Snubber capacitance)	6.8nF
C_o (Output capacitance)	560μF

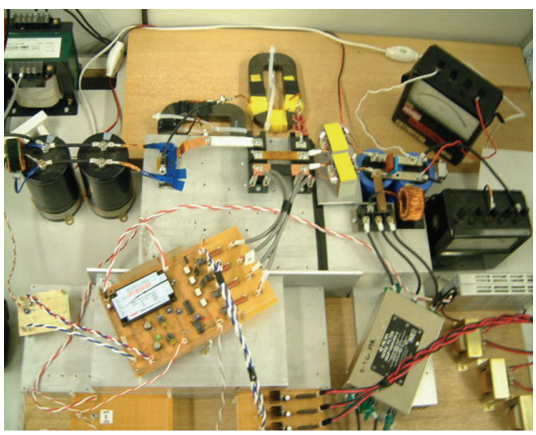


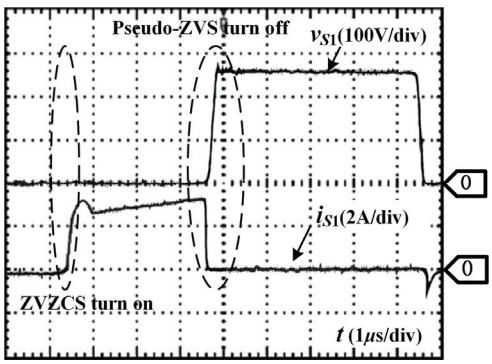
Fig. 11. Photo of the prototype converter.

V. SIMULATION AND EXPERIMENTAL RESULTS

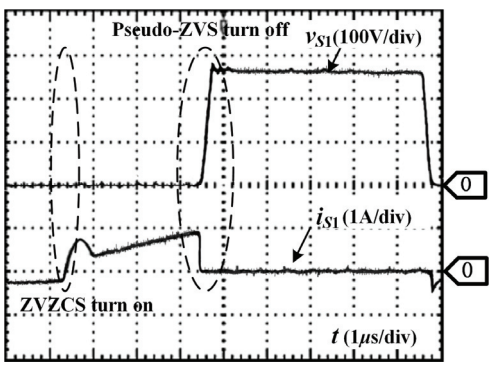
In order to verify the validity of the aforementioned analysis, a 500W, 100kHz prototype has been built. The specifications of the prototype converter are given in Table II. A photo of the prototype converter is shown in Fig. 11.

A. Waveform Evaluations

Fig. 12 and Fig. 13 show voltage and current waveforms of the leading switch S_1 and the lagging switch S_4 under a heavy load (I_o=10A) and a light load (I_o=2A), under E=260V, V_o=50V (Fig. 12(a) is a waveform of S_1 under a heavy load. Fig. 12(b) is a waveform of S_1 under a light load. Fig. 13(a) is a waveform of S_4 under a heavy load. Fig. 13(b) is a waveform of S_4 under a light load). From the obtained experimental results, it can be observed that waveforms of the

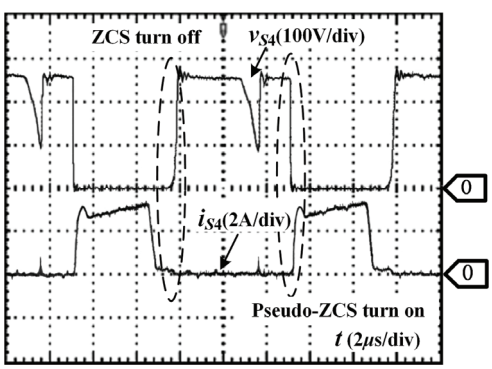


(a)

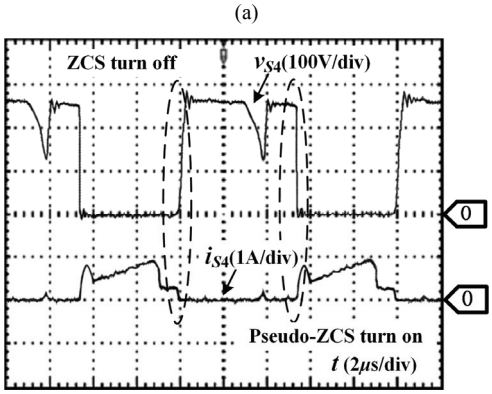


(b)

Fig. 12. Voltage and current waveforms of the leading switch S_1 (E=260V, f=100kHz, V_o=50V, t_d=0.5μs). (a) S_1 under a heavy load (I_o=10A). (b) S_1 under a light load (I_o=2A).

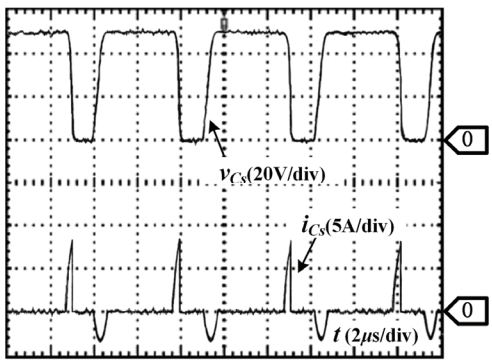


(a)

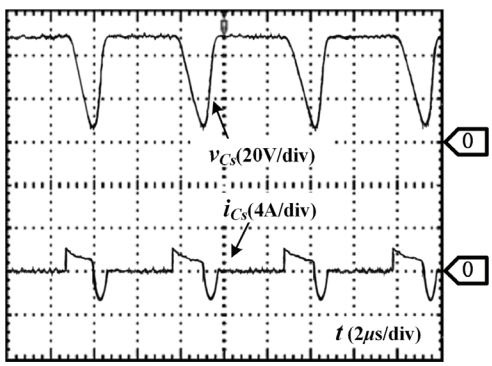


(b)

Fig. 13. Voltage and current waveforms of the lagging switch S_4 (E=260V, f=100kHz, V_o=50V, t_d=0.5μs). (a) S_4 under a heavy load (I_o=10A). (b) S_4 under a light load (I_o=2A).



(a)



(b)

Fig. 14. Voltage and current waveforms of the snubber capacitor C_s (E=260V, V_o=50V, f=100kHz). (a) C_s under a heavy load (I_o=10A). (b) C_s under a light load (I_o=2A).

power switches do not have the voltage or current spikes. In a wide load range, S_1 turns off with pseudo-ZVS and turns on with ZVZCS. S_4 turns off with near ZCS and turns on with pseudo-ZCS.

Fig. 14 shows voltage and current waveforms of the snubber capacitor under a heavy load (I_o=10A) and a light load (I_o=2A), under E=260V, V_o=50V (Fig. 14(a) is a waveform of C_s under a heavy load. Fig. 14(b) is a waveform of C_s under a light load). As shown in Fig. 14, the snubber capacitor is charged to the maximum value $v_{Cs\text{-max}}$ during the supplying period, and it is discharged to supply the load during the resetting period. From Fig. 14(a), it can be observed that the snubber capacitance is completely discharged under a heavy load. However, Fig. 14(b) shows that the snubber capacitor is not completely discharged under a light load. Meanwhile, from Fig. 14(a) and (b), the charging current under a light load is obviously less than that under a heavy load, which means that the circulating current of the auxiliary circuit is self-adjusted to the load condition. Hence, the circulating current losses of the auxiliary circuit are reduced.

Fig. 15 shows current waveforms of the coupled filter inductor in the proposed converter and the converter of [25], under E=260V, V_o=50V, I_o=10A, m=0.1, C_s=6.8nF. From Fig. 15, it can be observed that the converter in [25] has a serious parasitic ringing in the output filter inductor, which is

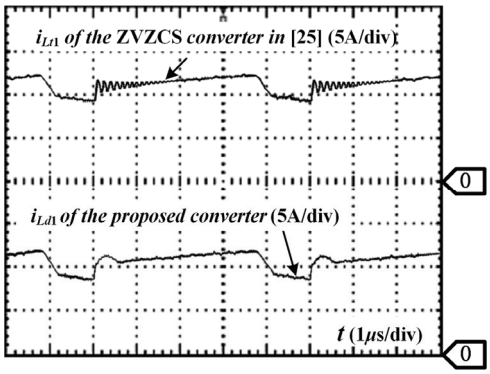


Fig. 15. The current waveforms of the coupled filter inductor (E=260V, f=100kHz, V_o=50V, I_o=10A).

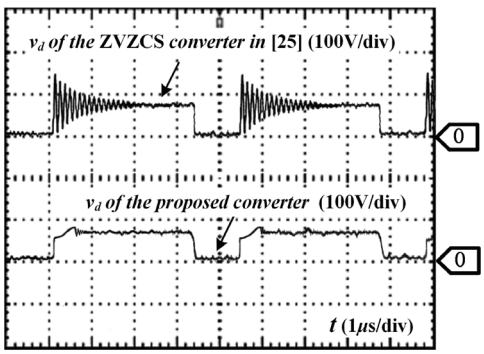
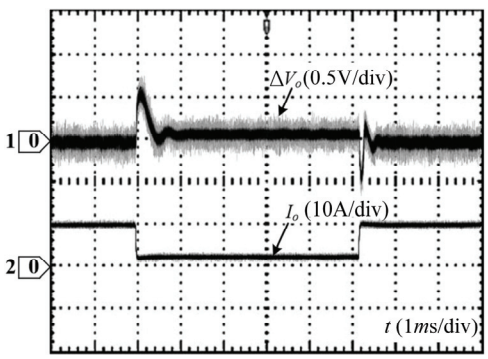
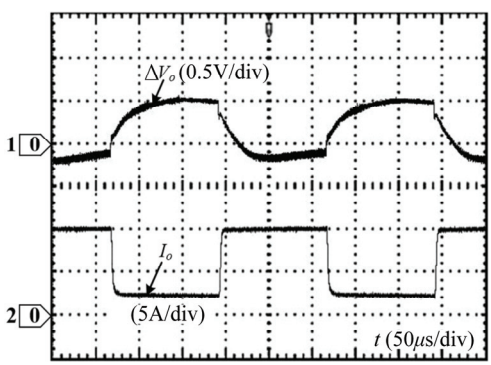


Fig. 16. Waveforms of the rectifier voltage v_d (E=260V, f=100kHz, V_o=50V, I_o=10A).



(a)



(b)

Fig. 17. Transient dynamic response of the proposed converter under output load step changes (V_o=50V).

produced by resonance among the transformer leakage inductance, the coupled inductor leakage inductance and the stray capacitors of the freewheeling diode and rectifier diode. However, as shown in Fig. 15, the proposed converter effectively suppresses parasitic ringing. This is because the proposed converter absorbs energy, which is then stored in the leakage inductances of transformer and coupled inductor, by the charging process of the snubber capacitance.

Fig. 16 compares waveforms of the rectifier voltage v_d in the proposed converter and the converter in [25]. From Fig. 16, it can be observed that by using the reverse voltage of the coupled inductor and the charging voltage of the snubber capacitance, the proposed converter can effectively suppress the transient over-voltage and parasitic ringing in the secondary side of the transformer.

B. Dynamic Response Characteristic Evaluation

Fig. 17 shows the dynamic response of the output voltage for the proposed converter when the output load is switched under an output voltage of V_o=50V. Fig. 17(a) shows the output voltage response characteristic when the load is switched from a light load (I_o=2A) to a heavy load (I_o=10A) and from a heavy load to a light load in the steady state. From Fig. 17(a), it can be seen that the voltage amplitude fluctuates within ±0.8V and that the recovery time is within 1.2ms. Fig. 17(b) shows the output voltage response characteristic when the load is quickly switched. From Fig. 17(b), it can be seen that the voltage amplitude fluctuates within ±0.6V when the load is quickly switched. From Fig. 17, it can be seen that the proposed converter has good steady state and dynamic response characteristics.

C. Efficiency Evaluation

Fig. 18 shows the distribution of the theoretical calculated losses in the proposed converter, the ZVS converter in [22] and the ZVZCS converter in [25], under a rated output power of P_o=500W. As shown in Fig. 18, the losses of the proposed converter produced by the switches Q_1/Q_2, the switches S_3/S_4, the rectifier diodes D_5/D_6, the freewheeling diode D_f, and the auxiliary diode D_{s1} and D_{s2} are, 0.48W, 0.31W, 10.34W, 2.28W, 0.08W and 0.16W, respectively. When compared with the ZVZCS converter in [25], the loss saved by the leading switches Q_1/Q_2, the lagging switches S_3/S_4, the rectifier diodes D_5/D_6 and freewheeling diode D_f are, 0.17W, 0.32W, 2.84W and 0.70W, respectively. The losses increased by the auxiliary diodes D_{s1} and D_{s2} are, 0.08W and 0.16W, respectively. In total, the losses are decreased by 3.79W. When compared with the ZVS converter in [22], the losses saved by the leading switches Q_1/Q_2, the lagging switches S_3/S_4 and the rectifier diodes D_5/D_6 are, 0.73W, 0.37W and 8.96W, respectively. The losses increased by the freewheeling diode D_f, and the auxiliary diodes D_{s1} and D_{s2} are 2.28W, 0.08W and 0.16W, respectively. In total, the losses are

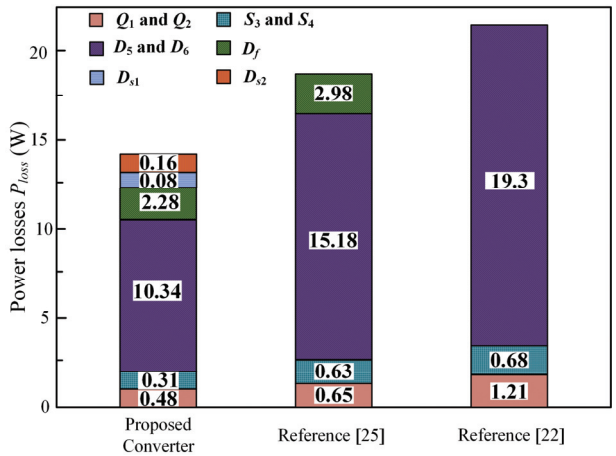


Fig. 18. Power loss analysis.

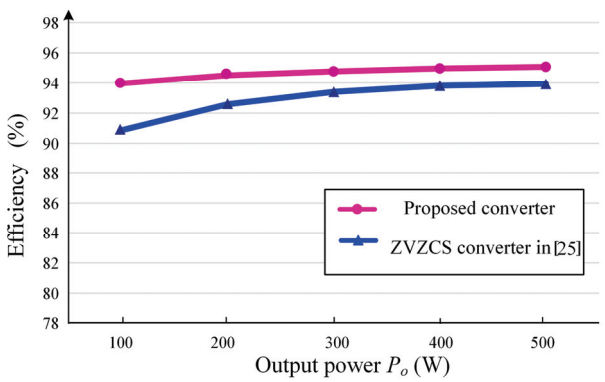


Fig. 19. Experiment efficiency curves.

decreased by 7.54W.

Fig. 19 illustrates actual power efficiency curves of the proposed converter and the ZVZCS converter in [25]. As shown in Fig. 19, in the full load range, the efficiency of the proposed converter is higher than that of the converter in [25]. In addition, the improved efficiency is more obvious with decreases in the load. The actual efficiency of the proposed converter can reach 95.2% at the rated load (500W). When compared with the ZVZCS converter in [25], the efficiency improved by nearly 1.2%. The actual power efficiency of the proposed converter is 94% under a light load (100W). When compared with the ZVZCS converter in [25], the efficiency is improved by nearly 3.2%.

VI. Conclusion

In this paper, a ZVZCS interleaved two-switch forward converter using a simple passive auxiliary resonant circuit is presented. Moreover, this paper has analyzed the operation principle, steady state characteristics and soft-switching conditions of the proposed converter. According to a theoretical analysis and experimental research, the following conclusions can be summarized.

(1) The leading switches realize ZVS turn-off and ZVZCS turn-on. The lagging switches achieve ZCS turn-on and near ZCS turn-off.

(2) By increasing the turn-ratio of the coupled inductor, the proposed converter can accelerate the speed of resetting the primary current. Thus, this converter can achieve ZCS control in lagging switches more easily.

(3) The proposed converter can overcome the effects of the reverse recovery loss, the voltage stress and the parasitic ringing in the rectifier diodes. Therefore, the topology can be extended to heavy load applications.

(4) The circulating current of the auxiliary circuit can be automatically adjusted with the load, which is helpful for improving efficiency under a light load. Thus, this converter can maintain high power conversion efficiency in the full load range.

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