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Common-Mode Current Reduction with Synchronized PWM Strategy in Two-Inverter Air-Conditioning Systems

Youngjin Baek*, Gwigeun Park**, Dongmin Park**, Honnyong Cha***, and Heung-Geun Kim†

†,*Department of Electrical Engineering, Kyungpook National University, Daegu, Korea
**Home Appliance and Air Solution Control R&D Lab, LG Electronics Inc., Changwon, Korea
***School of Energy Engineering, Kyungpook National University, Daegu, Korea

Abstract

A new method for reducing the common-mode current generated by the voltage variations in a two-inverter air conditioner system by applying a synchronized pulse-width modulation (PWM) strategy is proposed. The PWM signals of the master-mode inverter are generated based on the reference voltage, while those of the slave-mode inverter are output in the opposite direction when the master-mode inverter changes its switching state. However, the slave-mode control results in a mismatch between the reference voltage and the actual output voltage that is modified by synchronized control operation. The proposed method is capable of reducing and controlling this voltage error by performing signal selection in the vector space of the slave-mode inverter, which mitigates the distortion of the phase current. The efficacy of this method in reducing conducted emissions has been validated both theoretically and experimentally.

Key words: Air-conditioning system, Common-mode current, Conducted emission, Electromagnetic interference, Synchronized PWM strategy

I. INTRODUCTION

The development cycle for air conditioners (ACs) has become increasingly shorter, which has led to the release of a variety of AC products. Thus, it is important to reduce the duration and cost of verification procedures aimed at ensuring that their designs comply with electromagnetic interference (EMI) standards. The common-mode core, which is easy to install in power cables, is usually employed in EMI testing since it allows for the releasing of products immediately after development without violating EMI standards. Although the application of this method enables meeting EMI standards without modifying the circuits in equipment under test (EUT), the released products usually have a complicated structure. In addition, the cost of the materials increases with the implementation of this method, which negatively affects the price competitiveness of products. Consequently, many manufacturers have conducted intensive research studies to determine the fundamental causes of EMI.

When the fan motor of an AC is operated, the applied phase voltage changes due to a change in the switching state of the inverter in the circuit. This change leads to a parasitic capacitance between the motor phase and the ground, which generates common-mode current [1], which is the main cause of the conducted emission (CE) noise in ACs. The commercial 7-kW AC examined in this work uses two fans for heat exchange and contains control circuits for the inverter and fan drive motor. Accordingly, a common-mode current is constantly generated due to the voltage variation (dv/dt). Such currents produced at different loads often mutually overlap.

Multiple studies have been conducted to either restrict or reduce the flow of the dv/dt-driven common-mode current

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†Corresponding Author: kimhg@knu.ac.kr
Tel: +82-53-950-5605, Kyungpook National University
*Dept. of Electrical Engineering, Kyungpook National Univ., Korea
**Home Appliance and Air Solution Control R&D Lab, LG Electronics Inc., Korea
***School of Energy Engineering, Kyungpook National University, Korea

and resolve the EMI problem. Multilevel inverters were able to reduce this voltage variation due to changes in the switching state of the insulated-gate bipolar transistor (IGBT) [2], [3]. In a recent study, the use of an active noise filter was proposed to measu re the common-mode current generated in the EUT, which simultaneously enabled current flow in the opposite direction [4], [5]. However, these methods require the installation of additional components, and their application to AC systems results in decreases in price competitiveness.

A technique for reducing the change in common mode voltage by applying a pulse-width modulation (PWM) switching method has been examined as well [6], [7]. It decreases the magnitude of the dv/dt and the common mode current. However, it does not offset it completely. To mitigate this issue, a new method for reducing common-mode current has been developed. This method only modifies the PWM strategy without using additional components or modifying the circuits in AC systems containing two inverters for driving fans. The proposed synchronized PWM method can generate a current flowing in the direction opposite to that of the common-mode current. Since the two currents offset each other, the common-mode current measured at the input is effectively reduced. In previous works, a synchronized control strategy was applied to induction motors [8]-[12]. However, this study focused on reducing the noise caused by the dv/dt variations related to PWM switching. As a result, the voltage distortion of the permanent magnet synchronous motor (PMSM) motor can be minimized, and the current can be properly controlled.

In this paper, simulation tests were conducted under two fan loads without switching on the motor driving the compressor and indoor unit load. Compressors are another major source of AC noise. However, this study examined systems containing two motors with the same impedance. Its objective was to determine the efficacy of the proposed method in terms of inverter performance and reductions of the common-mode current and CE noise by the synchronized PWM strategy.

II. Synchronized PWM Strategy

Two types of parasitic capacitance leading to the generation of the common-mode current exist in AC systems. The first type is the capacitance between the cable connecting the inverter with the motor and the enclosure of the outdoor unit, and the second type is the capacitance between the motor winding and the motor enclosure [13]-[15]. Fig. 1 shows an equivalent circuit of the common-mode current in an AC system whose parameters can be obtained by measuring the common-mode impedance [16]. Differential mode impedances such as the stator inductance are not considered in this diagram.

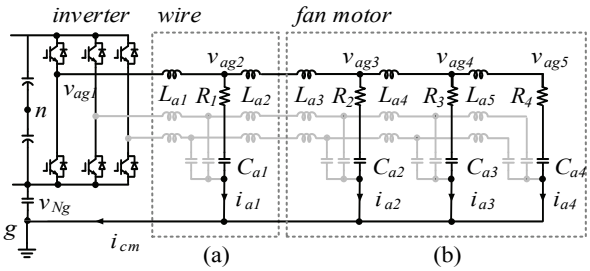


Fig. 1. Circuit diagram of the common-mode path and impedance. (a) Wire. (b) Fan motor.

A change in the phase voltage changes the electric potential between the outdoor unit enclosure (chassis ground) and the phase voltage of the motor. Among the three phases applied to the motor, the common-mode current generated in phase a can be expressed as the sum of the currents generated by the parasitic capacitors C_{a1}, C_{a2}, C_{a3} and C_{a4} as follows:

$$i_{cm} = i_{a1} + i_{a2} + i_{a3} + i_{a4} \tag{1}$$

Eq. (2) expresses the currents flowing in all of the parasitic capacitors as functions of the node voltages.

$$\begin{cases} i_{a1} = C_{a1}\dfrac{d(v_{ag2} - i_{a1}R_1)}{dt} \\ i_{a2} = C_{a2}\dfrac{d(v_{ag3} - i_{a2}R_2)}{dt} \\ i_{a3} = C_{a3}\dfrac{d(v_{ag4} - i_{a3}R_3)}{dt} \\ i_{a4} = C_{a4}\dfrac{d(v_{ag5} - i_{a4}R_4)}{dt} \end{cases} \tag{2}$$

where:

$$\begin{cases} v_{ag2} = v_{ag1} - L_{a1}\dfrac{d(\sum_{n=1}^{4} i_{an})}{dt} \\ v_{ag3} = v_{ag2} - (L_{a2} + L_{a3})\dfrac{d(\sum_{n=2}^{4} i_{an})}{dt} \\ v_{ag4} = v_{ag3} - L_{a4}\dfrac{d(\sum_{n=3}^{4} i_{an})}{dt} \\ v_{ag5} = v_{ag4} - L_{a5}\dfrac{di_{a4}}{dt} \end{cases}$$

The voltage drop caused by the parasitic inductance and resistance is negligible when compared with that caused by the capacitance. Thus, the voltages at all of the nodes can be considered equal, and the common-mode current i_{cm} can be expressed as follows:

$$\begin{aligned} i_{cm\_a} &= C_{a1}\frac{dv_{ag1}}{dt} + C_{a2}\frac{dv_{ag1}}{dt} + C_{a3}\frac{dv_{ag1}}{dt} + C_{a4}\frac{dv_{ag1}}{dt} \\ i_{cm\_a} &= C_{a\_total}\frac{dv_{ag1}}{dt} \end{aligned} \tag{3}$$

where C_{a_total} denotes the equivalent capacitance, which is equal to $C_{a1} + \cdots + C_{a4}$.

When the voltage changes due to the switching operation of the inverter, the common-mode current corresponding to the capacitance characteristics is generated. As shown in Fig. 2, a 7-kW commercial AC has two inverters sharing a single

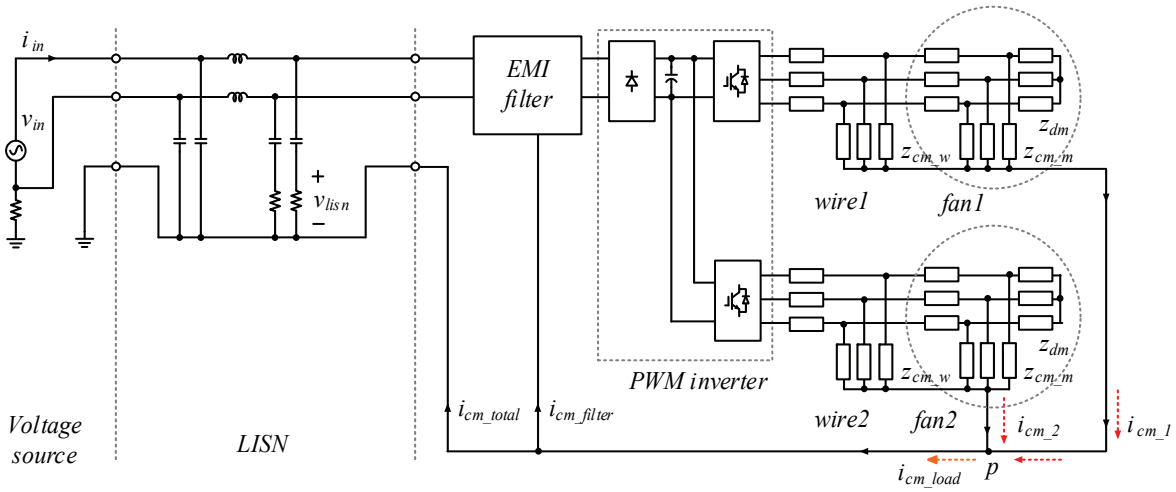


Fig. 2. Circuit diagram of the air conditioner common-mode path.

direct current (DC) power supply. If the generated common-mode currents are i_{cm_1} and i_{cm_2}, the common-mode current i_{cm_load} at point p, where these currents merge, can be expressed by Eq. (4):

$$i_{cm\_load} = i_{cm1\_load} + i_{cm2\_load} \tag{4}$$

where:

$$i_{cm1_{load}} = C_{a1_{total}}\frac{dv_{ag1}}{dt} + C_{b1_{total}}\frac{dv_{bg1}}{dt} + C_{c1_{total}}\frac{dv_{cg1}}{dt}$$
$$i_{cm2_{load}} = C_{a2_{total}}\frac{dv_{ag2}}{dt} + C_{b2_{total}}\frac{dv_{bg2}}{dt} + C_{c2_{total}}\frac{dv_{cg2}}{dt}$$

Because fans 1 and 2 use the same type of motor, the parasitic capacitance of fan 1 can be assumed to be equal to that of fan 2, i.e., $C_{x\_1total} = C_{x\_2total}$. Accordingly, if the dv/dt of fans 1 and 2 at the time of switching is applied in the opposite direction, the common-mode current i_{cm_load} at p can be maintained at a value close to zero, as shown in Eq. (5).

$$i_{cm\_load} \approx 0\left(\frac{dv_{xg1}}{dt} \approx -\frac{dv_{xg2}}{dt}\right) \tag{5}$$

Out of the two inverters, the one used to set the control criteria is called the master-mode inverter. Meanwhile the synchronized one is called the slave-mode inverter. The master-mode inverter uses the switching function $s^*_{x\_m}$, which corresponds to $T^*_{x\_m}$ calculated to generate a reference voltage. The slave-mode inverter outputs the switching function s_{x_s}, which is synchronized with $T^*_{x\_m}$ calculated for the master-mode inverter. Here, the switching function $s^*_{x\_s}$ for generating the reference voltage of the slave-mode inverter is neglected. It can be expressed as:

$$\begin{cases} s_{x\_m} = s^*_{x\_m} \\ s_{x\_s} = sync\left(s^*_{x\_m}\right) \end{cases} \tag{6}$$

Fig. 3(a) illustrates the proposed synchronized PWM method. For example, when the master inverter outputs a zero vector $\boldsymbol{V}_7$ ($T_0/2$), the slave inverter also outputs a zero vector $\boldsymbol{V}_0$. Subsequently, when the master inverter outputs $\boldsymbol{V}_2$ for $T^*_{1\_m}$, the slave inverter outputs $\boldsymbol{V}_1$ for T_{2_s} ($T^*_{1\_m}$). Thus, as soon as dv/dt exhibits a negative value at phase c of the master inverter, the dv/dt signal at phase a of the slave inverter assumes a positive value. To maintain current control stability, the two fans alternate between the master and slave modes during each PWM control period.

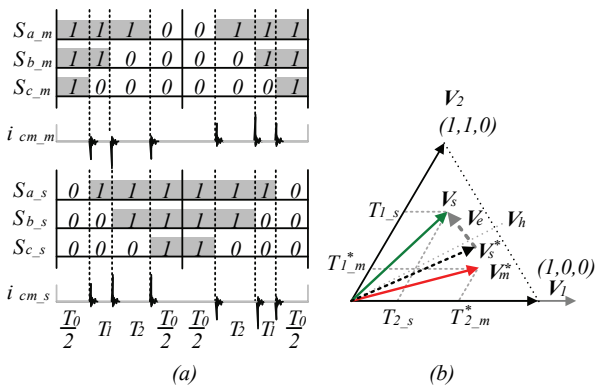


Fig. 3. Synchronized PWM strategy. (a) PWM switching function. (b) Vector diagram.

This synchronized PWM strategy ensures that the actual output voltage of the slave-mode inverter is different from the reference voltage. This difference can be expressed by the vectors depicted in Fig. 3(b). The reference voltage $\boldsymbol{V}^*_m$ of the master-mode inverter $\boldsymbol{V}_s$, which is symmetric to $\boldsymbol{V}_h$ bisecting the plane between $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$, corresponds to the actual output voltage of the slave-mode inverter, thereby generating a voltage error with respect to the reference voltage.

III. Error Reduction via the Synchronized PWM Strategy

An inverter operating in the slave mode always exhibits a

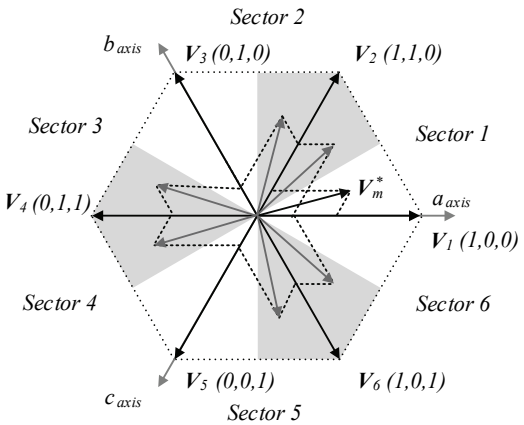


Fig. 4. Vector diagram of the synchronized PWM strategy.

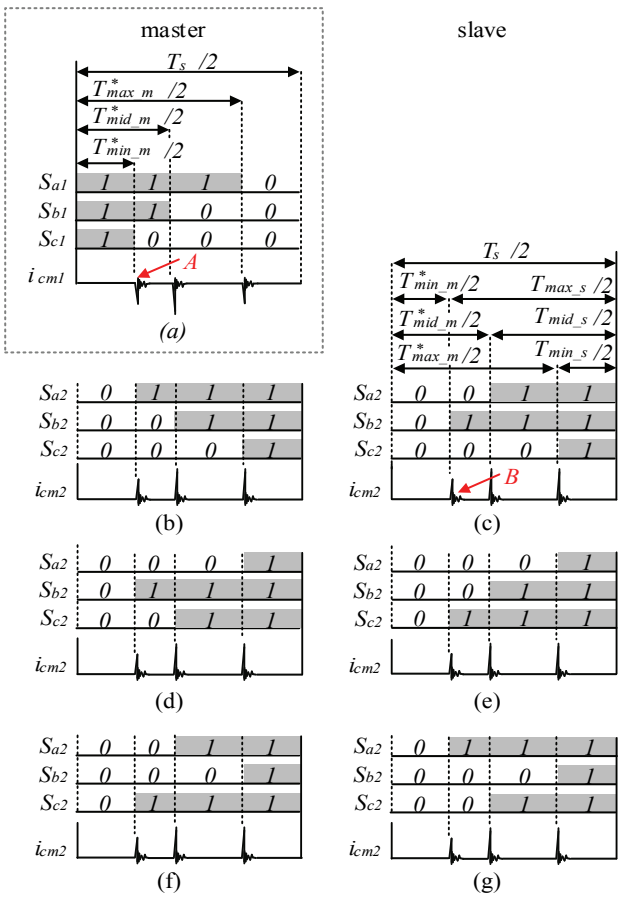


Fig. 5. Switching function of the synchronized PWM strategy. (a) Sector 1 of master mode. (b) Sector 1. (c) Sector 2. (d) Sector 3. (e) Sector 4. (f) Sector 5. (g) Sector 6.

voltage mismatch between the actual output voltage and the reference voltage leading to a distortion of the phase current. Hence, the resulting voltage error must be minimized. According to Eqns. (4) and (5), the common-mode current reduction depends on the direction of the voltage change caused by the change in the IGBT switching state. Once the switching function of the master-mode inverter is activated, the slave-mode inverter generating a dv/dt signal in the opposite direction during switching operation can have six switching functions (see Fig. 4). For a given output of the slave-mode inverter, the sector corresponding to $s^*_{x\_s}$ is maintained, and the voltage error is minimized Thus, in this paper, the implementation of the synchronized PWM strategy is based on the PWM output.

Fig. 5 depicts the six switching states s_{a2}, s_{b2}, s_{c2} of the slave-mode inverter. These states can be synchronized with the switching states s_{a1}, s_{b1}, s_{c1} to control the master-mode inverter.

The method for utilizing the difference between T_s and the target output of the master-mode inverter is expressed by Eq. (7).

$$S_{x\_s} = sync\left(s^*_{x\_m}\right) = \begin{cases} T_{min\_s} = T_s - T^*_{max\_m} \\ T_{mid\_s} = T_s - T^*_{mid\_m} \\ T_{max\_s} = T_s - T^*_{min\_m} \end{cases} \quad (7)$$

For example, when the reference voltage of the master-mode inverter is in sector 1 (Fig. 5(a)), and that of the slave-mode inverter is in sector 2 (Fig. 5(c)), the proposed control strategy ensures that the switching-off time (A) of the master-mode output $T^*_{min\_m}(s_{c1})$ at T_s coincides with the switching-on time (B) of the slave-mode output $T_{max\_s}(s_{b2})$.

Fig. 6 illustrates one case of the proposed PWM strategy. In this case, fan 1 operates in the master mode and fan 2 operates in the slave mode using the offset voltage [17].

IV. EMI Simulation

The conventional simulation procedures for an EMI analysis either examine the signal frequency attenuation or the operation of the switching element by applying a square-wave reference voltage [18], [19]. However, these procedures are less suitable for performing EMI CE simulations for the different logic states of an inverter control unit. Therefore, EMI CE was simulated in this paper by configuring a model that takes into account various loads such as the power source, line impedance stabilization network (LISN), motor wire, inverter and fan motor as well as the internal operation of the microprocessor [20].

A simulation environment was created using a circuit simulation program (TwinBuilder) [21]. A fast Fourier transform technique was used to analyze the data obtained for the LISN circuit, which was configured in the power supply network. Simulation Program with Integrated Circuit Emphasis (SPICE) models of the diode and IGBT used in actual inverters served as components. The inverter control logic was implemented using a control software design tool (SCADE) [21].

Real situations were reproduced by independently configuring the synchronized control program and the microprocessor. The simulation procedure lasted 125 ms at 10-ns intervals.

The common-mode impedance characteristics of the fan

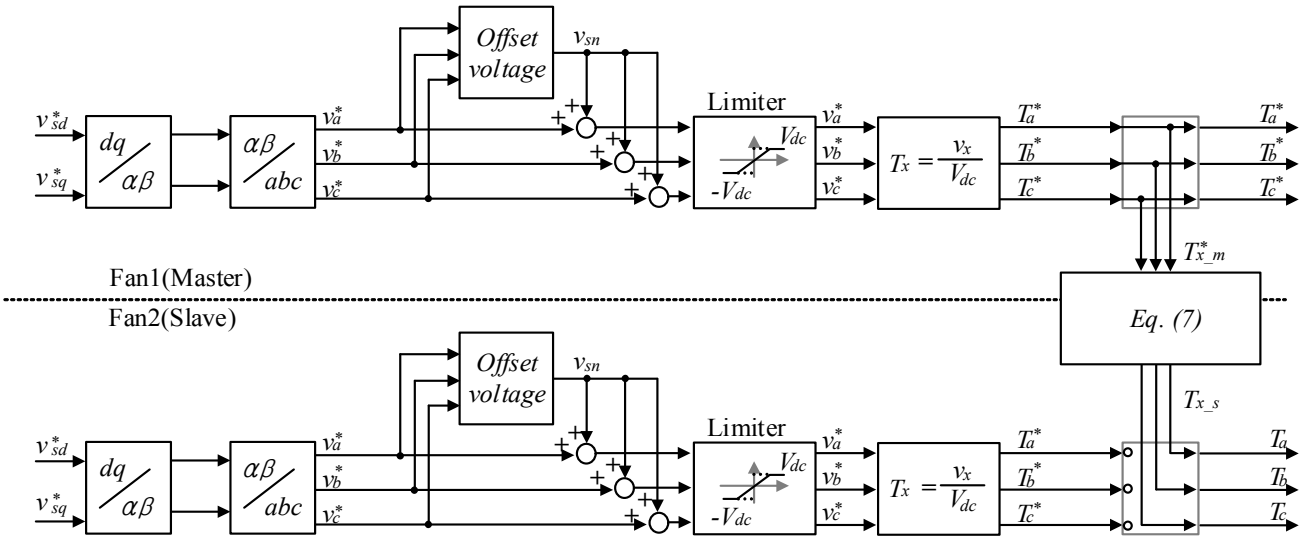


Fig. 6. Control block diagram of the synchronized PWM strategy.

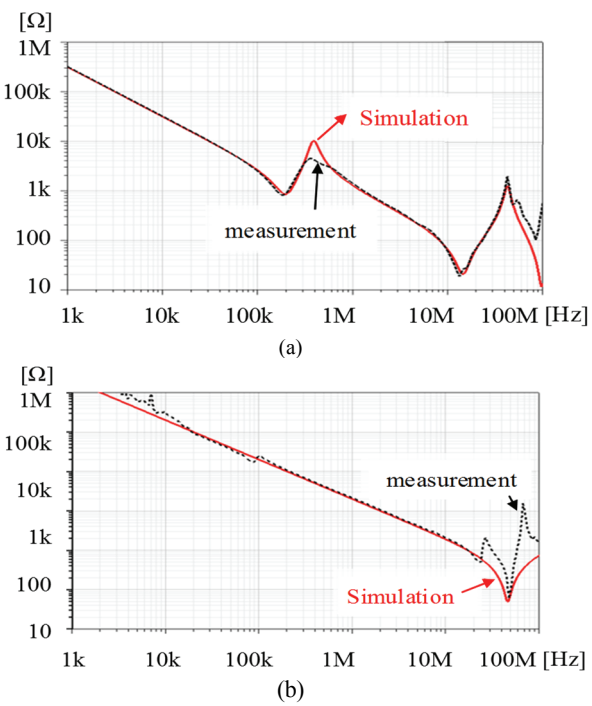


Fig. 7. Common-mode impedances of the fan motor. (a) Motor-to-chassis impedance. (b) Wire-to-chassis impedance.

motor are shown in Fig. 7(a), and the common-mode impedance between the outdoor unit enclosure and the motor wire is illustrated in Fig. 7(b). Table I lists the parameters of the circuit utilized to construct the equivalent impedance between the fan motor and the wire. As shown in Fig. 8(a), in the existing control method, the PWM-generated common-mode currents flow in the same direction. Meanwhile, when the synchronized control method is used, the IGBT states of inverters 1 and 2 simultaneously change to produce common-mode currents flowing in the opposite directions (see Fig. 9(a)).

TABLE I
FAN MOTOR AND WIRE COMMON-MODE MODEL PARAMETERS

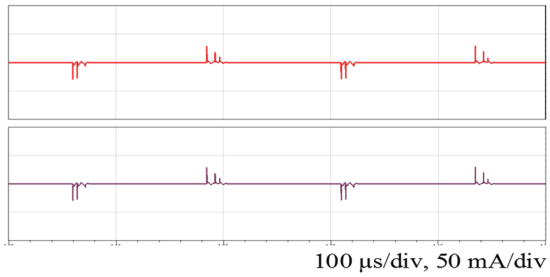
Parameter	Value	Unit
L_1, L_2	150	nH
L_3	0.5	μH
L_4	2.52	μH
L_5	5.0	mH
C_1	80	pF
C_2	6.5	pF
C_3	40	pF
C_4	123	pF
R_1	5	Ω
R_2	22	Ω
R_3	65	Ω
R_4	2.61	Ω

The existing control method often increases the sum of the common-mode currents generated by the two inverters, as shown in Fig. 8(b). However, the synchronized PWM control reduces their magnitudes (see Fig. 9(b)). When compared with the phase current of the existing method (Fig. 8(c)), the synchronized PWM strategy does not significantly distort the phase current any further, as shown in Fig. 9(c).

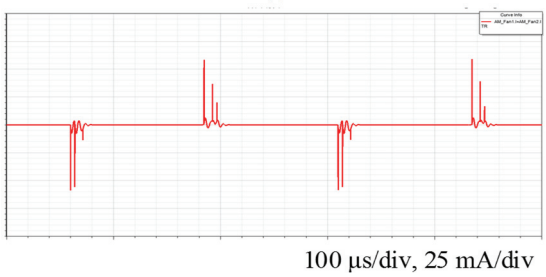
The results of the EMI CE analysis reveal that the synchronized PWM strategy yields an overall CE decrease of 6.7–20 dB (Fig. 10). In particular, the obtained decreases are equal to 20 dB at 170 kHz, 6.7 dB at 1 MHz, and 9.8 dB at 10 MHz.

V. EXPERIMENTAL RESULTS

Fig. 11 shows an experimental setup for measuring EMI CE voltages, in which a LISN is connected to a 7-kW commercial AC system in an EMI measurement chamber at room temperature. The compressor load and indoor unit were not operated. The fan control circuit was activated, and all of



(a)



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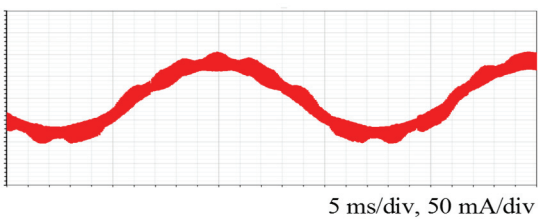
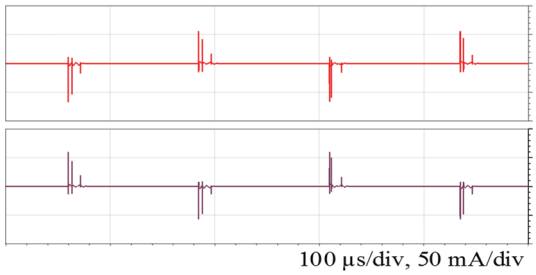
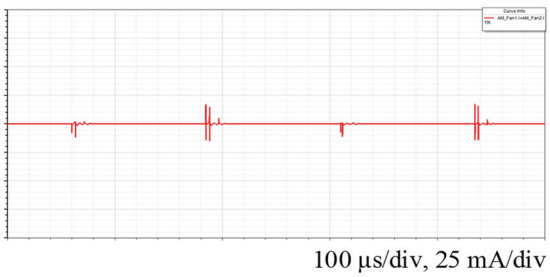


(c)

Fig. 8. Simulation results obtained without the synchronized PWM strategy (base). (a) Common-mode currents generated in fans 1 (top) and 2 (bottom). (b) Common-mode current in the GND path. (c) Phase current of the fan 1 motor.



(a)



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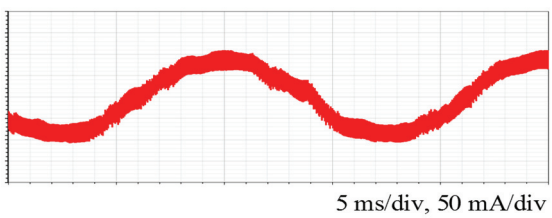

(c)

Fig. 9. Simulation results obtained with the synchronized PWM strategy. (a) Common-mode currents generated in fans 1 and 2. (b) Common-mode current in the GND path. (c) Phase current of the fan 1 motor.

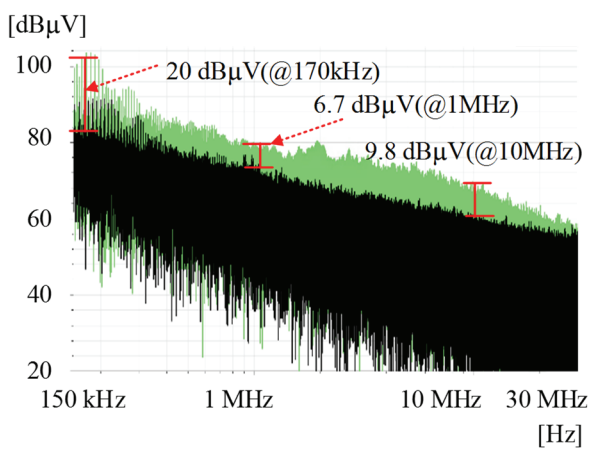

Fig. 10. Simulation results obtained with (black) and without (green) the synchronized PWM strategy.

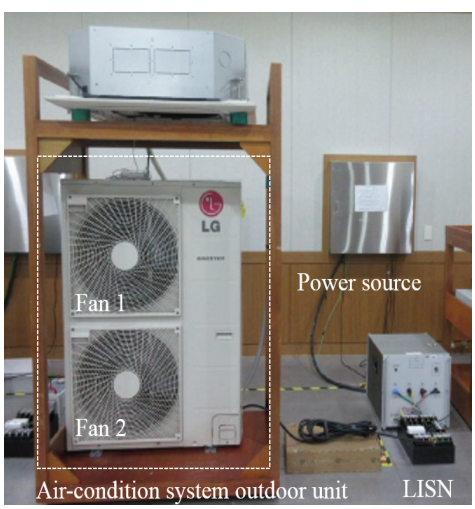

Fig. 11. Hardware setup utilized in this paper.

the EMI measurement components such as the noise filter and core were removed to evaluate only the performance of the synchronized PWM strategy. By applying the noise filter, the specified CE limits of the EMI standard can be satisfied.

When the existing PWM method is used, the two inverters perform PWM at close times. As a result, common-mode currents are generated in the same direction (Fig. 12(a)). However, the synchronized control strategy generates currents in opposite directions, as illustrated in Fig. 13(a). Furthermore, Fig. 12(b) reveals that the common-mode currents generated by fans 1 and 2 are added together. However, according to Fig. 13(b), the PWM strategy changes the distortion of the phase current very little relative to the existing method.

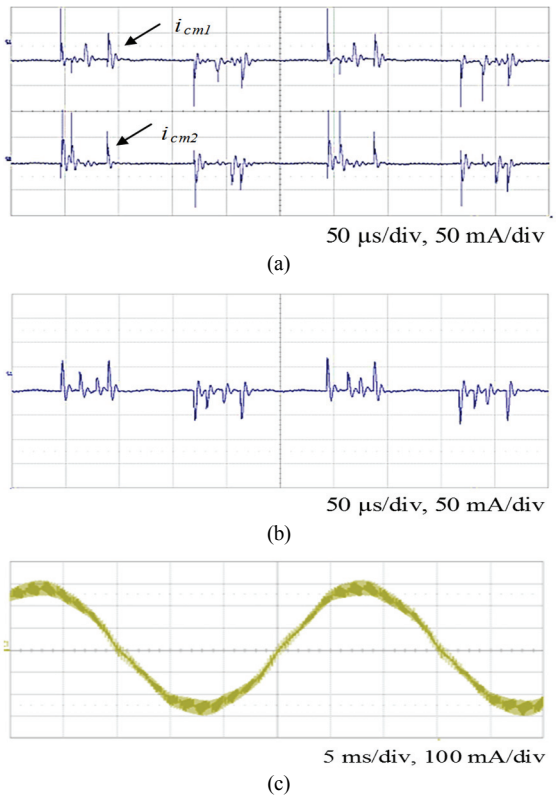

Fig. 12. Test results obtained without the synchronized PWM strategy (base). (a) Common-mode currents generated in fans 1 and 2. (b) Common-mode current in the GND path. (c) Phase current of the fan 1 motor.

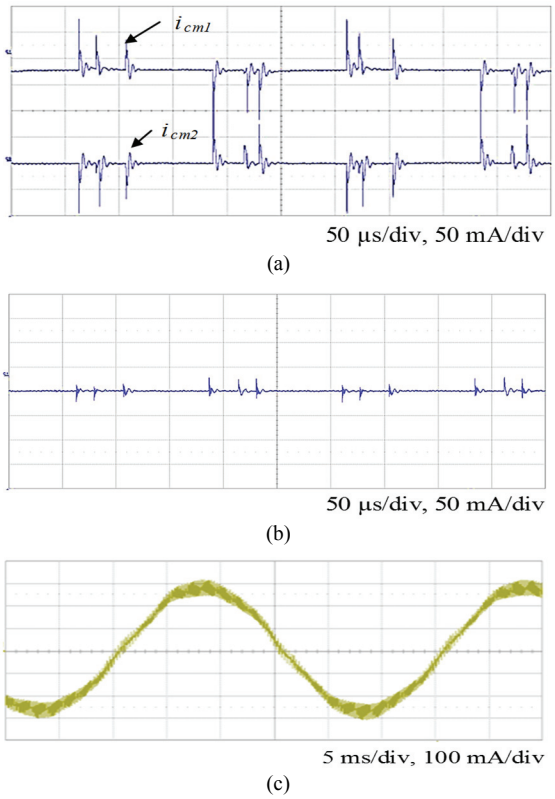

Fig. 13. Test result obtained with the synchronized PWM strategy. (a) Common-mode currents generated in fans 1 and 2. (b) Common-mode current in the GND path. (c) Phase current of the fan 1 motor.

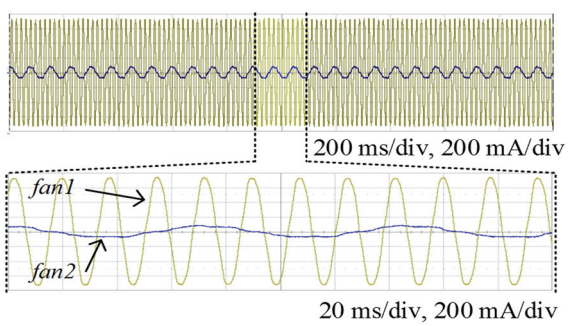

Fig. 14. EMI (CE) test results obtained with the synchronized PWM strategy at different operating conditions (fan 1 speed: 200 rpm; fan 2 speed: 900 rpm).

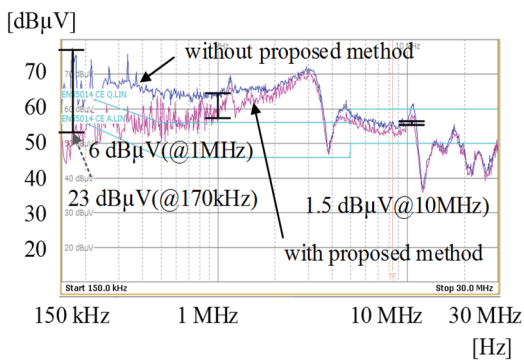

Fig. 15. EMI (CE) test results obtained with and without the synchronized PWM strategy.

This observation is confirmed by comparing waveforms of phase currents generated by the existing and the proposed PWM control methods in Figs. 12(c) and 13(c), respectively. Phase current distortion does not occur when the two fans are operated at different speeds, as shown in Fig. 14. In this paper, their values are equal to 200 rpm for fan 1 and 900 rpm for fan 2 since the fan rotation speed in ACs can vary from 200 to 900 rpm. Fig. 14 shows a magnified waveform of the phase current.

The results of EMI CE measurements (Fig. 15) revealed that noise reductions of 23, 6 and 1.5 can be achieved at frequencies of 170 kHz, 1 MHz and 10 MHz, respectively. Unlike the simulated case, the experimental data demonstrated that the noise level was reduced in the range from 150 kHz to 1 MHz. When compared with the simulation results, the experimental values exhibited smaller reductions at frequencies equal to 1 MHz or greater due to differences in the printed circuit board patterns, single IGBT components and motor impedances in the final products. Measuring the CE in the commercial AC tested in this study is typically very expensive in the low-frequency range (near 150 kHz), which makes the proposed method more attractive.

VI. CONCLUSIONS

In this paper, a new synchronized PWM strategy for reducing the common-mode currents in AC systems with multiple inverters is proposed. An alternative method was employed to avoid the instability of a PMSM (fan motor) with a vector control, and a special sector selection methodology was applied to reduce voltage errors. As a result, the distortion of the phase current was significantly reduced. Simulation tests conducted to verify the proposed strategy reveal that the EMI CE decreased under the EMI conditions for ACs.

Thus, the common-mode currents were successfully reduced by changing the control method without adding new hardware or modifying the existing one. The EMI CE value was improved by 6–23 dB in the frequency range from 150 kHz to 1 MHz. Further studies in this area should focus on developing new methods for reducing the voltage error when two fans operate at different speeds.

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Youngjin Baek received his B.S. and M.S. degrees from the Department of Electrical and Electronics Engineering, Korea Maritime and Ocean University, Busan, South Korea, in 2008 and 2015, respectively. He is presently working in the Air Solution Control Research Lab., Home Appliance and Air Solution Company, LG Electronics Inc., Changwon, South Korea. His current research interests include inverter control, motor control, electromagnetic compatibility and simulations.

Gwigeun Park received his B.S. degree in Electronics Engineering from Kyungnam University, Kyungnam, South Korea, in 1990; and his M.S. and Ph.D. degrees from Busan National University, Pusan, South Korea, in 2006 and 2010, respectively. In 1990, he joined the Air Solution Control Research Lab., Home Appliance and Air Solution Company, LG Electronics Inc., Changwon, South Korea. Since 2013, he has been working as a Research Fellow. His current research interests include motor drives, the control of electrical machines, power converters, EMC and inverter air conditioners.

Dongmin Park was born in Suwon, Korea, in 1986. He received his B.S. and M.S. degrees from the Department of Control and Instrumentation Engineering, Seoul National University of Science and Technology, Seoul, South Korea, in 2010 and 2013, respectively. He is presently working at the Air Solution Control Research Lab., Home Appliance and Air Solution Company, LG Electronics Inc., Changwon, Korea. His current research interests include inverter control, motor drives, EMC and simulations.

Honnyong Cha received the B.S. and M.S. degrees in Electronics Engineering from Kyung pook National University, Daegu, South Korea, in 1999 and 2001, respectively and the Ph.D. degree in Electrical Engineering from Michigan State University, East Lansing, MI, USA, in 2009. From 2001 to 2003, he was a Research Engineer with the Power System Technology Company, Ansan, South Korea. From 2010 to 2011, he was a Senior Researcher with the Korea Electrotechnology Research Institute, Changwon, South Korea. In 2011, he joined the School of Energy Engineering, Kyungpook National University. In 2017, he was a Visiting Scholar with the Future Energy Electronics Center, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. His current research interests include high-power dc-dc converters, dc-ac inverters, Z-source inverters, and power conversion for electric vehicles and wind power generation.

Heung-Geun Kim was born in Busan, South Korea, in 1956. He received the B.S., M.S. and Ph.D. degrees in Electrical Engineering from Seoul National University, Seoul, South Korea, in 1980, 1982 and 1988, respectively. Since 1984, he has been with the Department of Electrical Engineering, Kyungpook National University, Daegu, South Korea, where he is currently a Full Professor and the Director of the Microgrid Research Center. From 1990 to 1991, he was a Visiting Scholar with the Department of Electrical and Computer Engineering, University of Wisconsin-Madison, Madison, WI, USA. From 2006 to 2007, he was with the Department of Electrical Engineering, Michigan State University, East Lansing, MI, USA. His current research interests include ac machine control, photovoltaic power generation and microgrid systems.